- **Low Supply-Voltage Range, 1.8 V . . . 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 160 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.9 μA**
  - **Off Mode (RAM Retention) : 0.1 μA**
- **Low Operating Current:**
  - **2.5 μA at 4 kHz, 2.2 V**
  - **160 μA at 1 MHz, 2.2 V**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Timer With Three Capture/Compare-With-Shadow Registers, Timer_B**
- **16-Bit Timer With Three Capture/Compare Registers, Timer_A**
- **On-Chip Comparator**
- **Serial Communication Interface (USART), Software Selects Asynchronous UART or Synchronous SPI**
- **Programmable Code Protection With Security Fuse**
- **Family Members Include:**
  - **MSP430C1331: 8KB ROM, 256B RAM**
  - **MSP430C1351: 16KB ROM, 512B RAM**
- **Available in 64-Pin Quad Flat Pack (QFP)**
- **MTP and Emulation: Use MSP430F13xIPM**

description

The Texas Instruments MSP430 series is an ultralow-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for use in extended-time applications. The MSP430 achieves maximum code efficiency with its 16-bit RISC architecture, 16-bit CPU-integrated registers, and a constant generator. The digitally-controlled oscillator provides wake-up from low-power mode to active mode in less than 6 μs. The MSP430C13x1 is a microcontroller configuration with two built-in 16-bit timers, one universal serial synchronous/asynchronous communication interfaces (USART), and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system. The timers make the configurations ideal for industrial control applications, hand-held meters, etc.

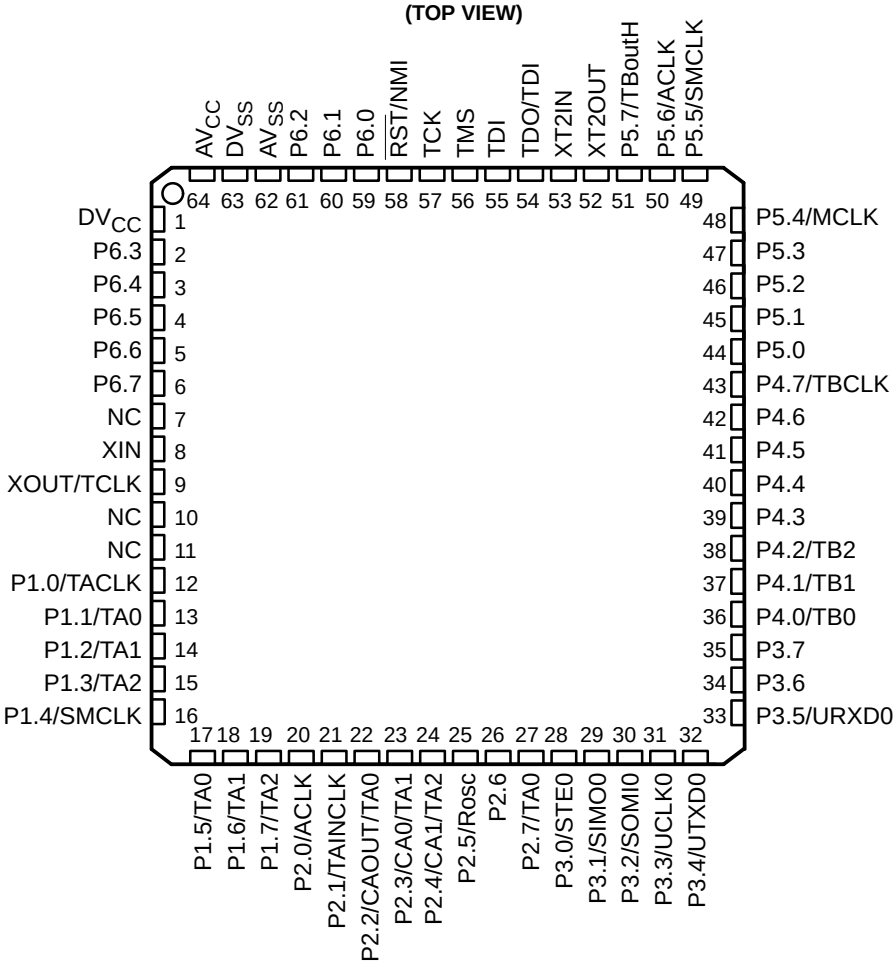
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
–40°C to 85°C	MSP430C1331IPM MSP430C1351IPM

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

pin designation, MSP430C1331, MSP430C1351

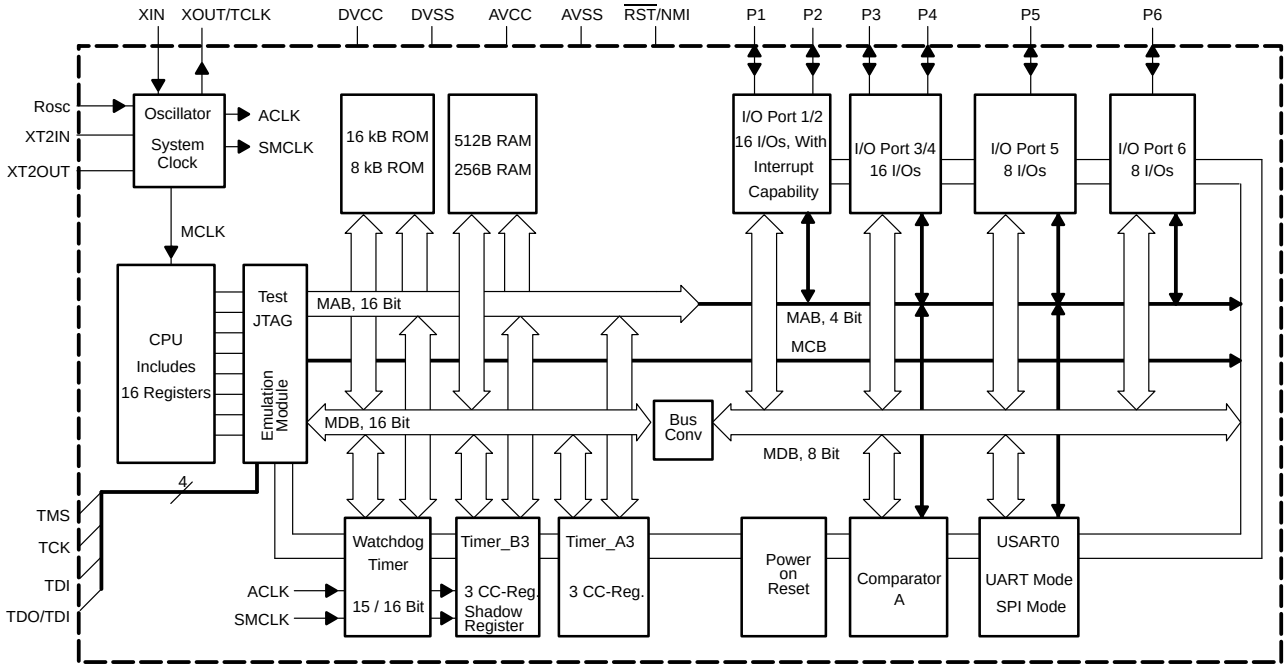
PM PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagrams

MSP430C13x1



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{CC}	64		Supply voltage, positive terminal. AV_{CC} and DV_{CC} are internally connected together.
AV_{SS}	62		Supply voltage, negative terminal. AV_{SS} and DV_{SS} are internally connected together.
DV_{CC}	1		Supply voltage, positive terminal. AV_{CC} and DV_{CC} are internally connected together.
DV_{SS}	63		Supply voltage, negative terminal. AV_{SS} and DV_{SS} are internally connected together.
P1.0/TACLK	12	I/O	General digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	14	I/O	General digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General digital I/O pin/Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output
P2.3/CA0/TA1	23	I/O	General digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc	25	I/O	General-purpose digital I/O pin, input for external resistor defining the DCO nominal frequency
P2.6	26	I/O	General digital I/O pin
P2.7/TA0	27	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General digital I/O, slave transmit enable – USART0/SPI mode

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P3.1/SIMO0	29	I/O	General digital I/O, slave in/master out of USART0/SPI mode
P3.2/SOMI0	30	I/O	General digital I/O, slave out/master in of USART0/SPI mode
P3.3/UCLK0	31	I/O	General digital I/O, external clock input – USART0/UART or SPI mode, clock output – USART0/SPI mode
P3.4/UTXD0	32	I/O	General digital I/O, transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General digital I/O, receive data in – USART0/UART mode
P3.6	34	I/O	General digital I/O
P3.7	35	I/O	General digital I/O
P4.0/TB0	36	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR0
P4.1/TB1	37	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR1
P4.2/TB2	38	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR2
P4.3	39	I/O	General-purpose digital I/O
P4.4	40	I/O	General-purpose digital I/O
P4.5	41	I/O	General-purpose digital I/O
P4.6	42	I/O	General-purpose digital I/O
P4.7/TBCLK	43	I/O	General-purpose digital I/O, input clock TBCLK – Timer_B7
P5.0	44	I/O	General-purpose digital I/O
P5.1	45	I/O	General-purpose digital I/O
P5.2	46	I/O	General-purpose digital I/O
P5.3	47	I/O	General-purpose digital I/O
P5.4/MCLK	48	I/O	General-purpose digital I/O, main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O, submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O, auxiliary clock ACLK output
P5.7/TBoutH	51	I/O	General-purpose digital I/O, switch all PWM digital output ports to high impedance – Timer_B7 TB0 to TB2
P6.0	59	I/O	General digital I/O
P6.1	60	I/O	General digital I/O
P6.2	61	I/O	General digital I/O
P6.3	2	I/O	General digital I/O
P6.4	3	I/O	General digital I/O
P6.5	4	I/O	General digital I/O
P6.6	5	I/O	General digital I/O
P6.7	6	I/O	General digital I/O
$\overline{\text{RST}}$/NMI	58	I	Reset input, nonmaskable interrupt input port
TCK	57	I	Test clock. TCK is the clock input port for device programming test.
TDI	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output
TMS	56	I	Test mode select. TMS is used as an input port for device test.
NC	7, 10, 11		No internal connection
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2

short-form description

processing unit

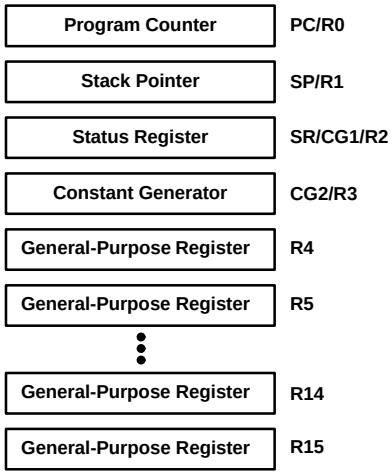
The processing unit is based on a consistent and orthogonal CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and notable for its ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

CPU

The CPU has sixteen registers that provide reduced instruction execution time. This reduces the register-to-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register, and constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus, and can be easily handled with all memory manipulation instructions.



instruction set

The instruction set for this register-to-register architecture constitutes a powerful and easy-to-use assembler language. The instruction set consists of 51 instructions with three formats and seven address modes. Table 1 provides a summary and example of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ——> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Each instruction operating on word and byte data is identified by the suffix B.

Examples:	**WORD INSTRUCTIONS**		**BYTE INSTRUCTIONS**	
	MOV	EDE, TONI	MOV.B	EDE,TONI
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

short-form description (continued)

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

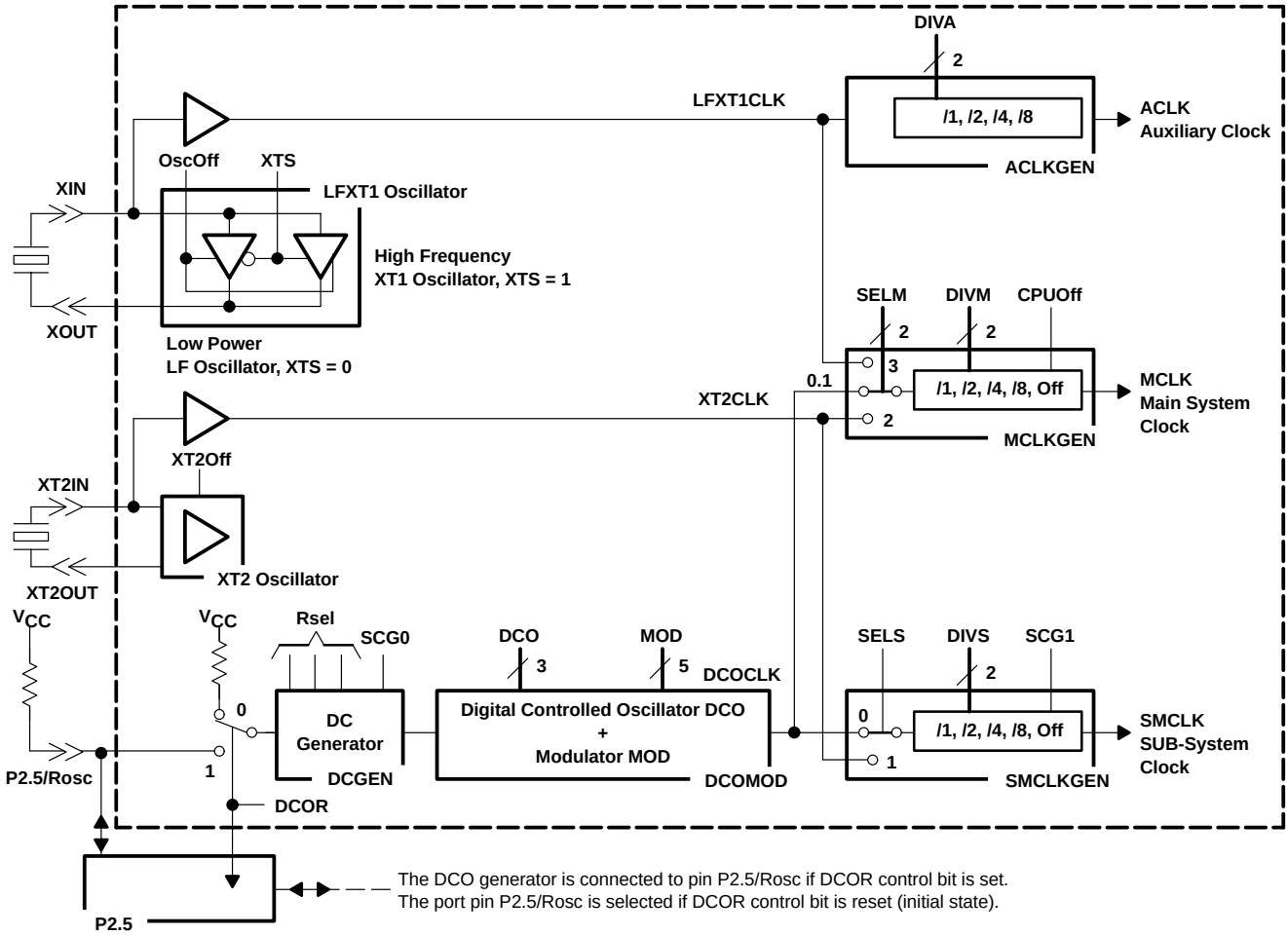
Computed branches (BR) and subroutine call (CALL) instructions use the same address modes as other instructions. These address modes provide *indirect* addressing, which is ideally suited for computed branches and calls. The full use of this programming capability results in a program structure which is different from structures used with conventional 8- and 16-bit controllers. For example, numerous routines can be easily designed to deal with pointers and stacks instead of using flag-type programs for flow control.

operating modes and interrupts

The MSP430 operating modes provide advanced support of the requirements for ultralow-power and ultralow-energy consumption. This goal is achieved by intelligent management during the different operating modes of modules and CPU states and is fully supported during interrupt event handling. An interrupt event awakes the system from each of the various operating modes and returns, using the *RETI* instruction, to the mode that was selected before the interrupt event occurred. The different requirements on CPU and modules—driven by system cost and current consumption objectives—require the use of different clock signals:

- Auxiliary clock ACLK, sourced by LFXT1CLK (crystal frequency) and used by the peripheral modules
- Main system clock MCLK, used by the CPU and system
- Subsystem clock SMCLK, used by the peripheral modules

operating modes and interrupts (continued)



Any of these clock sources—LFXT1CLK, XT2CLK, or DCOCLK—can be used to drive the MSP430 system.

LFXT1CLK is defined by connecting a low-power, low-frequency crystal to the oscillator, by connecting a high-frequency crystal to the oscillator, or by applying an external clock source. The high-frequency crystal oscillator is used if control bit XTS is set. The crystal oscillator may be switched off if LFXT1CLK is not required for the current operating mode.

XT2CLK is defined by connecting a high-frequency crystal to the oscillator or by applying an external clock source. Crystal oscillator XT2 may be switched off using the XT2Off control bit if not required by the current operating mode.

When DCOCLK is active, its frequency is selected or adjusted by software. DCOCLK is inactive or stopped when it is not being used by the CPU or peripheral modules. The dc generator can be stopped when SCG0 is reset and DCOCLK is not required. The dc generator determines the basic DCO frequency, and can be set by one external resistor or adjusted in eight steps by selection of integrated resistors.

NOTE:

The system clock generator always starts with DCOCLK selected as MCLK (CPU clock) to ensure proper start of program execution. The software determines the final system clock through control bit manipulation.

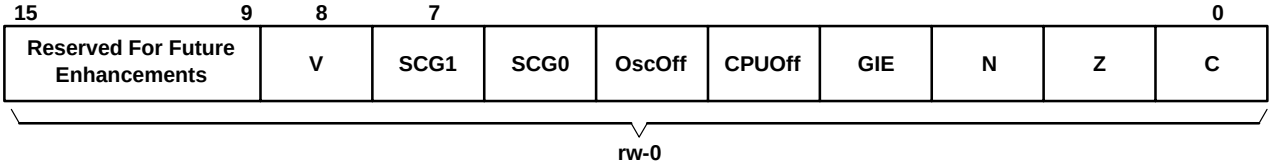
The system clock MCLK is also selected by hardware to be the DCOCLK (DCO and DCGEN are on) if the crystal oscillator (XT1 or XT2) fails while being selected as MCLK. Without this *forced clock mode* the NMI, requested by the oscillator fault flag, can not be handled and control may be lost. Without forced-clock mode the processor could not execute any code until the failed oscillator restarts.

low-power consumption capabilities

The various operating modes are handled by software by controlling the operation of the internal clock system. This clock system provides a large combination of hardware and software capabilities to run the application while maintaining the lowest power consumption and optimizing system costs. This is accomplished by:

- Use of the internal clock (DCO) generator without any external components
- Selection of an external crystal or ceramic resonator for lowest frequency and cost
- Selection and activation of the proper clock signals (LFXT1CLK, XT2Off, and/or DCOCLK) and clock predivider function. Control bit XT2Off is embedded in control register BCSCTL1.
- Application of an external clock source

The control bits that most influence the operation of the clock system and support fast turnon from low power operating modes are located in the status register SR. Four bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.



CPUOff, SCG1, SCG0, and OscOff are the most important bits in low-power control when the basic function of the system clock generator is established. They are pushed to the stack whenever an interrupt is accepted and saved for returning to the operation before an interrupt request. They can be manipulated via indirect access to the data on the stack during execution of an interrupt handler so that program execution can resume in another power operating mode after return-from-interrupt.

CPUOff: Clock signal MCLK, used with the CPU, is active when the CPUOff bit is reset or stopped when set.

SCG1: Clock signal SMCLK, used with peripherals, is enabled when the SCG1 bit is reset or stopped when set.

OscOff: Crystal oscillator LFXT1 is active when the OscOff bit is reset. The LFXT1 oscillator can be inactive only when the OscOff bit is set and it is not used for MCLK. The setup time to start a crystal oscillation requires special consideration when the off option is used. Mask-programmable devices can disable this feature and the oscillator can never be switched off by software.

SCG0: The dc generator is active when the SCG0 bit is reset. The DCO can be inactive only if the SCG0 bit is set and the DCOCLK signal is not used as MCLK or SMCLK. The dc current consumed by the dc generator defines the basic frequency of the DCOCLK.

When the current is switched off (SCG0=1) the start of the DCOCLK is slightly delayed. This delay is in the microsecond range.

DCOCLK: Clock signal DCOCLK is stopped if not used as MCLK or SMCLK. There are two situations when the SCG0 bit can not switch the DCOCLK signal off:

The DCOCLK frequency is used as MCLK (CPUOff=0 and SELM.1=0), or the DCOCLK frequency is used as SMCLK (SCG1=0 and SELS=0).

If DCOCLK is required for operation, the SCG0 bit can not switch the dc generator off.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog	WDTIFG (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator fault	NMIIFG (see Notes 1 & 4) OFIFG (see Notes 1 & 4)	(Non)maskable (Non)maskable	0FFFCh	14
Timer_B3	BCCIFG0 (see Note 2)	Maskable	0FFFAh	13
Timer_B3	BCCIFG1 to BCCIFG2 TBIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
			0FFEEh	7
Timer_A3	CCIFG0 (see Note 2)	Maskable	0FFECh	6
Timer_A3	CCIFG1, CCIFG2, TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 & 2) To P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 & 2) To P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
			0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
4. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h	UTXIE0	URXIE0		NMIIE			OFIE	WDTIE
	rw-0	rw-0		rw-0			rw-0	rw-0

WDTIE: Watchdog-timer-interrupt enable signal
OFIE: Oscillator-fault-interrupt enable signal
NMIIE: Nonmaskable-interrupt enable signal
URXIE0: USART0, UART, and SPI receive-interrupt enable signal
UTXIE0: USART0, UART, and SPI transmit-interrupt enable signal

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
	rw-1	rw-0		rw-0			rw-1	rw-0

WDTIFG: Set on overflow or security key violation or reset on VCC power-on or reset condition at $\overline{\text{RST}}$/NMI
OFIFG: Flag set on oscillator fault
NMIIFG: Set via $\overline{\text{RST}}$/NMI pin
URXIFG0: USART0, UART, and SPI receive flag
UTXIFG0: USART0, UART, and SPI transmit flag

Address	7	6	5	4	3	2	1	0
03h								

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h	UTXE0	URXE0 USPIE0						
	rw-0	rw-0						

URXE0: USART0, UART receive enable
UTXE0: USART0, UART transmit enable
USPIE0: USART0, SPI (synchronous peripheral interface) transmit and receive enable

Address	7	6	5	4	3	2	1	0
05h								

Legend: rw: **Bit Can Be Read and Written**
rw-0: **Bit Can Be Read and Written. It Is Reset by PUC.**
SFR Bit Not Present in Device

memory organization

		MSP430C1331	MSP430C1351
Memory Interrupt vector Code memory	Size ROM ROM	8kB 0FFFFh – 0FFE0h 0FFFFh – 0E000h	16kB 0FFFFh – 0FFE0h 0FFFFh – 0C000h
RAM	Size	256 Byte 02FFh – 0200h	512 Byte 03FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

nonmaskable interrupt scheme

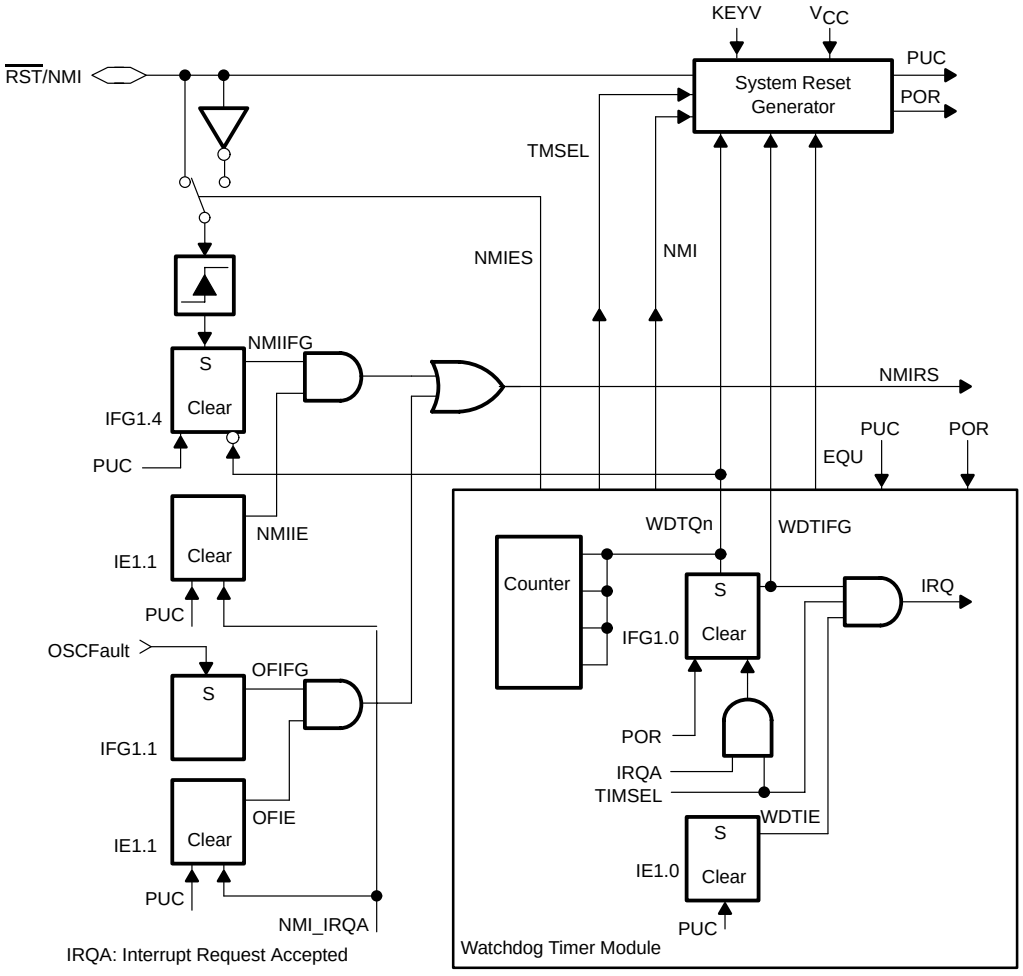


Figure 1. Block Diagram of NMI Interrupt Sources

One NMI vector is used for two NMI events: $\overline{\text{RST}}$/NMI (NMIIFG), and oscillator fault (OFIFG). The software can determine the source of the interrupt request, since both flags remain set until reset by software. The enable flag(s) should be set only within one instruction directly before the return-from-interrupt (RETI) instruction. This ensures that the stack remains under control. A pending NMI interrupt request will not increase stack demand unnecessarily.

peripherals

Peripherals are connected to the CPU through data, address, and control busses, and can be easily handled using all memory-manipulation instructions.

oscillator and system clock

Three clocks are used in the system—the main system (master) clock (MCLK) used by the CPU and the system, the subsystem (master) clock (SMCLK) used by the peripheral modules, and the auxiliary clock (ACLK) originated by LFXT1CLK (crystal frequency) and used by the peripheral modules.

Following a POR the DCOCLK is used by default, the DCOR bit is reset, and the DCO is set to the nominal initial frequency. Additionally, if either LFXT1CLK (with XT1 mode selected by XTS=1) or XT2CLK fails as the source for MCLK, DCOCLK is automatically selected to ensure fail-safe operation.

SMCLK can be generated from XT2CLK or DCOCLK. ACLK is always generated from LFXT1CLK.

Crystal oscillator LFXT1 can be defined to operate with watch crystals (32,768 Hz) or with higher-frequency ceramic resonators or crystals. The crystal or ceramic resonator is connected across two terminals. No external components are required for watch-crystal operation. If the high-frequency XT1 mode is selected, external capacitors from XIN to VSS and XOUT to VSS are required, as specified by the crystal manufacturer.

The LFXT1 oscillator starts after application of VCC. If the OscOff bit is set to 1, the oscillator stops when it is not used for MCLK.

Crystal oscillator XT2 is identical to oscillator LFXT1, but only operates with higher-frequency ceramic resonators or crystals. The crystal or ceramic resonator is connected across two terminals. External capacitors from XT2IN to VSS and XT2OUT to VSS are required as specified by the crystal manufacturer.

The XT2 oscillator is off after application of VCC, since the XT2 oscillator control bit XT2Off is set. If bit XT2Off is set to 1, the XT2 oscillator stops when it is not used for MCLK or SMCLK.

Clock signals ACLK , MCLK, and SMCLK may be used externally via port pins.

Different application requirements and system conditions dictate different system-clock requirements, including:

- High frequency for quick reaction to system hardware requests or events
- Low frequency to minimize current consumption, EMI, etc.
- Stable peripheral clock for timer applications, such as real-time clock (RTC)
- Start-stop operation that can be enabled with minimum delay

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6. Ports P1 and P2 use seven control registers, while ports P3, P4, P5, and P6 use only four of the control registers to provide maximum digital input/output flexibility to the application:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- Read/write access to all registers using all instructions is possible.

digital I/O (continued)

The seven control registers are:

- Input register — 8 bits at ports P1 through P6
- Output register — 8 bits at ports P1 through P6
- Direction register — 8 bits at ports P1 through P6
- Interrupt edge select — 8 bits at ports P1 and P2
- Interrupt flags — 8 bits at ports P1 and P2
- Interrupt enable — 8 bits at ports P1 and P2
- Selection (port or module) — 8 bits at ports P1 through P6

Each one of these registers contains eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on ports P1.0 to P1.7, and another commonly used for any interrupt event on ports P2.0 to P2.7.

Ports P3, P4, P5, and P6 have no interrupt capability.

Watchdog Timer

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. A system reset is generated if the selected time interval expires. If an application does not require this watchdog function, the module can work as an interval timer, which generates an interrupt after a selected time interval.

The Watchdog Timer counter (WDTCNT) is a 15/16-bit up-counter not directly accessible by software. The WDTCNT is controlled using the Watchdog Timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL in either operating mode (watchdog or timer) is only possible when using the correct password (05Ah) in the high-byte. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. The password is read as 069h to minimize accidental write operations to the WDTCTL register. The low-byte stores data written to the WDTCTL. In addition to the Watchdog Timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

USART0

The universal synchronous/asynchronous interface is a dedicated peripheral module used in serial communications. The USART supports synchronous SPI (3- or 4-pin), and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Data streams of 7 or 8 bits in length can be transferred at a rate determined by the program, or by an external clock. Low-power applications are optimized by UART mode options which allow for the reception of only the first byte of a complete frame. The application software should then decide if the succeeding data is to be processed. This option reduces power consumption.

Two dedicated interrupt vectors are assigned to the USART module—one for the receive and one for the transmit channels.

timer_A (three capture/compare registers)

The timer module offers one sixteen-bit counter and three capture/compare registers. The timer clock source can be selected from two external sources P1.0/TACLK (SSEL=0) or P2.1/TAINCLK (SSEL=3), or from two internal sources—ACLK (SSEL=1) or SMCLK (SSEL=2). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode)—it can be halted, read, and written; it can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The three capture/compare blocks are configured by the application to run in capture or compare mode.

The capture mode is mostly used to individually measure internal or external events from any combination of positive, negative, or positive and negative edges. It can also be stopped by software. Three different external events can be selected: TA0, TA1, and TA2. In the capture/compare register CCR2, ACLK is the capture signal if CCI2B is selected. Software capture is chosen if CCISx=2 or CCISx=3.

The compare mode is mostly used to generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes like D/A conversion functions or motor control. An individual output module is assigned to each of the three capture/compare registers. This module can run independently of the compare function or can be triggered in several ways.

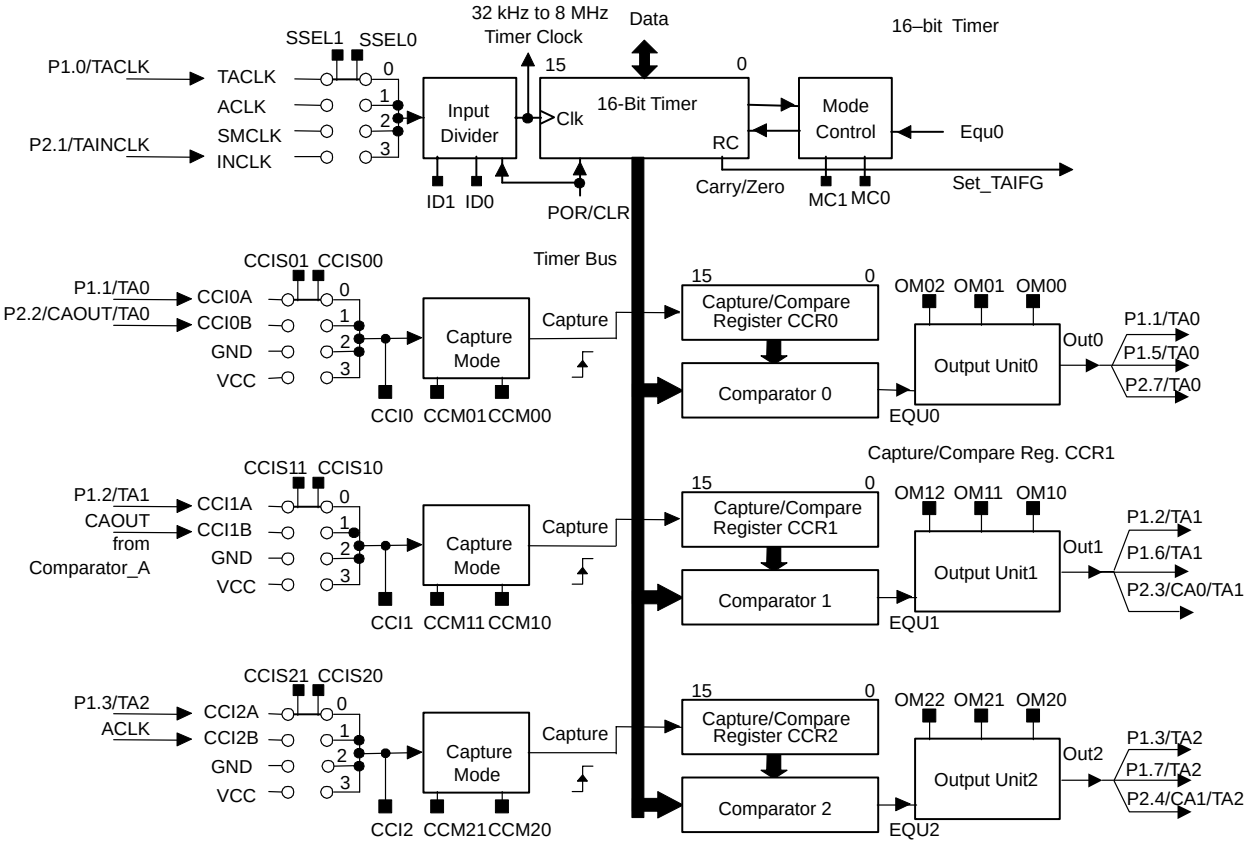


Figure 2. Timer_A, MSP430C13x1 Configuration

Two interrupt vectors are used by the module. One vector is assigned to capture/compare block CCR0, and one common-interrupt vector is implemented for the timer and the other two capture/compare blocks. The three interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter so that the interrupt handler software continues at the corresponding program location. This simplifies the interrupt handler and assigns each interrupt event the same five-cycle overhead.

timer_B (three capture/compare registers)

Timer_B3 is identical to Timer_A3, except for the following:

- The timer counter can be configured to operate in 8-, 10-, 12-, or 16-bit mode.
- The function of the capture/compare registers is slightly different when in compare mode. In Timer_B, the compare data is written to the capture/compare register, but is then transferred to the associated compare latch for the comparison.
- All output level Outx can be set to Hi-Z from the TboutH external signal.
- The SCCI bit is not implemented in Timer_B

The timer module has one sixteen-bit counter and three capture/compare registers. The timer clock source can be selected from an external source TBCLK (SSEL=0 or 3), or from two internal sources: ACLK (SSEL=1) and SMCLK (SSEL=2). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode): it can be halted, read, and written; it can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The seven capture/compare blocks are configured by the application to run in capture or in compare mode.

The capture mode is mostly used to measure external or internal events from any combination of positive, negative, or positive and negative edges. It can also be stopped by software. Any of three different external events TB0 to TB2 can be selected. In the capture/compare register CCR2, ACLK is the capture signal if CCI2B is selected. Software capture is chosen if CCISx=2 or CCISx=3.

The compare mode is mostly used to generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes such as D/A conversion functions or motor control. An individual output module is assigned to each of the seven capture/compare registers. This module can run independently of the compare function, or can be triggered in several ways. The comparison is made from the data in the compare latches (TBCLx) and not from the compare register.

Two interrupt vectors are used by the module. One vector is assigned to capture/compare block CCR0, and one common interrupt vector is implemented for the timer and the other two capture/compare blocks. The three interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter so that the interrupt handler software continues at the corresponding program location. This simplifies the interrupt handler and assigns each interrupt event the same five-cycle overhead.

compare latches (TBCLx)

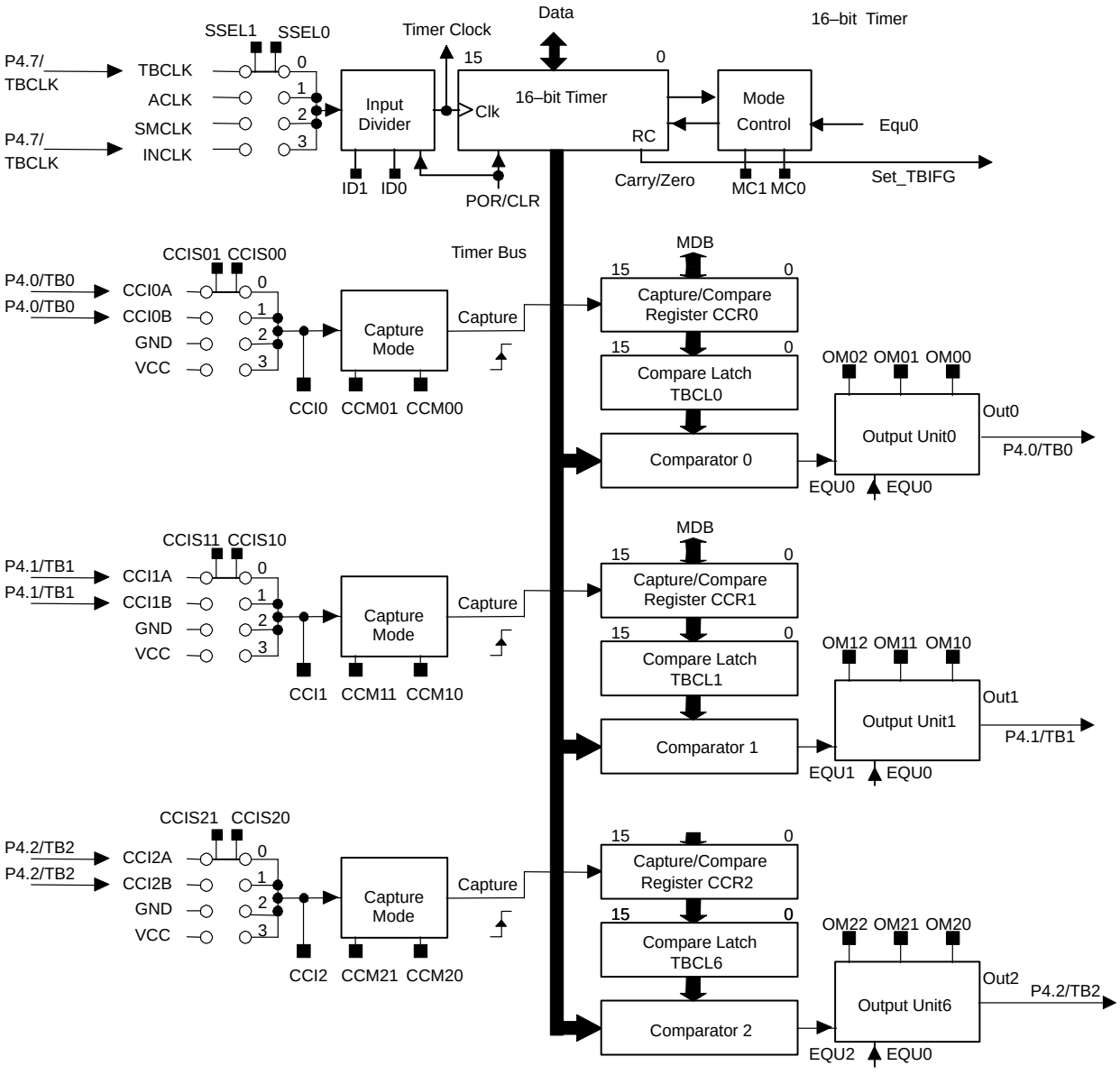
The compare latches can be loaded directly by software or via selected conditions triggered by the PWM function. They are reset by the POR signal.

Load TBCLx immediate, CLLD=0:	Capture/compare register CCRx and the corresponding compare latch are loaded simultaneously.
Load TBCLx at Zero, CLLD=1:	The data in capture/compare register CCRx is loaded to the corresponding compare latch when the 16-bit timer TBR counts to zero.
Load TBCLx at Zero + Period, CLLD=2:	The data in capture/compare register CCRx is loaded to the corresponding compare latch when the 16-bit timer TBR counts to zero or when the next period starts (in UP/DOWN mode).
Load TBCLx at EQUx, CLLD=3:	The data in capture/compare register CCRx is loaded when CCRx is equal to TBR.

compare latches (TBCLx) (continued)

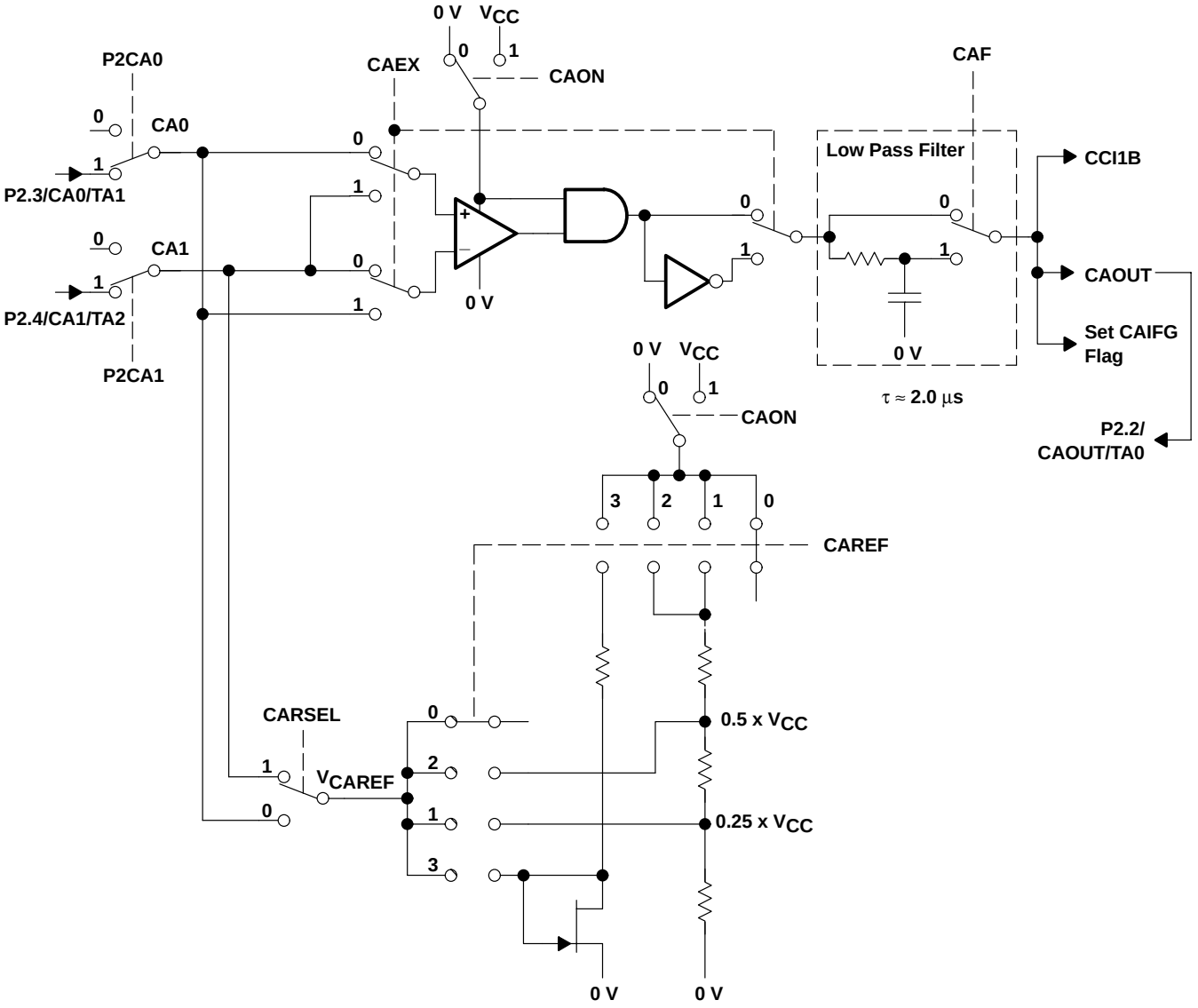
Loading the compare latches can be done individually or in groups. Individually means that whenever the selected load condition (see above) is true, the CCRx data is loaded into TBCLx.

Load TBCLx individually, TBCLGRP=0:	Compare latch TBCLx is loaded when the selected load condition (CLLD) is true.
Dual load TBCLx mode, TBCLGRP=1 or 2:	The compare latches TBCL1 and TBCL2 are loaded when data are written to both CCR1 and CCR2 registers and the load condition (CLLD) is true.
Full load TBCLx mode, TBCLGRP=3:	All three compare latches TBCLx are loaded when data are written to all three CCRx registers and then the selected load condition (CLLD) is true. All CCRx data, CCR0+CCR1+CCR2, are simultaneously loaded to the corresponding SHRx compare latches.



comparator_A

The primary functions of the comparator module are support of precision slope conversion in A/D applications, battery voltage supervision, and external analog signal monitoring. The comparator is connected to port pins P2.3 (+ terminal) and to P2.4 (–terminal). It is controlled via eight control bits in the CACTL register.



comparator_A

The control bits are:

CAOUT,	05Ah, bit0	Comparator output
CAF,	05Ah, bit1	The comparator output is transparent or fed through a small filter
P2CA0,	05Ah, bit2	0: Pin P2.3/CA0/TA1 is not connected to Comparator_A. 1: Pin P2.3/CA0/TA1 is connected to Comparator_A.
P2CA1,	05Ah, bit3	0: Pin P2.4/CA1/TA2 is not connected to Comparator_A. 1: Pin P2.4/CA1/TA2 is connected to Comparator_A.
CACTL2.4 to CATCTL2.7	05Ah, bit4 to 05Ah, bit7	Bits are implemented but do not control any hardware in this device.
CAIFG,	059h, bit0	Comparator_A interrupt flag
CAIE,	059h, bit1	Comparator_A interrupt enable
CAIES,	059h, bit2	Comparator_A interrupt edge select bit 0: The rising edge sets the Comparator_A interrupt flag CAIFG 1: The falling edge set the Comparator_A interrupt flag CAIFG
CAON,	059h, bit3	The comparator is switched on.
CAREF,	059h, bit4,5	Comparator_A reference 0: Internal reference is switched off, an external reference can be applied. 1: 0.25 × VCC reference selected. 2: 0.50 × VCC reference selected. 3: A diode reference selected.
CARSEL,	059h, bit6	An internal reference V_{CAREF}, selected by CAREF bits, can be applied to signal path CA0 or CA1. The signal V_{CAREF} is only driven by a voltage source if the value of CAREF control bits is 1, 2, or 3.
CAEX,	059h, bit7	The comparator inputs are exchanged, used to measure and compensate the offset of the comparator.

Eight additional bits are implemented into the Comparator_A module. They enable the software to switch off the input buffer of Port P2. A CMOS input buffer can dissipate supply current when the input is not near V_{SS} or V_{CC}. Control bits CAPI0 to CAIP7 are initially reset and the port input buffer is active. The port input buffer is inactive if the corresponding control bit is set.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_B3	Timer_B interrupt vector	TBIV	011Eh
	Timer_B control	TBCTL	0180h
	Capture/compare control 0	CCTL0	0182h
	Capture/compare control 1	CCTL1	0184h
	Capture/compare control 2	CCTL2	0186h
	Reserved		0188h
	Reserved		018Ah
	Reserved		018Ch
	Reserved		018Eh
	Timer_B register	TBR	0190h
	Capture/compare register 0	CCR0	0192h
	Capture/compare register 1	CCR1	0194h
	Capture/compare register 2	CCR2	0196h
	Reserved		0198h
	Reserved		019Ah
	Reserved		019Ch
	Reserved		019Eh
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Capture/compare control 0	CCTL0	0162h
	Capture/compare control 1	CCTL1	0164h
	Capture/compare control 2	CCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A register	TAR	0170h
	Capture/compare register 0	CCR0	0172h
	Capture/compare register 1	CCR1	0174h
	Capture/compare register 2	CCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
PERIPHERALS WITH BYTE ACCESS			
UART0	Transmit buffer	UTXBUF.0	077h
	Receive buffer	URXBUF.0	076h
	Baud rate	UBR1.0	075h
	Baud rate	UBR0.0	074h
	Modulation control	UMCTL.0	073h
	Receive control	URCTL.0	072h
	Transmit control	UTCTL.0	071h
	UART control	UCTL.0	070h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
Comparator_A	Comp._A port disable	CAPD	05Bh
	Comp._A control2	CACTL2	05Ah
	Comp._A control1	CACTL1	059h
System Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to + 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature (programmed device) . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}.

PARAMETER			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			1.8		3.6	V
Supply voltage, V_{SS}			0.0		0.0	V
Operating free-air temperature range, T_A			–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 5 and 6)	LF selected, XTS=0	Watch crystal		32768		Hz
	XT1 selected, XTS=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
Low-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IL} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS} +0.6	V
High-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IH} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	0.8×V_{CC}		V_{CC}	V
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V	V_{SS}		0.2×V_{SS}	V
	$V_{IH(Xin, Xout)}$		0.8×V_{CC}		V_{CC}	

NOTES: 5. In LF mode, the LFXT1 oscillator requires a watch crystal and the LFXT1 oscillator requires a 5.1-MΩ resistor from XOUT to VSS when VCC < 2.5 V. In XT1 mode, the LFXT1. and XT2 oscillators accept a ceramic resonator or a 4-MHz crystal frequency at $V_{CC} \geq$ 2.2 V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or an 8-MHz crystal frequency at $V_{CC} \geq$ 2.8 V.
6. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, FXT1 accepts a ceramic resonator or a crystal.

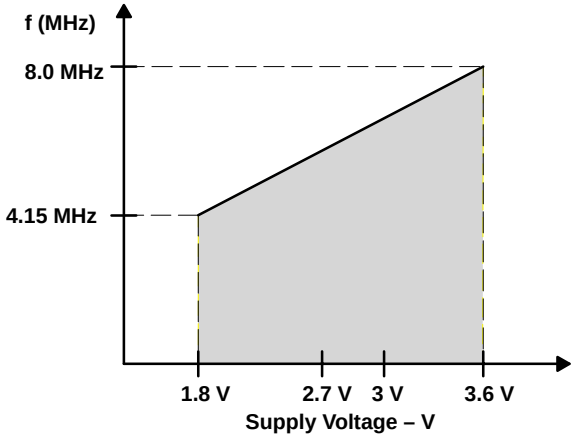


Figure 3. Frequency vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current, $f_{(System)}$ = 1 MHz

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 7) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS=0, SELM=(0,1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		160	200	µA
			V_{CC} = 3 V		240	300	
	Active mode, (see Note 7) $f_{(MCLK)} = f_{(SMCLK)}$ = 4 096 Hz, $f_{(ACLK)}$ = 4,096 Hz XTS=0, SELM=(0,1), XTS=0, SELM=3	T_A = –40°C to 85°C	V_{CC} = 2.2 V		2.5	7	µA
			V_{CC} = 3 V		2.5	7	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 7)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	45	µA
			V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2), $f_{(MCLK)}$ = f (SMCLK) = 0 MHz, f(ACLK) = 32.768 Hz, SCG0 = 0	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 8)	T_A = –40°C	V_{CC} = 2.2 V		0.8	1.5	µA
		T_A = 25°C			0.9	1.5	
		T_A = 85°C			1.6	2.8	
		T_A = –40°C	V_{CC} = 3 V		1.8	2.2	µA
		T_A = 25°C			1.8	2.2	
		T_A = 85°C			2.3	3.9	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	T_A = –40°C	V_{CC} = 2.2 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 85°C			0.8	2.5	
		T_A = –40°C	V_{CC} = 3 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 85°C			0.8	2.5	

NOTES: 7. Timer_B is clocked by f(DCOCLK) = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
8. Timer_B is clocked by f(ACLK) = 32,768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency

$$I(AM) = I(AM)\ [1\ MHz] \times f(System)\ [MHz]$$

Current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

SCHMITT-trigger inputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.90		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.4		1	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

standard inputs – $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 9	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 10	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 9	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 10	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 9	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 10	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 9	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 10	V_{SS}		V_{SS}+0.6	

NOTES: 9. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.

10. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

outputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

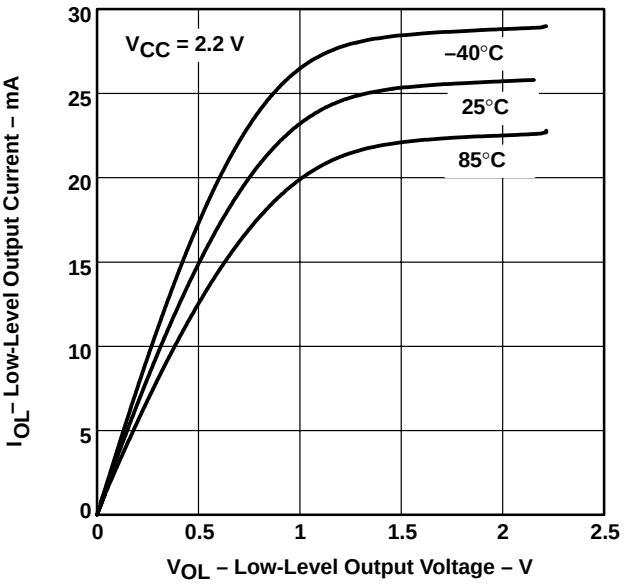


Figure 4

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

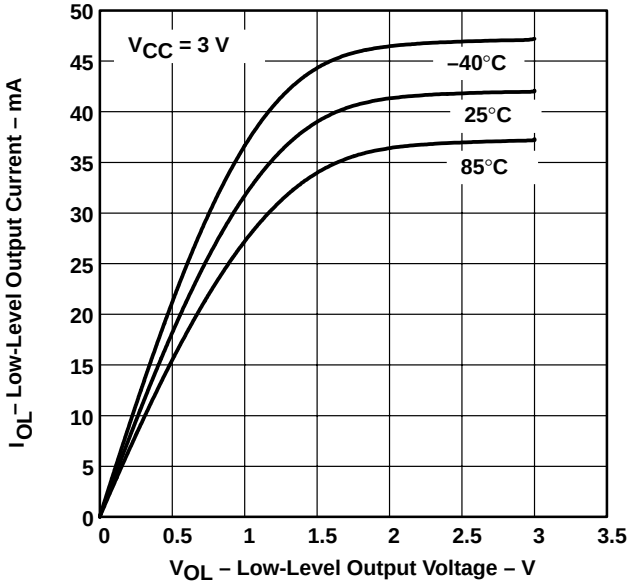


Figure 5

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

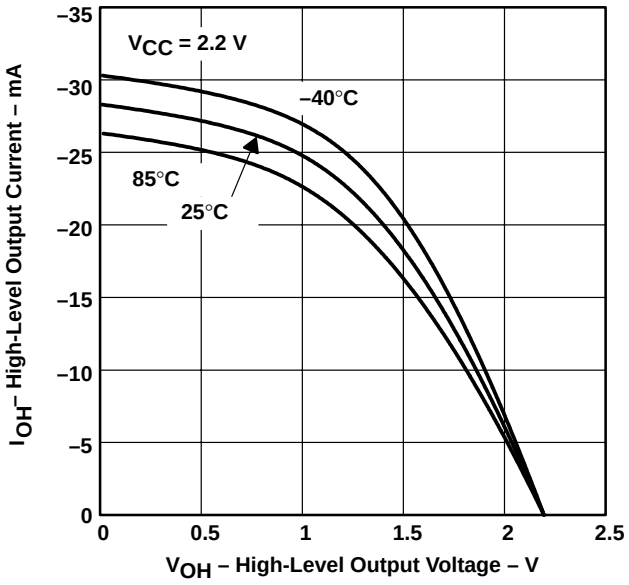


Figure 6

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

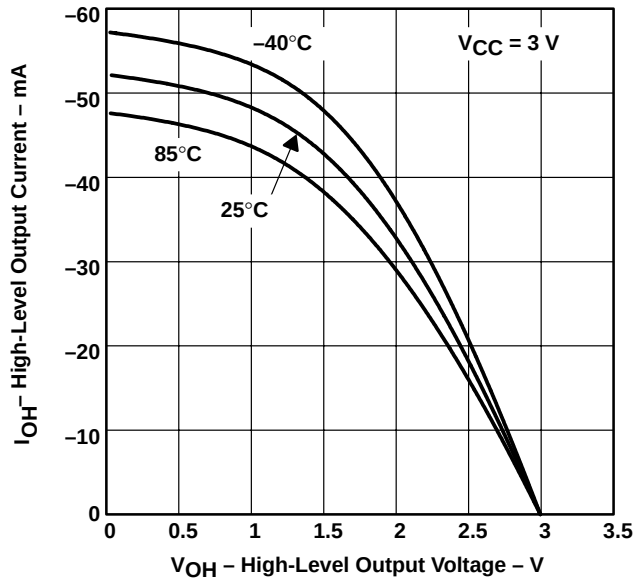


Figure 7

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

input frequency – Ports P1, P2, P3, P4, P5, and P6

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(IN)}$	$t_{(h)} = t_{(L)}$	V_{CC} = 2.2 V			8	MHz
		V_{CC} = 3 V			10	

capture timing _ Timer_A3: TA0, TA1, TA2; Timer_B3: TB0, TB1, TB2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P2, P4: External trigger signal for the interrupt flag (see Notes 11 and 12)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 11. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
12. The external signal needs additional timing because of the maximum input-frequency constraint.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{TAx}, f_{TBx}	TA0..2, TB0..2 Internal clock source, SMCLK signal applied (see Note 13)	C_L = 20 pF		DC		f_{System}	MHz
f_{ACLK}, f_{MCLK}, f_{SMCLK}	P5.6/ACLK, P5.4/MCLK, P5.5/SMCLK	C_L = 20 pF				f_{System}	
t_{Xdc}	Duty cycle of output frequency	P2.0/ACLK C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		P1.4/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$	35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$	50%– 15 ns	50%	50%– 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	50%– 15 ns	50%	50%– 15 ns	

NOTE 13: The limits of the system clock MCLK has to be met; the system (MCLK) frequency should not exceed the limits. MCLK and SMCLK frequencies can be different.

external interrupt timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P1, P2: External trigger signal for the interrupt flag (see Notes 14 and 15)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 14. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
15. The external signal needs additional timing because of the maximum input-frequency constraint.

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

leakage current (see Note 16)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$ (see Note 17)	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P2.x)}$		Port P2	Port 2: $V_{(P2.3)}$ $V_{(P2.4)}$ (see Note 17)				±50	

NOTES: 16. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
17. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU HALTED (see Note 26)	1.6			V

NOTE 18: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

Comparator_A (see Note 19)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		30	47	µA
			V_{CC} = 3 V		55	74	
$I_{(Refladder/Refdiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		40	57	µA
			V_{CC} = 3 V		60	87	
$V_{(IC)}$	Common-mode input voltage	CAON =1	V_{CC} = 2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$ See Figure 8	$\frac{\text{Voltage at 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, See Figure 8	V_{CC} = 2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$ See Figure 8	$\frac{\text{Voltage at 0.5}V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, See Figure 8	V_{CC} = 2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 20	V_{CC} = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	V_{CC} = 2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 19. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
20. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

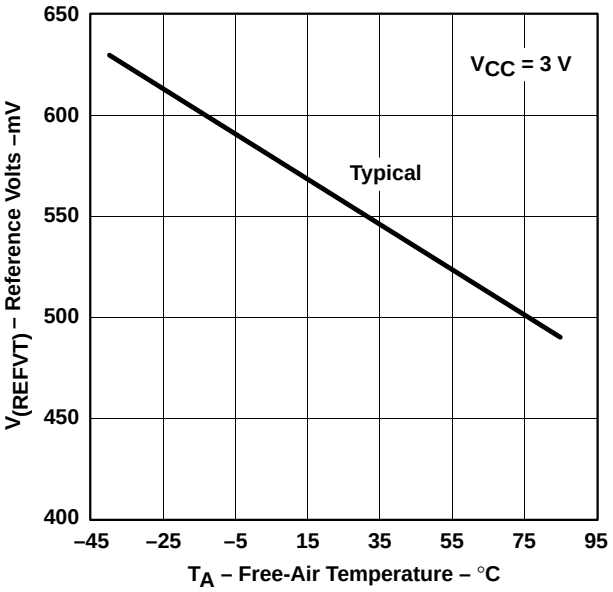


Figure 8. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

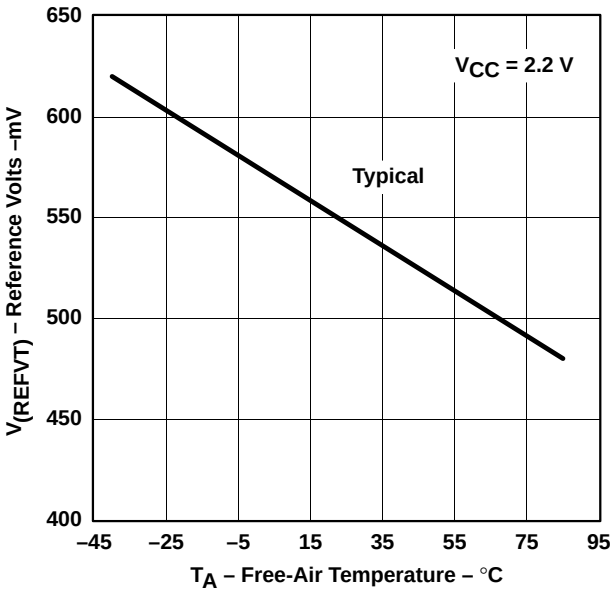


Figure 9. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

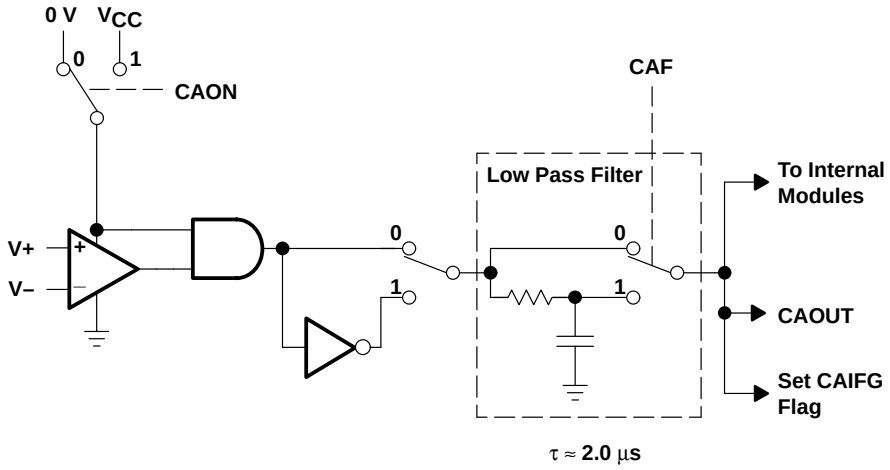


Figure 10. Block Diagram of Comparator_A Module

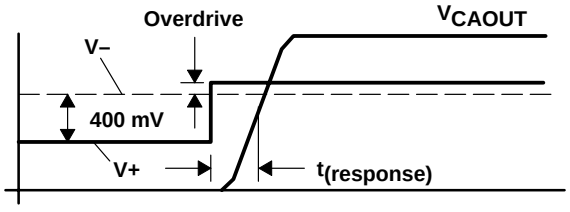


Figure 11. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR

PARAMETER		CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$t_{(POR)}$ Delay	POR		2.2 V/3 V		150	250	µs
$V_{(POR)}$		T_A = –40°C		1.4		1.8	V
$V_{(POR)}$		T_A = +25°C		1.1		1.5	V
$V_{(POR)}$		T_A = +85°C		0.8		1.2	V
$V_{(min)}$				0		0.4	V
$t_{(Reset)}$	PUC/POR	Reset is accepted internally	2.2 V/3 V	2			µs

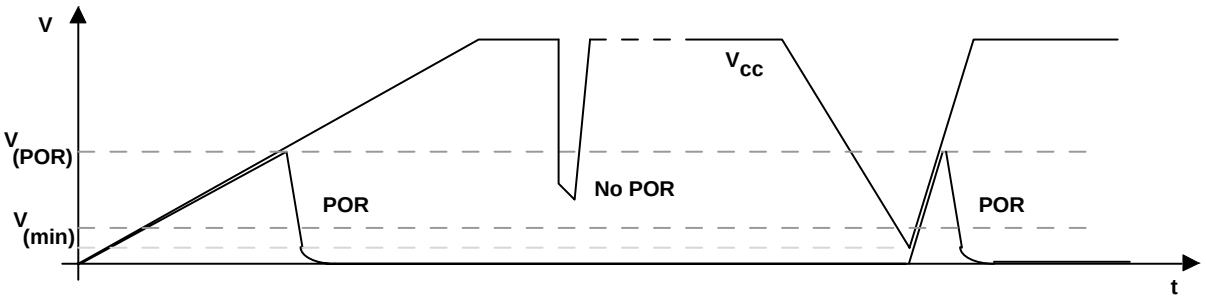


Figure 12. Power-On Reset (POR) vs Supply Voltage

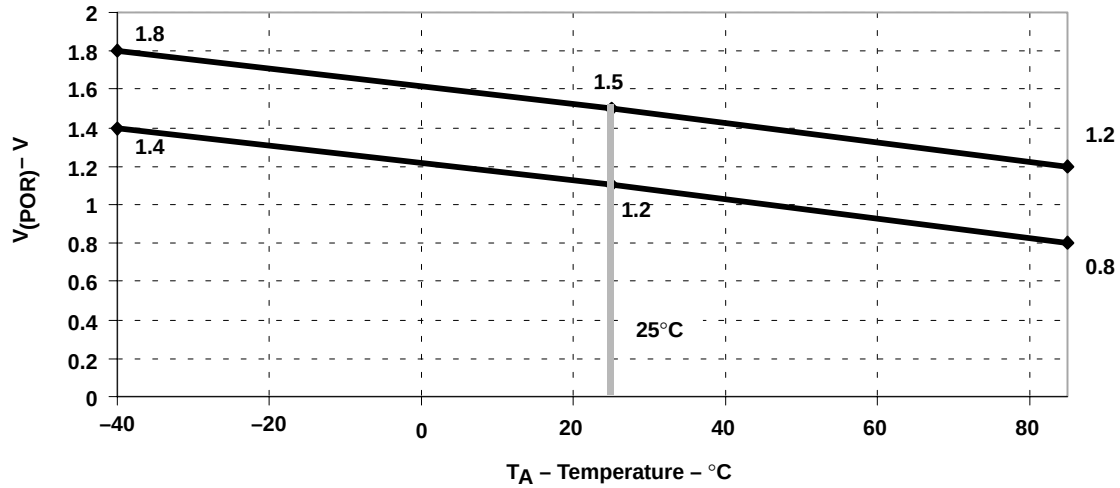


Figure 13. V(POR) vs Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO (see Note 21)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.90	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2.0	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	$f_{DCO40} \times 1.7$	$f_{DCO40} \times 2.1$	$f_{DCO40} \times 2.5$	MHz
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
$S_{(Rsel)}$	$S_R = f_{Rsel+1} / f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1} / f_{DCO}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 22)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 22)	V_{CC} = 2.2 V/3 V	0	5	10	%/V

NOTES: 21. The DCO frequency may not exceed the maximum system frequency defined by parameter processor frequency, $f_{(System)}$.
22. This parameter is not production tested.

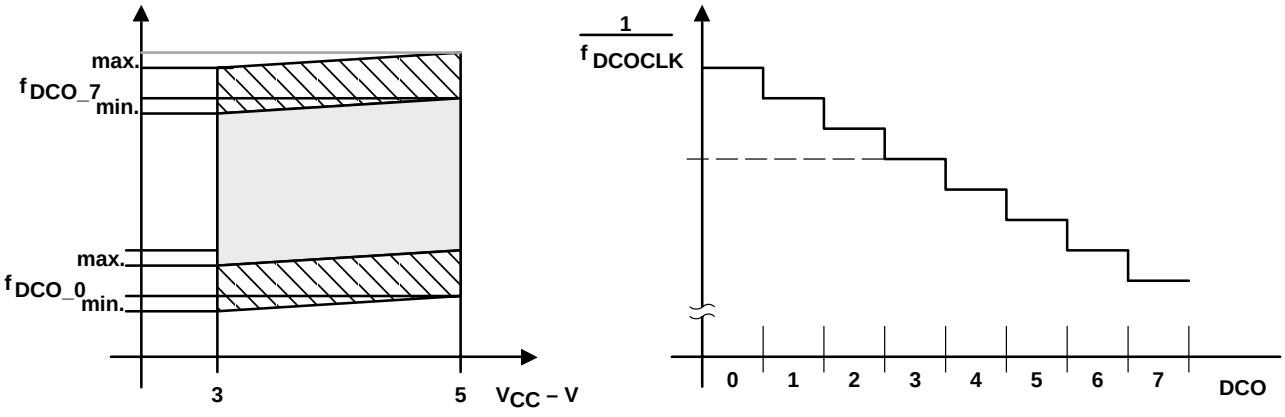


Figure 14. DCO Characteristics

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for f_{DCOx0} to f_{DCOx7} are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps with Rsel1, ... Rsel6 overlaps with Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to $f_{(DCO)} \times (2^{MOD/32})$.

crystal oscillator, LFXT1 oscillator (see Note 23)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	XTS=0; LF oscillator selected V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected V_{CC} = 2.2 V/3 V		2		
X_{COUT}	Integrated output capacitance	XTS=0; LF oscillator selected V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected V_{CC} = 2.2 V/3 V		2		
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 23: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

crystal oscillator, XT2 oscillator (see Note 24)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{COUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 24: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

USART0 (see Note 25)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 25: The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(t)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(t)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

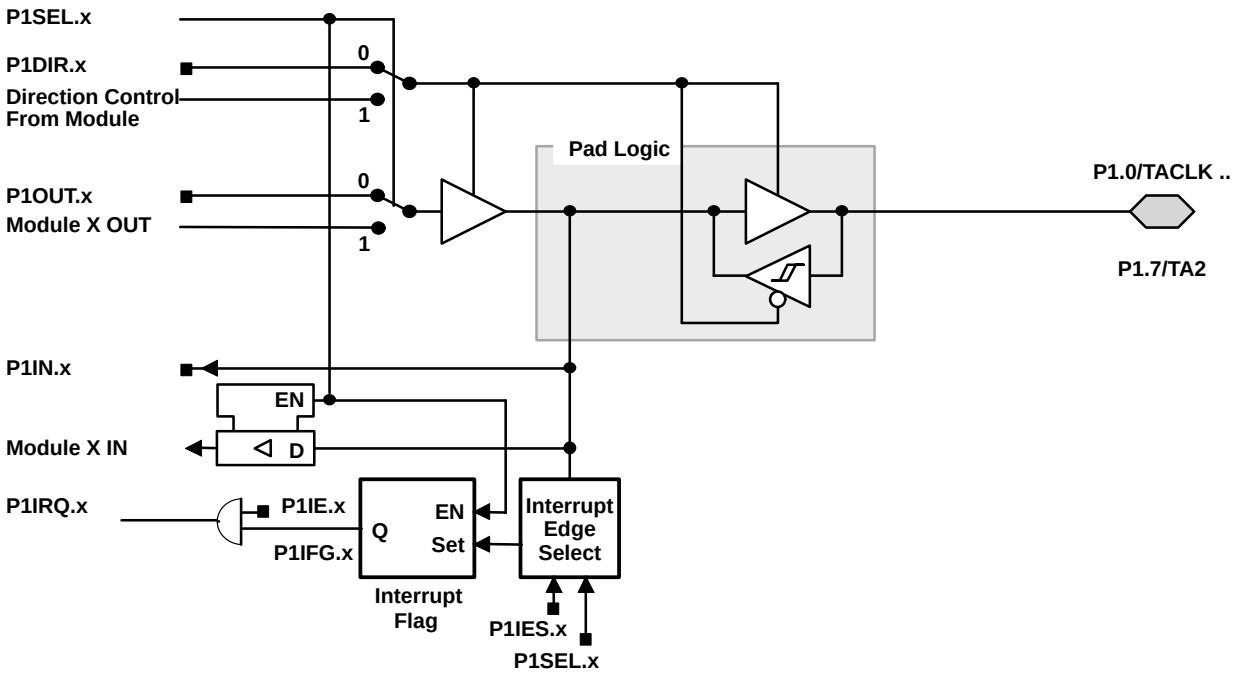
JTAG, fuse

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/test	TCK frequency	2.2 V	DC		5	MHz
			3 V	DC		10	
		Pullup resistors on TMS, TCK, TDI (see Note 26)	2.2 V/ 3V	25	60	90	kΩ
V_{FB}	JTAG/fuse (see Note 27)	Fuse-blow voltage (see Note 28)	3.6	5		5.5	V
I_{FB}		Supply current on TDI with fuse blown				100	mA
		Time to blow the fuse				20	ms

NOTES: 26. TMS, TDI, and TCK pull-up resistors are implemented in all F versions.
27. Once the fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
28. The supply voltage to blow the fuse is applied to the TDI pin.

input/output schematic

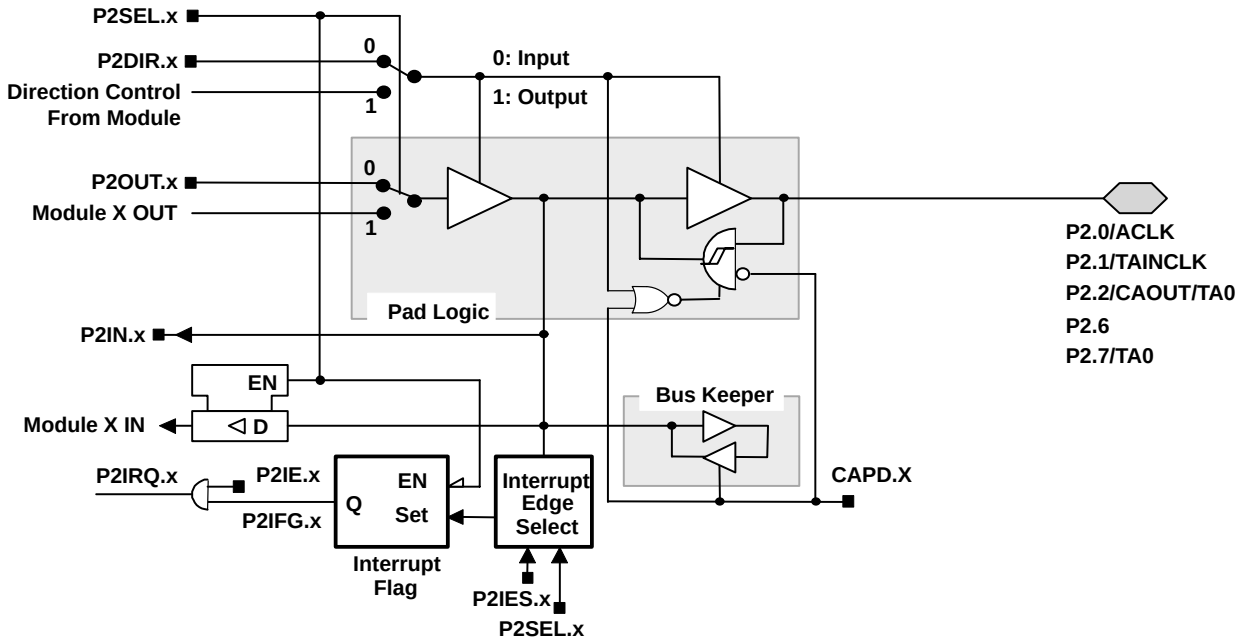
port P1, P1.0 to P1.7, input/output with Schmitt-trigger



PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DV_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

port P2, P2.0 to P2.2, P2.6, and P2.7 input/output with Schmitt-trigger



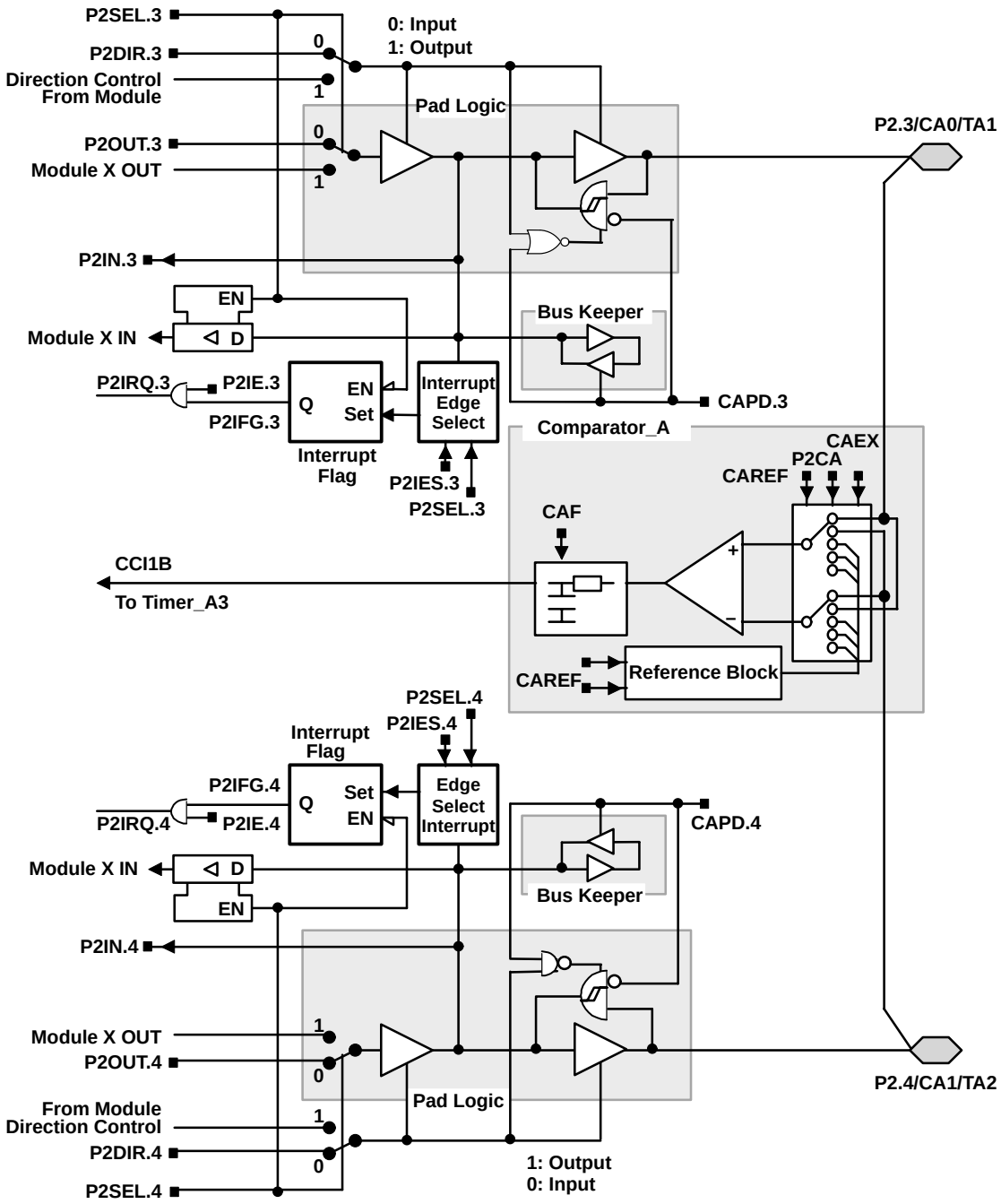
x: Bit Identifier 0 to 2, 6, and 7 for Port P2

PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV_{SS}	P2IN.1	INCLK‡	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT†	P2IN.2	CCI0B‡	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	DV_{SS}	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

† Signal from Comparator_A
‡ Signal to Timer_A
§ Signal from Timer_A

input/output schematic (continued)

port P2, P2.3 to P2.4, input/output with Schmitt-trigger

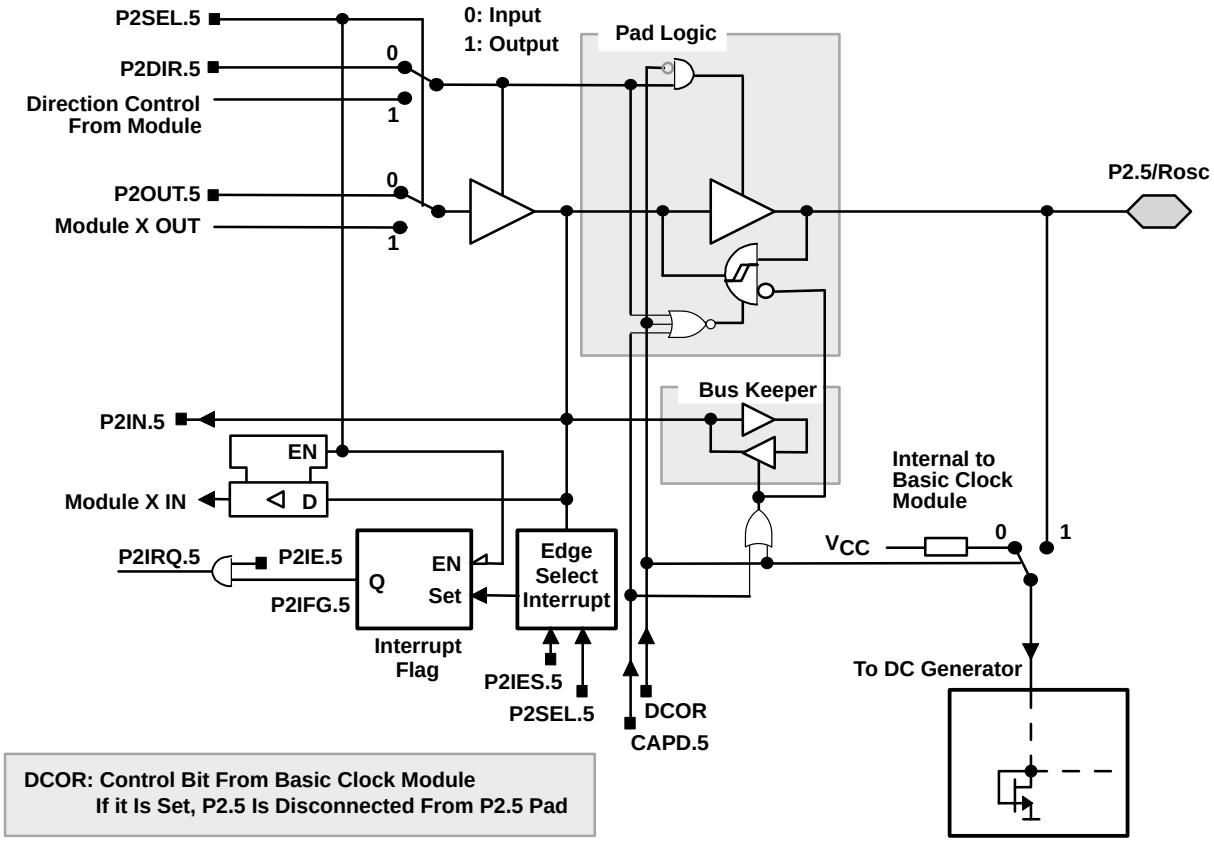


PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

† Signal from Timer_A

input/output schematic (continued)

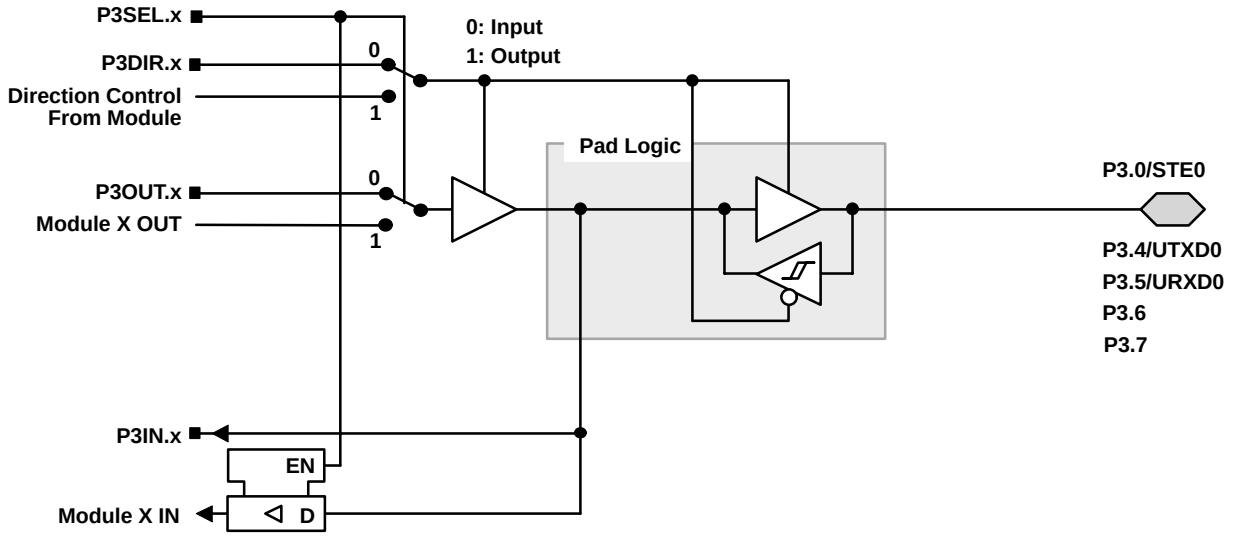
port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the basic clock module



PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

input/output schematic (continued)

port P3, P3.0 and P3.4 to P3.7, input/output with Schmitt-trigger

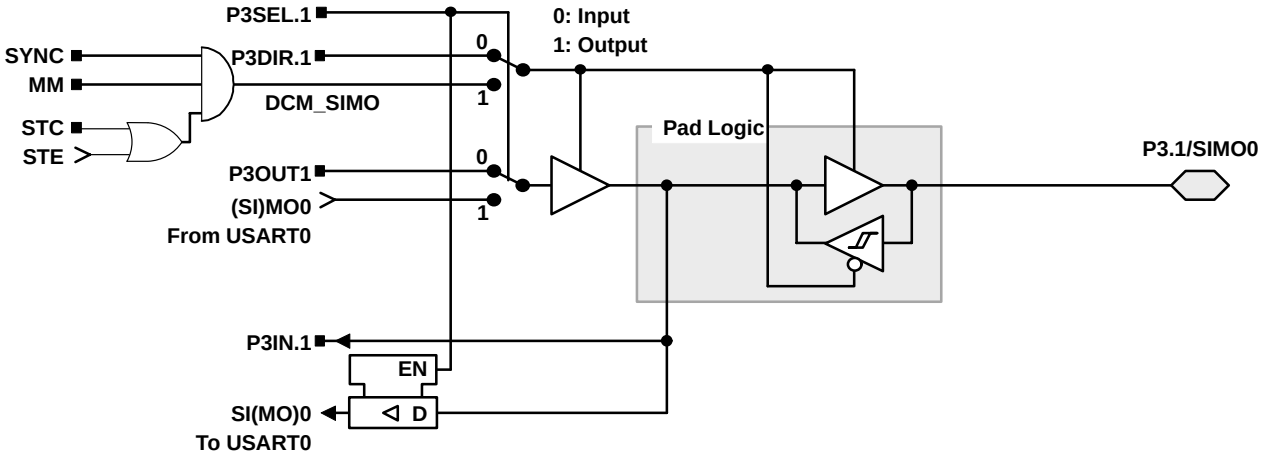


x: Bit Identifier, 0 and 4 to 7 for Port P3

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV_{CC}	P3OUT.4	UTXD0†	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV_{SS}	P3OUT.5	DV_{SS}	P3IN.5	URXD0‡
P3Sel.6	P3DIR.6	DV_{CC}	P3OUT.6	DV_{SS}	P3IN.6	Unused
P3Sel.7	P3DIR.7	DV_{SS}	P3OUT.7	DV_{SS}	P3IN.7	Unused

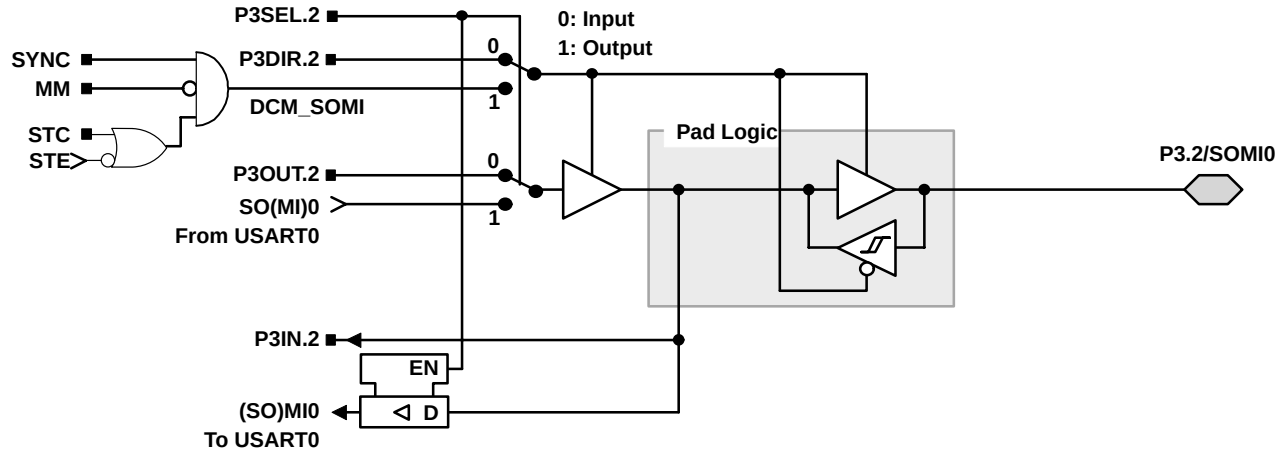
† Output from USART0 module
‡ Input to USART0 module

port P3, P3.1, input/output with Schmitt-trigger

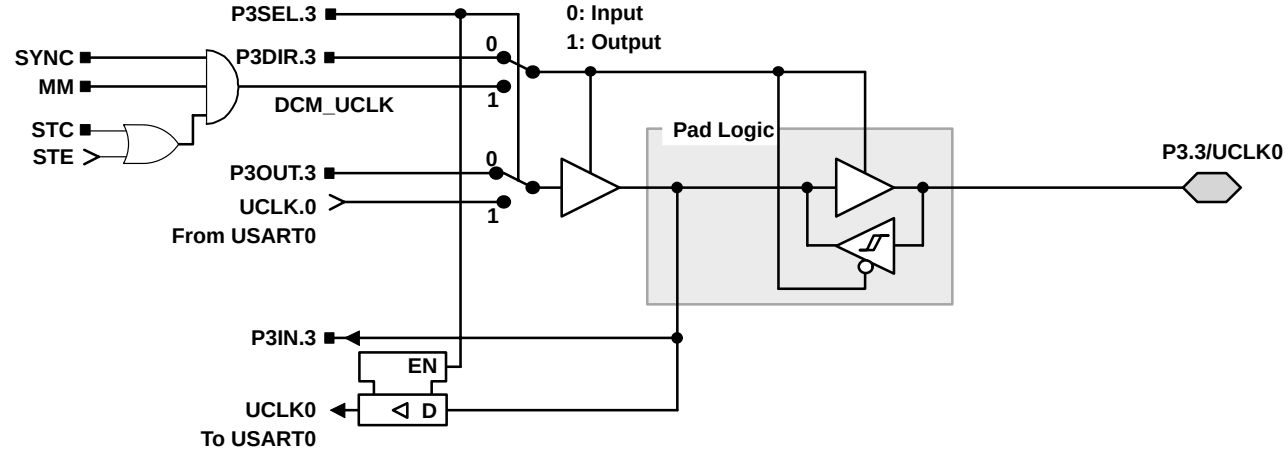


input/output schematic (continued)

port P3, P3.2, input/output with Schmitt-trigger



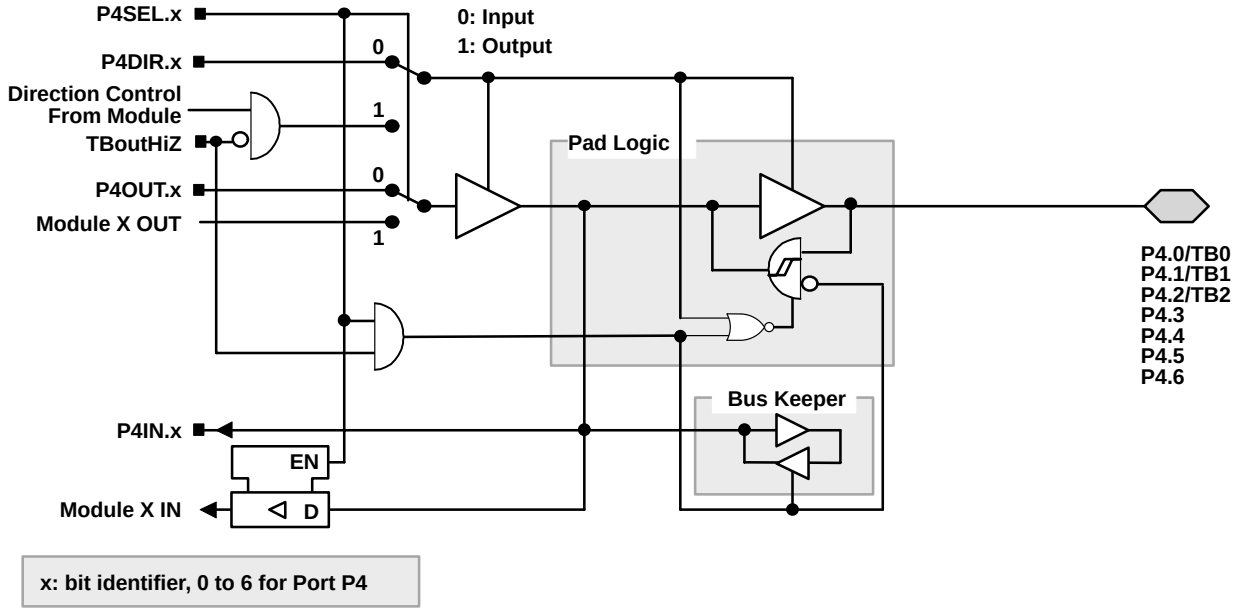
port P3, P3.3, input/output with Schmitt-trigger



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.
SPI, slave mode: The clock applied to UCLK0 is used to shift data in and out.
SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

input/output schematic (continued)

port P4, P4.0 to P4.6, input/output with Schmitt-trigger



x: bit identifier, 0 to 6 for Port P4

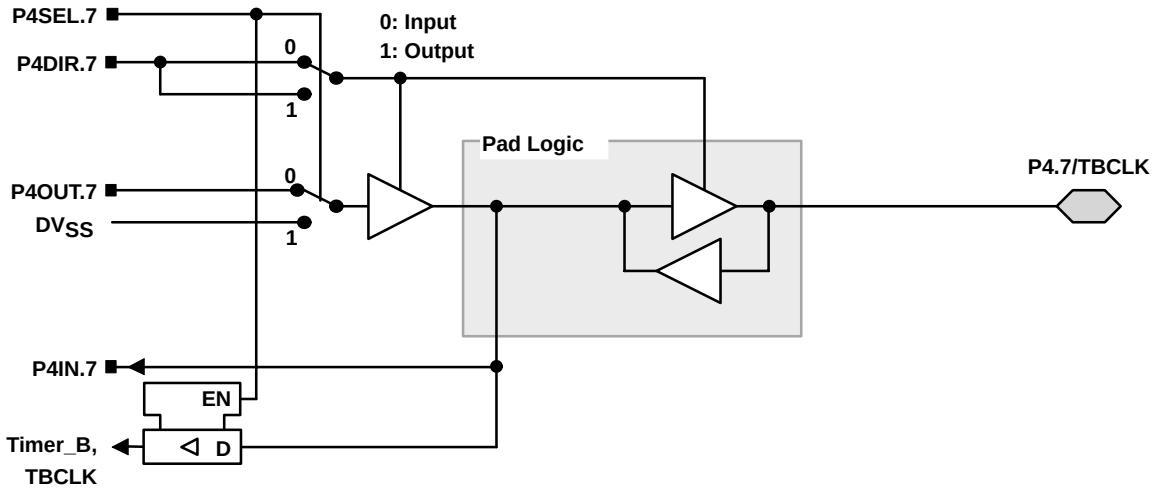
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal†	P4IN.0	CCI0A / CCI0B‡
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal†	P4IN.1	CCI1A / CCI1B‡
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal†	P4IN.2	CCI2A / CCI2B‡
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	DV_{SS}	P4IN.3	Unused
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	DV_{SS}	P4IN.4	Unused
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	DV_{SS}	P4IN.5	Unused
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	DV_{SS}	P4IN.6	Unused

† Signal from Timer_B
‡ Signal to Timer_B

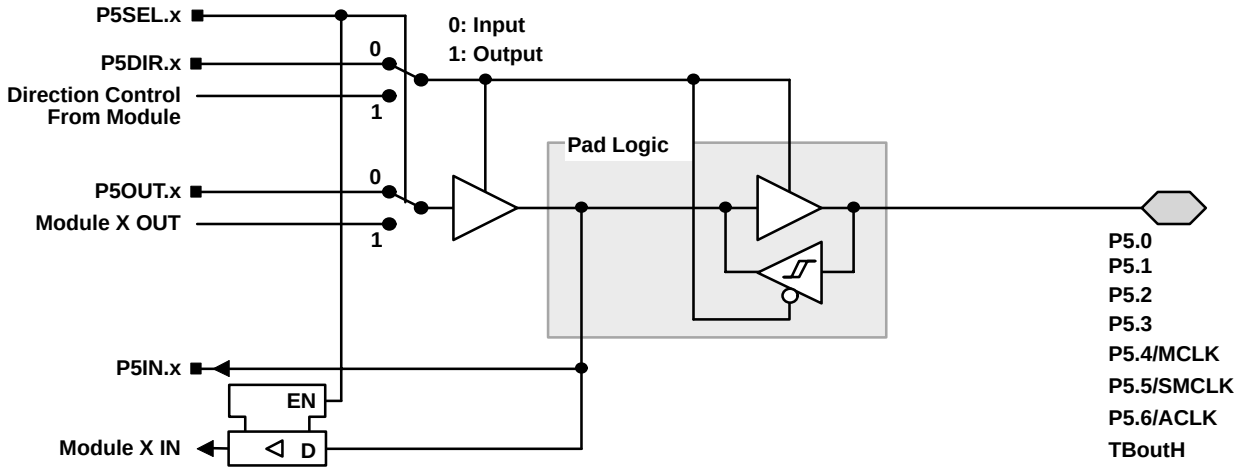
NOTE: TBoutHiZ signal is used by port module P4, pins P4.0 to P4.6. The function TBoutHiZ is mainly used with Timer_B. Port pins P4.3 to P4.6 have the TBoutHiZ function, but no Timer_B output is available for secondary functions. The port selection function can be used to get the port pin to high impedance and to use the P4DIR.x bits.

input/output schematic (continued)

port P4, P4.7, input/output with Schmitt-trigger



port P5, P5.0 to P5.7, input/output with Schmitt-trigger



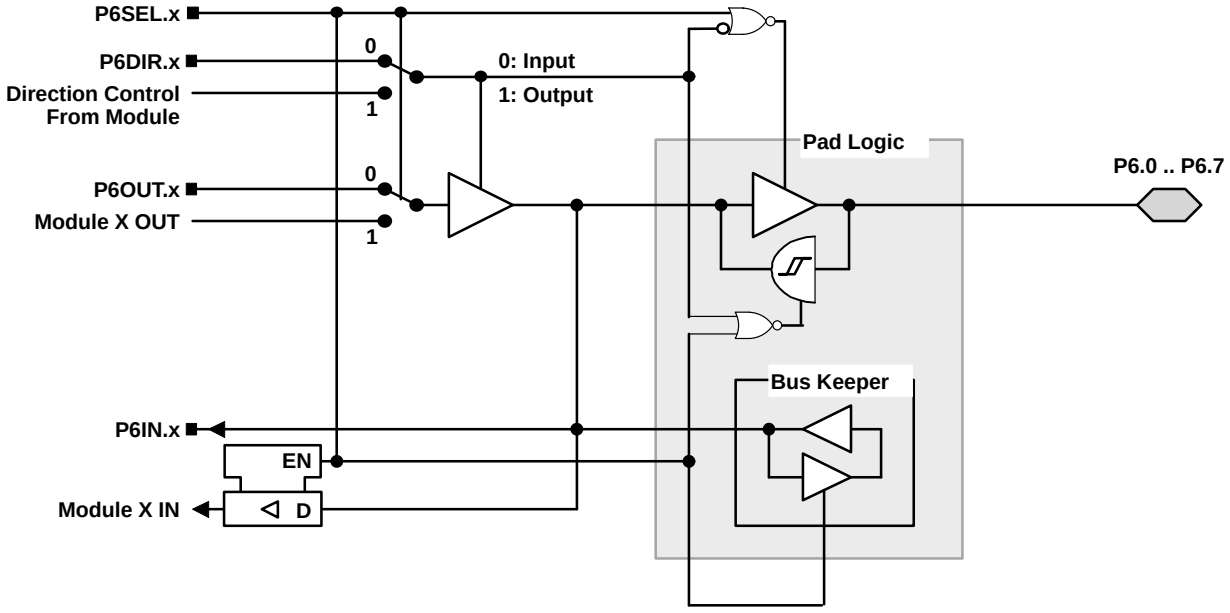
x: Bit Identifier, 0 to 7 for Port P5

PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV_{SS}	P5OUT.0	DV_{SS}	P5IN.0	unused
P5Sel.1	P5DIR.1	DV_{CC}	P5OUT.1	DV_{SS}	P5IN.1	unused
P5Sel.2	P5DIR.2	DV_{CC}	P5OUT.2	DV_{SS}	P5IN.2	unused
P5Sel.3	P5DIR.3	DV_{CC}	P5OUT.3	DV_{SS}	P5IN.3	unused
P5Sel.4	P5DIR.4	DV_{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV_{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV_{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV_{SS}	P5OUT.7	DV_{SS}	P5IN.7	TBoutHiZ

NOTE: TBoutHiZ signal is used by port module P4, pins P4.0 to P4.6. The function of TboutHiZ is mainly useful when used with Timer_B.

input/output schematic (continued)

port P6, P6.0 to P6.7, input/output with Schmitt-trigger



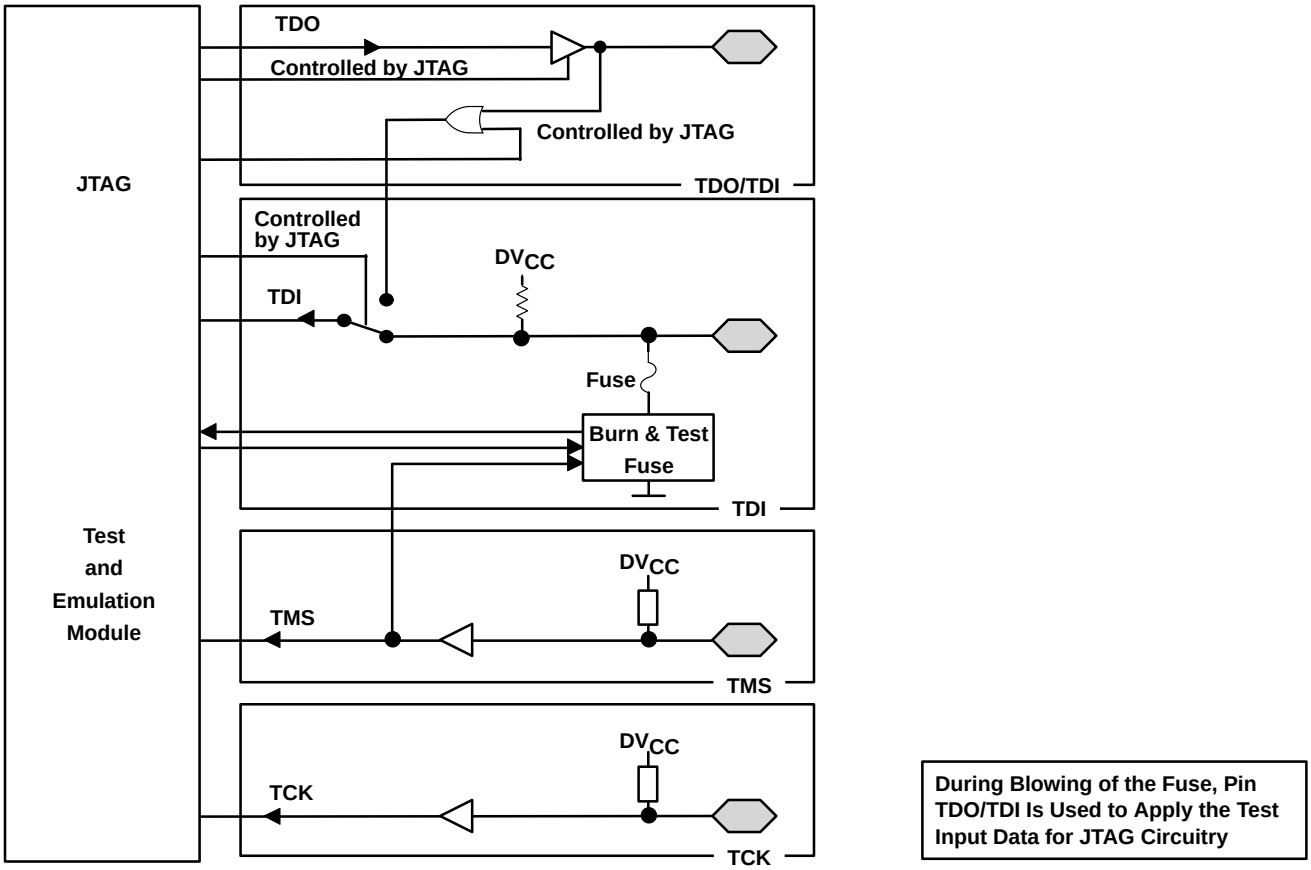
x: Bit Identifier, 0 to 7 for Port P6

PnSel.x	PnDIR.x	DIR. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV_{SS}	P6IN.6	unused
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV_{SS}	P6IN.7	unused

NOTE: Direction control bits P6DIR.x and P6SEL.x control whether the port function is active (P6DIR.x=0) or whether the input P6.x is in the high-impedance state. This is identical to the port P6 function in the MSP430F13x devices (used for emulation/prototyping), but different from other digital-only ports such as P5.

input/output schematic (continued)

JTAG pins TMS, TCK, TDI, TDO/TDI, input/output with Schmitt-trigger



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V can flow from the TDI pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 15). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

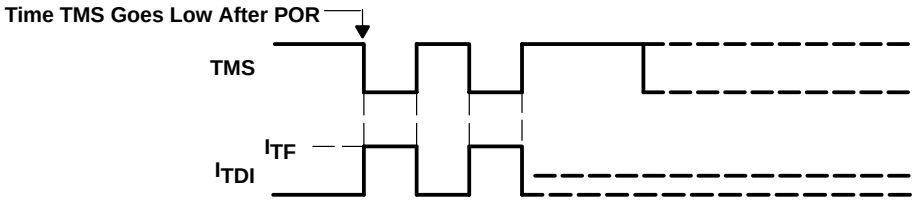
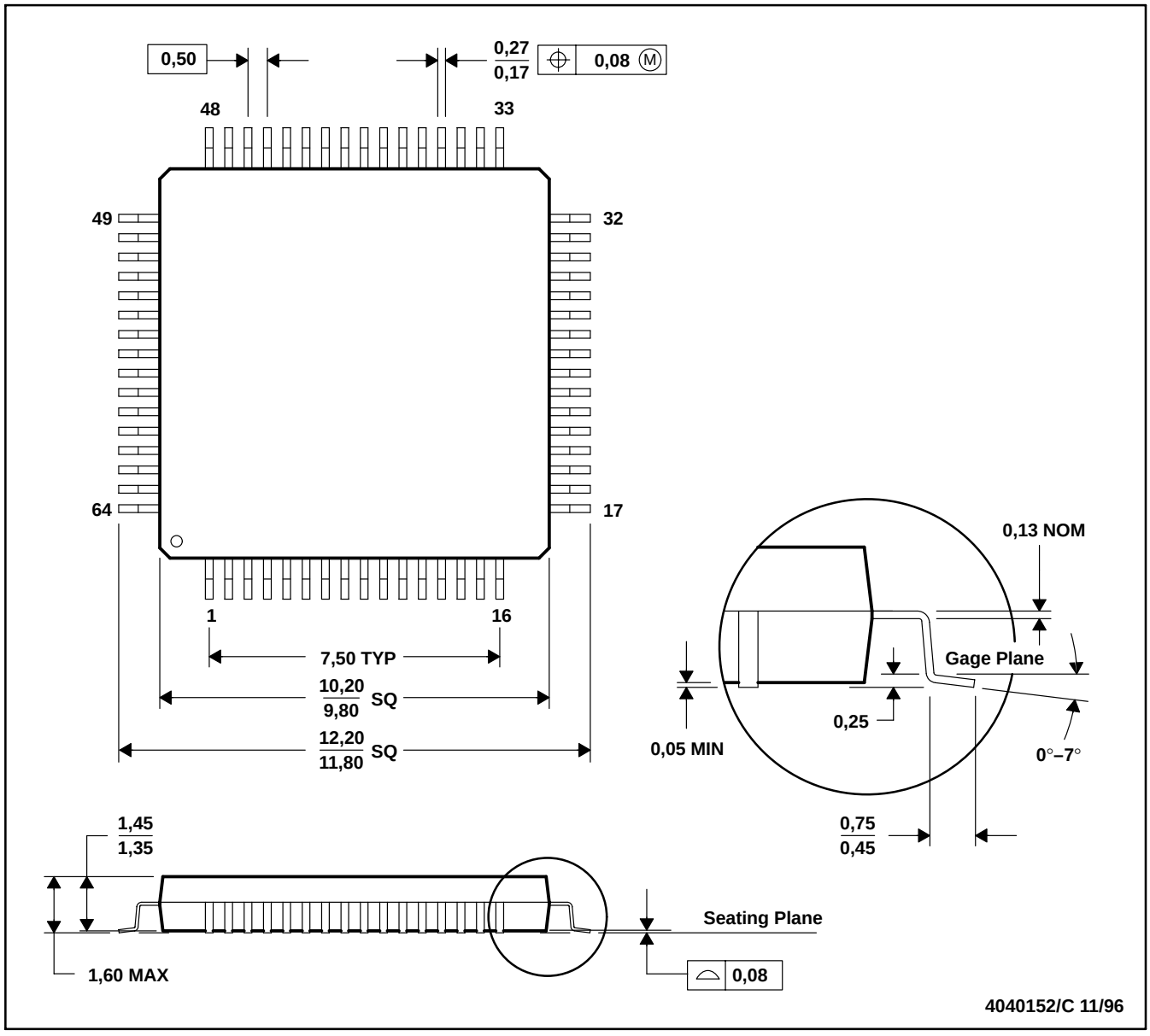


Figure 15. Fuse Check Mode Current

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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