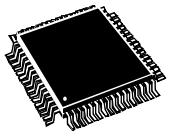
ST7265

LOW-POWER, FULL-SPEED USB 8-BIT MCU WITH 32K FLASH, 5K RAM, FLASH CARD I/F, TIMER, PWM, ADC, I^2C

DATA BRIEFING

- **Memories**
  - Up to 32K of ROM or Flash program memory with read/write protection
  - For Flash devices, In-Application Programming (IAP) via USB and In-Circuit programming (ICP)
  - Up to 5 Kbytes of RAM with up to 256 bytes stack
- **Clock, Reset and Supply Management**
  - PLL for generating 48 MHz USB clock using a 12 MHz crystal
  - Low Voltage Reset (optional)
  - Dual supply management: analog voltage detector on the USB power line to enable smart power switching from USB power to battery.
  - Programmable Internal Voltage Regulator for Memory cards (2.4V to 3.3V) supplying:
    Flash Card I/O lines (voltage shifting)
    Up to 50 mA for Flash card supply
  - Clock-out capability
- **47 programmable I/O lines**
  - 11 high sink I/Os (10mA at 1V)
  - 5 true open drain outputs
  - 16 lines programmable as interrupt inputs
- **USB (Universal Serial Bus) Interface**
  - with DMA for full speed bulk applications compliant with USB 12 Mbs specification (version 1.1)
  - On-Chip 3.3V USB voltage regulator and transceivers with software power-down
  - 5 USB endpoints:
    1 control endpoint
    2 IN endpoints supporting interrupt and bulk
    2 OUT endpoints supporting interrupt and bulk
  - Hardware conversion between USB bulk packets and 512-byte blocks



TQFP64 10x10
TQFP64 14x14

- **Mass Storage Interface**
  - DTC (Data Transfer Coprocessor): Universal Serial/Parallel communications interface, with software plug-ins for current and future protocol standards:
    16-bit IDE mode Compact Flash
    Multimedia Card (MMC protocol)
    SmartMediaCard
    Secure Digital Card
- **2 Timers**
  - Configurable Watchdog for system reliability
  - 16-bit Timer with 2 output compare functions.
- **1 Communication Interface**
  - I^2C Single Master Interface up to 400 KHz
- **D/A and A/D Peripherals**
  - PWM/BRM Generator (with 2 10-bit PWM/BRM outputs)
  - 8-bit A/D Converter (ADC) with 2 channels
- **Instruction Set**
  - 8-bit data manipulation
  - 63 basic instructions
  - 17 main addressing modes
  - 8 x 8 unsigned multiply instruction
  - True bit manipulation
- **Development Tools**
  - Full hardware/software development package

Device Summary

Features	ST72651	ST72F651	ST72652	ST72F652
Program memory	32K ROM	32K FLASH	16K ROM	16K FLASH
User RAM (stack) - bytes	5K (256)		1K (256)	
Peripherals	USB, DTC, Timer, ADC, I^2C, PWM		USB, DTC, Timer	
Operating Supply	Dual 2.4V to 5.5V or 4.0V to 5.5V (for USB)		Single 4.0V to 5.5V	
CPU Frequency	6 or 3 MHz (8 MHz in USB mode)		8, 6 or 3 MHz	
Package	TQFP64 (10 x10 or 14 x14)		TQFP64 (14 x14)	
Operating Temperature	0°C to +70°C			

Rev. 1.2

1 INTRODUCTION

The ST7265 MCU supports volume data exchange with a host (computer or kiosk) via a full speed USB interface. The MCU is capable of handing various transfer protocols, with a particular emphasis on FLASH media card mass storage applications.

ST7265 is compliant with the USB Mass Storage Class specifications, and supports related protocols such as BOT (Bulk Only Transfer) and CBI (Control, Bulk, Interrupt).

It is based on the ST7 standard 8-bit core, with specific peripherals for managing USB full speed data transfer between the host and most types of FLASH media card:

– A full speed USB interface with Serial Interface Engine, and on-chip 3.3V regulator and transceivers.

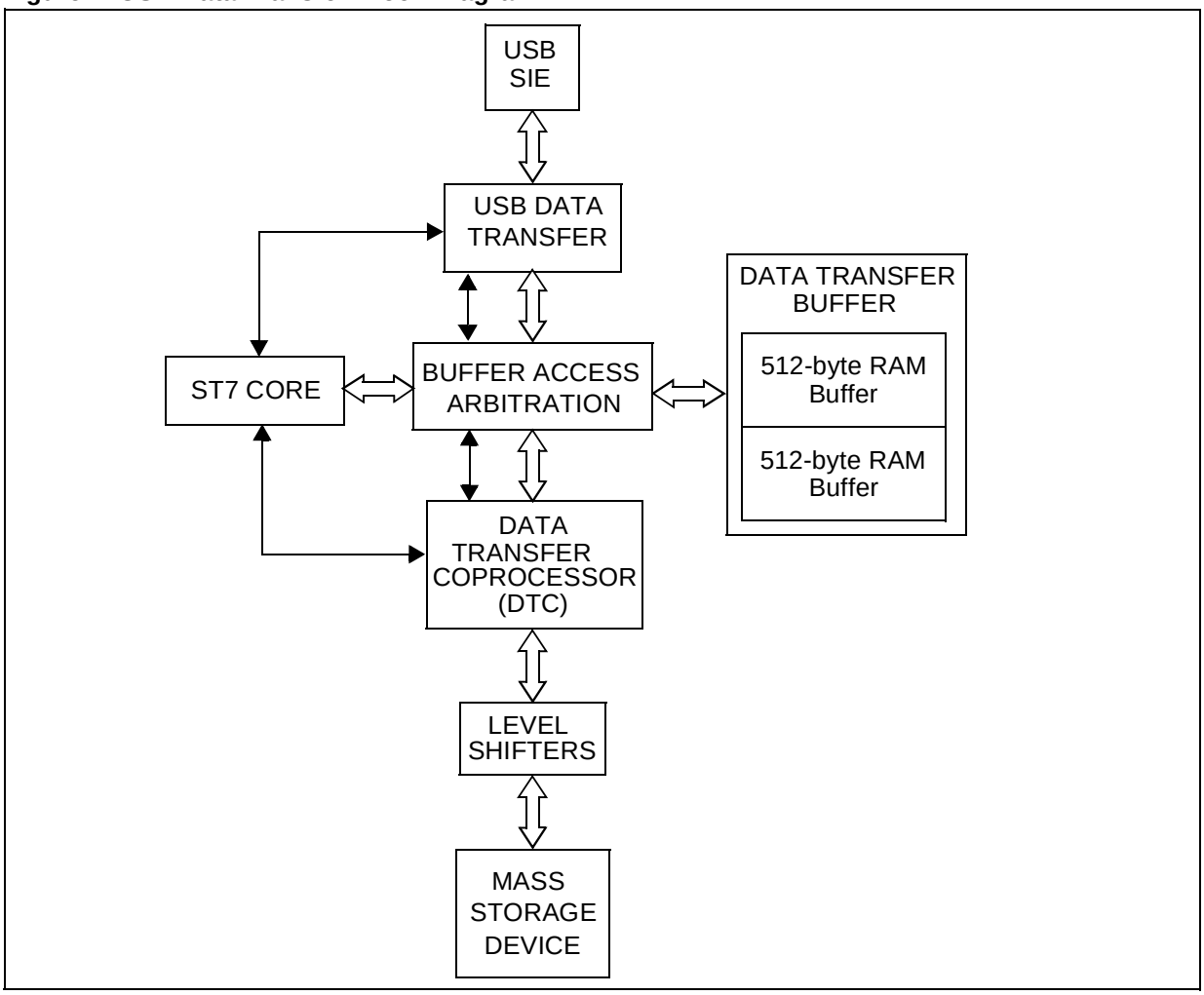
– A dedicated 24 MHz Data Buffer Manager state machine for handling 512-byte data blocks (this size corresponds to a sector both on computers and FLASH media cards).

– A Data Transfer Coprocessor (DTC), able to handle fast data transfer with external devices. This DTC also computes the CRC or ECC required to handle Mass storage media.

– An Arbitration block gives the ST7 core priority over the USB and DTC when accessing the Data Buffer. In USB mode, the USB interface is serviced before the DTC.

– A FLASH Supply Block able to provide programmable supply voltage and I/O electrical levels to the FLASH media card.

Figure 1. USB Data Transfer Block Diagram



INTRODUCTION (Cont'd)

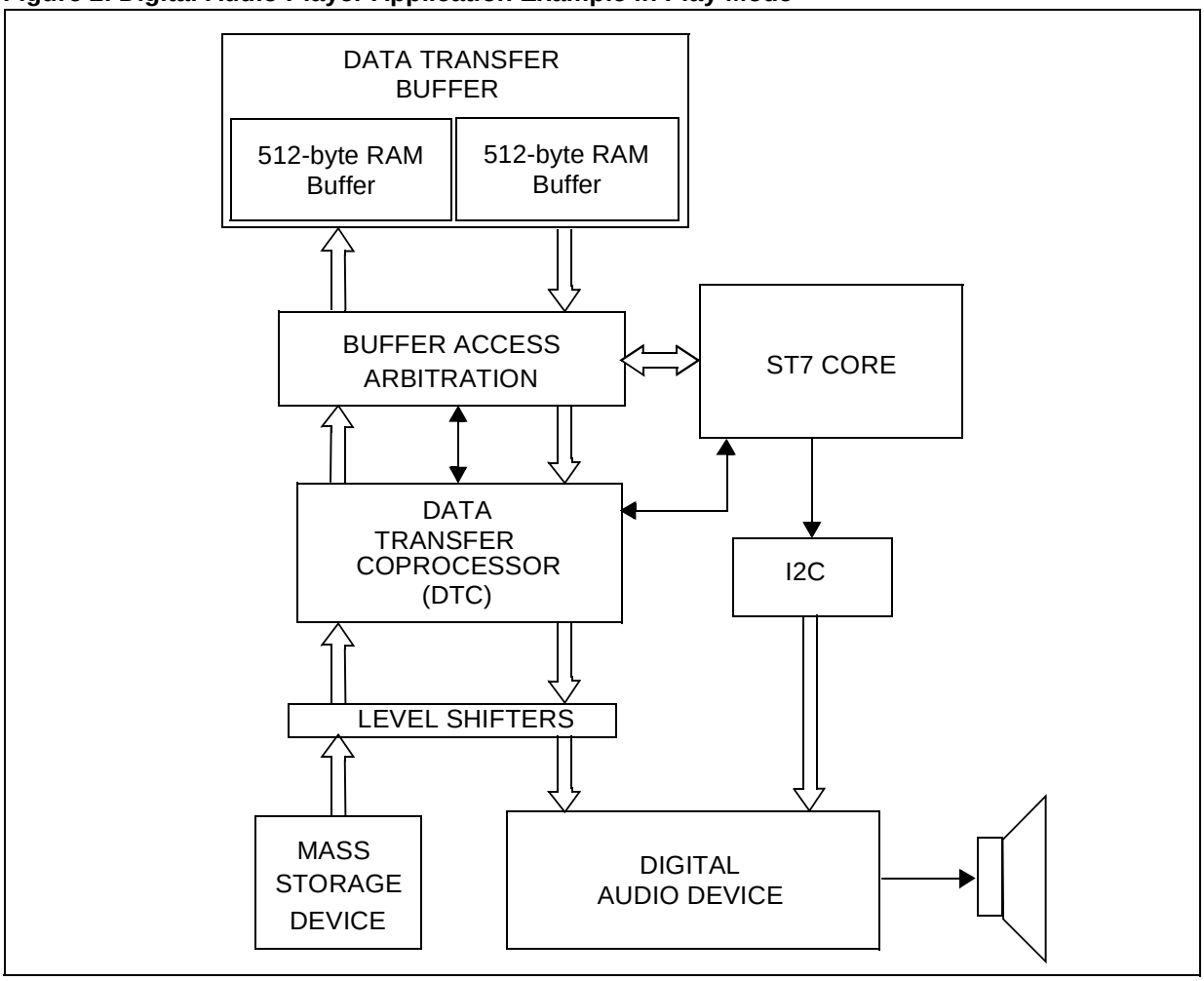
In addition to the peripherals for USB full speed data transfer, the ST7265 includes all the necesscary features for stand-alone applications with FLASH mass storage.

– Low voltage reset ensuring proper power-on or power-off of the device (selectable by option)
– Digital Watchdog
– 16-bit Timer with 2 output compare functions.
– Two 10-bit PWM outputs (not on all products - see device summary)
– Fast I^2C Single Master interface (not on all products - see device summary)
– 8-bit Analog-to-Digital converter (ADC) with 2 multiplexed analog inputs (not on all products - see device summary)

The ST72F65x are the Flash versions of the ST7265x in a TQFP64 package.

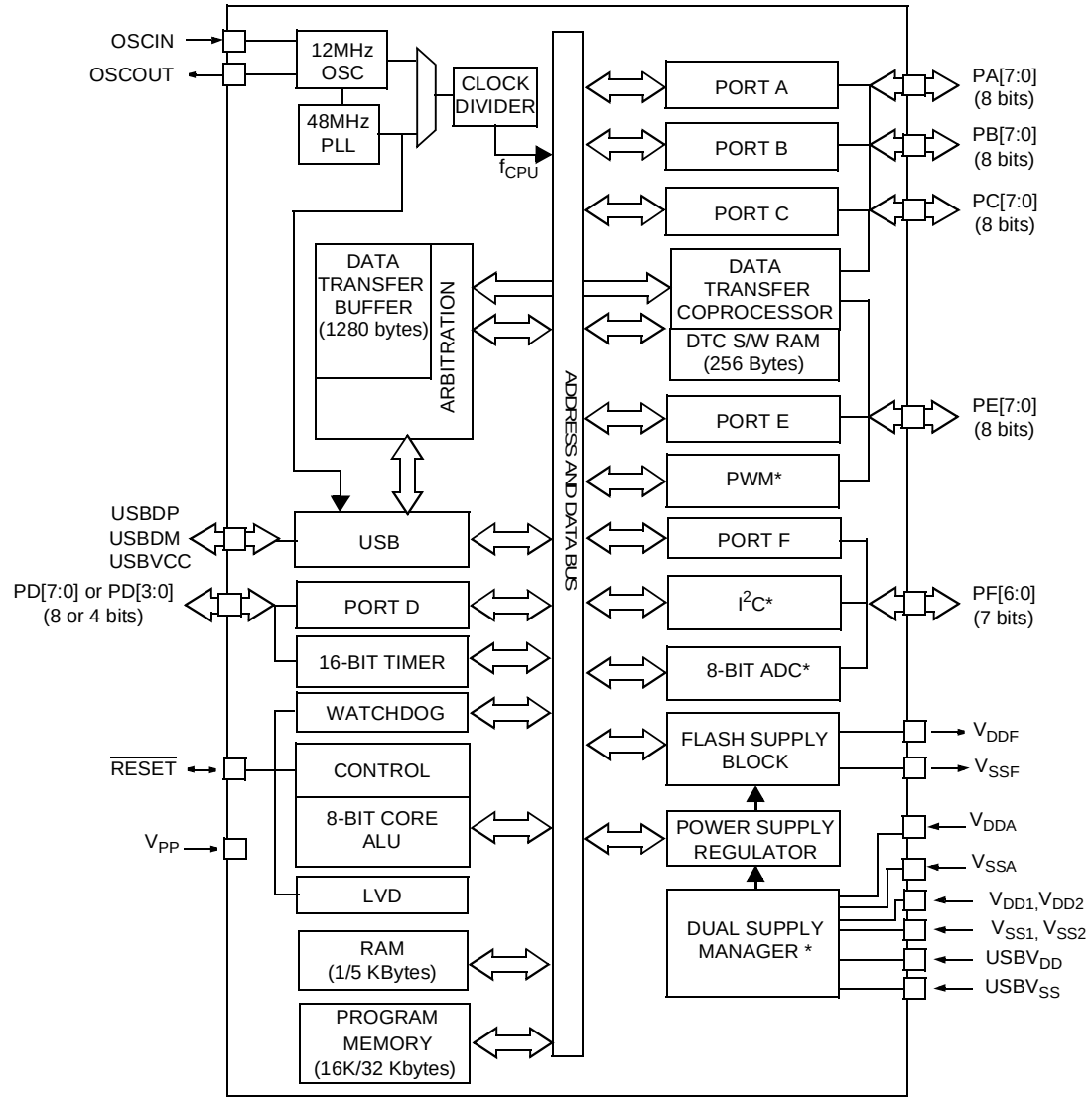
The ST7265x are the ROM versions in a TQFP64 package.

Figure 2. Digital Audio Player Application Example in Play Mode



INTRODUCTION (Cont'd)

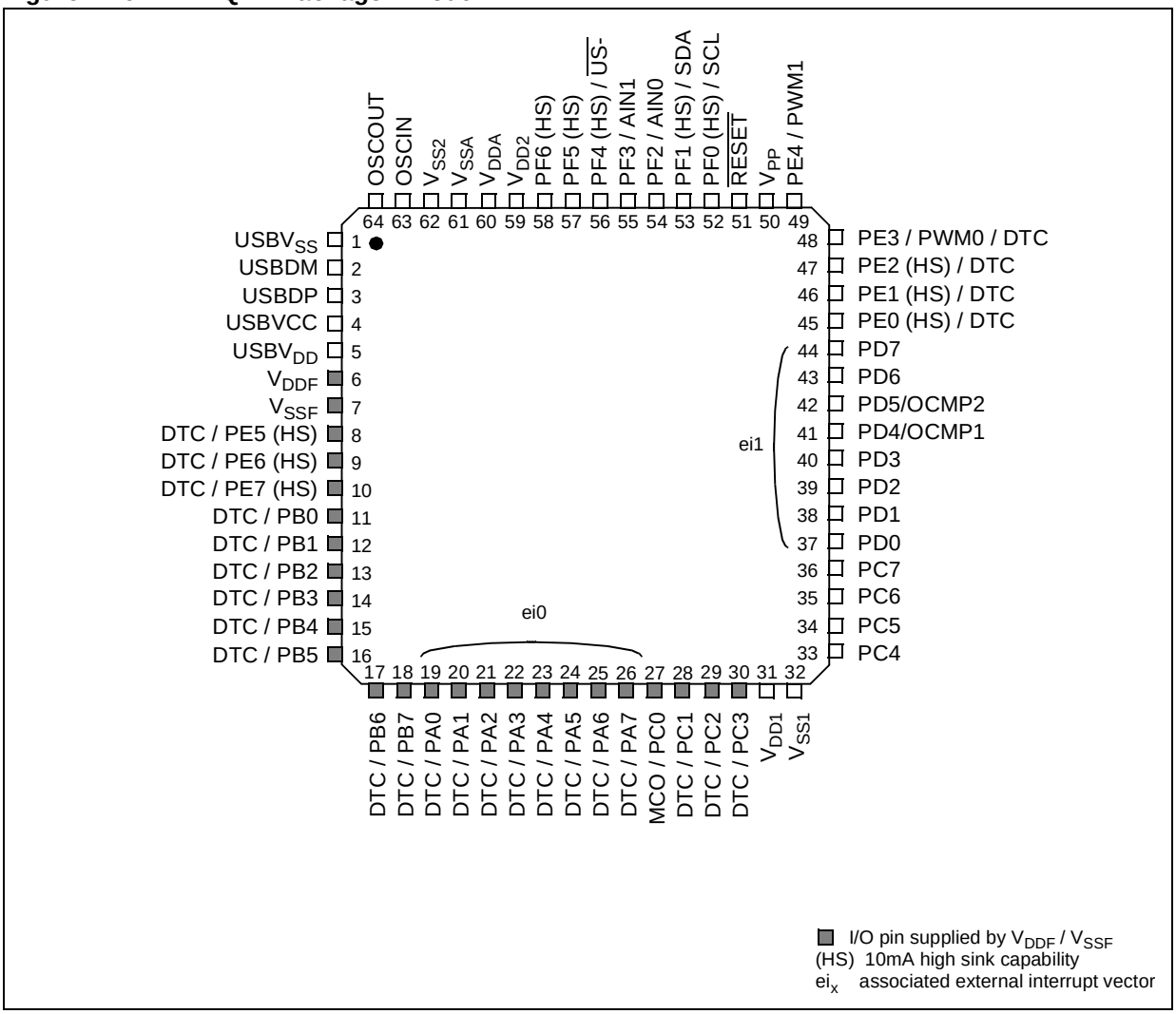
Figure 3. ST7265 Block Diagram



* not on all products (refer to Table 1: Device Summary)

2 PIN DESCRIPTION

Figure 4. 64-Pin TQFP Package Pinout



PIN DESCRIPTION (Cont'd)

Legend / Abbreviations:

Type: I = input, O = output, S = supply

V_{DDF} powered: I/O powered by the alternate supply rail, supplied by V_{DDF} and V_{SSF}.

In/Output level: C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 10mA high sink (on N-buffer only)

Port and control configuration:

– Input:float = floating, wpu = weak pull-up, int = interrupt

– Output: OD = open drain, T = true open drain, PP = push-pull, OP = pull-up enabled by option byte.

Refer to "I/O Port Implementation" on page 51 of the datasheet for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold.

Table 1. Device Pin Description

Pin	Pin Name	Type	V_{DDF} Powered	Level		Port / Control					Main Function (after reset)	Alternate Function
TQFP64				Input	Output	Input			Output			
						float	wpu	int	OD	PP		
1	$USBV_{SS}$	S									USB Digital ground	
2	USBDM	I/O									USB bidirectional data (data -)	
3	USBDP	I/O									USB bidirectional data (data +)	
4	USBVCC	O									USB power supply, output by the on-chip USB 3.3V linear regulator.	
5	$USBV_{DD}$	S									USB Power supply voltage (4V - 5.5V)	
6	V_{DDF}	S	X								Power Line for alternate supply rail. Can be used as input (with external supply) or output (when using the on-chip voltage regulator). **Note:** An external decoupling capacitor (min. 20nF) must be connected to this pin to stabilize the regulator.	
7	V_{SSF}	S	X								Ground Line for alternate supply rail. Can be used as input (with external supply) or output (when using the on-chip voltage regulator)	
8	PE5/DTC	I/O	X	C_T	HS	X^2			X^2	X	Port E5	DTC I/O with serial capability (MMC_CMD)
9	PE6/DTC	I/O	X	C_T	HS	X			X	X	Port E6	DTC I/O with serial capability (MMC_DAT)
10	PE7/DTC	I/O	X	C_T	HS	X			X	X	Port E7	DTC I/O with serial capability (MMC_CLK)
11	PB0/DTC	I/O	X	CT		X				X	Port B0	DTC
12	PB1/DTC	I/O	X	CT		X				X	Port B1	DTC
13	PB2/DTC	I/O	X	CT		X				X	Port B2	DTC
14	PB3/DTC	I/O	X	CT		X				X	Port B3	DTC
15	PB4/DTC	I/O	X	CT		X				X	Port B4	DTC
16	PB5/DTC	I/O	X	CT		X				X	Port B5	DTC
17	PB6/DTC	I/O	X	CT		X				X	Port B6	DTC

Pin	Pin Name	Type	V_{DDF} Powered	Level		Port / Control					Main Function (after reset)	Alternate Function
				Input	Output	Input			Output			
TQFP64						float	wpu	int	OD	PP		
18	PB7/DTC	I/O	X	CT		X				X	Port B7	DTC
19	PA0/DTC	I/O	X	CT		X		ei0	X	X	Port A0	DTC
20	PA1/DTC	I/O	X	CT		X			X	X	Port A1	DTC
21	PA2/DTC	I/O	X	CT		X			X	X	Port A2	DTC
22	PA3/DTC	I/O	X	CT		X			X	X	Port A3	DTC
23	PA4/DTC	I/O	X	CT		X			X	X	Port A4	DTC
24	PA5/DTC	I/O	X	CT		X			X	X	Port A5	DTC
25	PA6/DTC	I/O	X	CT		X			X	X	Port A6	DTC
26	PA7/DTC	I/O	X	CT		X			X	X	Port A7	DTC
27	PC0/MCO	I/O	X	CT		X				X	Port C0	Main Clock Output
28	PC1/DTC	I/O	X	C_T		X				X	Port C1	DTC I/O with serial capability (DATARQ)
29	PC2/DTC	I/O	X	C_T		X				X	Port C2	DTC I/O with serial capability (SDAT)
30	PC3/DTC	I/O	X	C_T		X				X	Port C3	DTC I/O with serial capability (SCLK)
31	V_{DD1}	S									Power supply voltage (2.4V - 5.5V)	
32	V_{SS1}	S									Digital ground	
33	PC4/DTC	I/O		C_T		X				X	Port C4	DTC
34	PC5/DTC	I/O		C_T		X				X	Port C5	DTC
35	PC6/DTC	I/O		C_T		X				X	Port C6	DTC
36	PC7/DTC	I/O		C_T		X				X	Port C7	DTC
37	PD0	I/O		CT		X		ei1	X	X	Port D0	
38	PD1	I/O		CT		X			X	X	Port D1	
39	PD2	I/O		CT		X			X	X	Port D2	
40	PD3	I/O		CT		X			X	X	Port D3	
41	PD4/OCMP1	I/O		CT		X			X	X	Port D4	Timer Output Compare 1
42	PD5/OCMP2	I/O		CT		X			X	X	Port D5	Timer Output Compare 2
43	PD6	I/O		CT		X			X	X	Port D6	
44	PD7	I/O		CT		X			X	X	Port D7	
45	PE0/DTC	I/O		CT	HS	X				X	Port E0	DTC
46	PE1/DTC	I/O		C_T	HS	X				X	Port E1	DTC
47	PE2/DTC	I/O		C_T	HS	X				X	Port E2	DTC
48	PE3/DTC/PWM0	I/O		C_T		X				X	Port E3	DTC / PWM Output 0

Pin	Pin Name	Type	V_{DDF} Powered	Level		Port / Control					Main Function (after reset)	Alternate Function
				Input	Output	Input			Output			
TQFP64						float	wpu	int	OD	PP		
49	PE4/PWM1	I/O		C_T		X				X	Port E4	PWM Output 1
50	V_{PP}	S									Flash programming voltage. Must be held low in normal operating mode.	
51	$\overline{RESET}$	I/O					X		X		Bidirectional. This active low signal forces the initialization of the MCU. This event is the top priority non maskable interrupt. This pin is switched low when the Watchdog has triggered or V_{DD} is low. It can be used to reset external peripherals.	
52	PF0 / SCL	I/O		C_T	HS	X			T		Port F0	I^2C Serial Clock[1]
53	PF1 / SDA	I/O		C_T	HS	X			T		Port F1	I^2C Serial Data[1]
54	PF2 / AIN0	I/O		C_T		X				X	Port F2	Analog Input 0[1]
55	PF3 / AIN1	I/O		C_T		X				X	Port F3	Analog Input 1[1]
56	PF4 / $\overline{USBEN}$	I/O		C_T	HS	X			T		Port F4	USB Power Management USB Enable (alternate function selected by option bit)
57	PF5	I/O		C_T	HS	X			T		Port F5	
58	PF6	I/O		C_T	HS	X			T		Port F6	
59	V_{DD2}	S									Main Power supply voltage (2.4V - 5.5V)	
60	V_{DDA}	S									Analog supply voltage	
61	V_{SSA}	S									Analog ground	
62	V_{SS2}	S									Digital ground	
63	OSCIN	I									Input/Output Oscillator pins. These pins connect a 12 MHz parallel-resonant crystal, or an external source to the on-chip oscillator.	
64	OSCOUT	O										

[1] If the peripheral is present on the device (see Table –)

[2] A weak pull-up can be enabled on PE5 input and open drain output by configuring the PEOR register and depending on the PE5PU bit in the option byte.

Notes: