National Semiconductor

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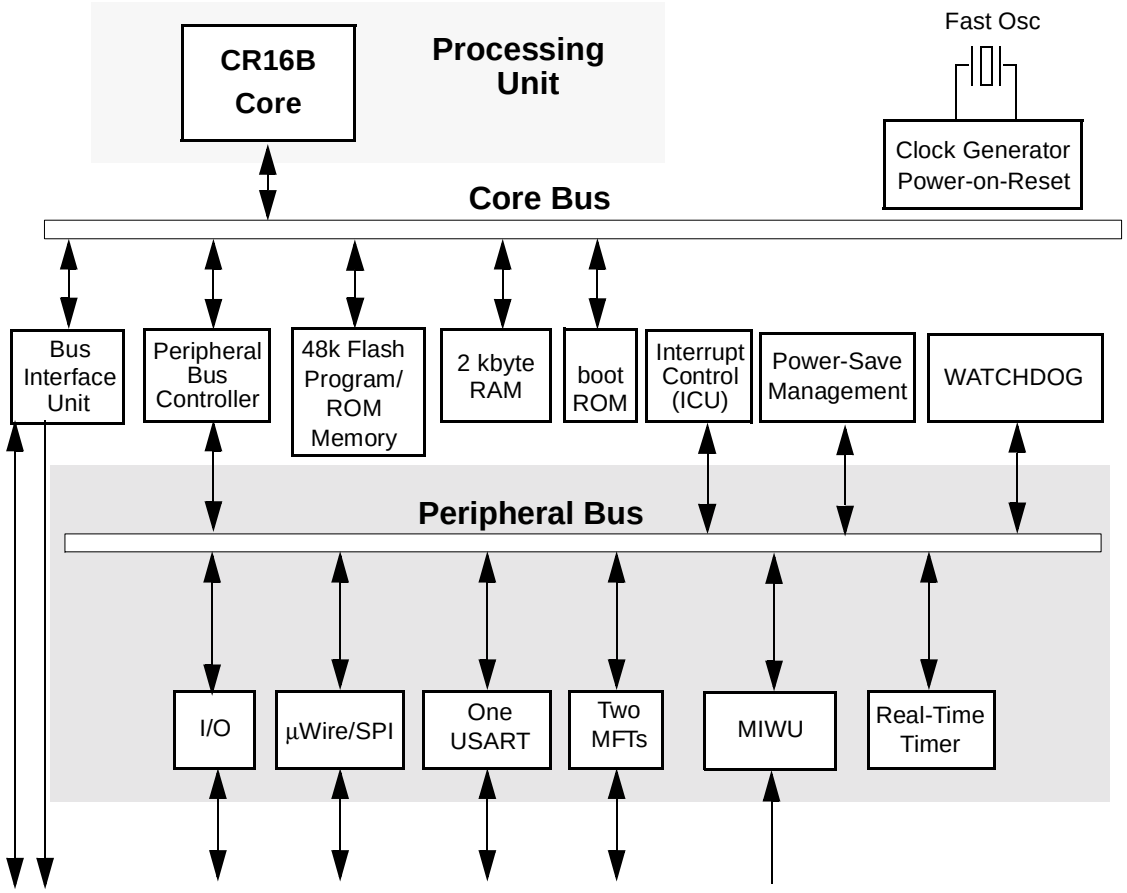
CR16MNS9/CR16MNS5 CompactRISC 16-Bit Reprogrammable/ROM Microcontrollers

1.0 General Description

The CR16MNS9 and CR16MNS5 CompactRISC™ microcontrollers are general-purpose 16-bit microcontrollers based on a Reduced Instruction Set Computer (RISC) architecture. The device operates as a complete microcomputer with all system timing, interrupt logic, flash program memory or ROM memory, RAM, and I/O ports included on-chip. It is ideally suited to a wide range of embedded controller applications because of its high performance, on-chip integrated features and low power consumption, resulting in decreased system cost.

The CR16MNS9 and CR16MNS5 offers the high performance of a RISC architecture while retaining the advantages of a traditional Complex Instruction Set Computer (CISC): compact code, on-chip memory and I/O, and reduced cost. The CPU uses a three-stage instruction pipeline that allows execution of up to one instruction per clock cycle, or up to 20 million instructions per second (MIPS) at a clock rate of 20 MHz.

Block Diagram



Note: Not all peripherals shown above will be contained in every device.

1.0 General Description (Continued)

All CR16MNS9 and CR16MNS5 devices have 48 kbytes of reprogrammable flash program memory or ROM memory, 1.5 kbytes of ISP memory, and 2 kbytes of static RAM. The 44-pin devices offer the same basic features as the 80-pin device, but with fewer I/O ports and peripheral modules due to the smaller number of available pins.

All CR16MNS9 and CR16MNS5 devices operate with a high-frequency crystal as the main clock source. The device supports several Power Save modes which are combined with multi-source interrupt and wake-up capabilities.

Powerful cross-development tools are available from National Semiconductor and third party suppliers to support the development and debugging of application software for the CR16MNS9 and CR16MNS5 . These tools let you program the application software in C and are designed to take full advantage of the CompactRISC architecture.

2.0 Features

- CPU Features
  - — Fully static core
  - — 20 MHz operating frequency
  - — Multi-source vectored interrupts (internal, external, and on-chip peripheral)
  - — On-chip power-on reset
- On-Chip Memory
  - — 48 kbytes of flash program memory or ROM memory
  - — For flash program memory, 1.5 kbytes of ISP memory is used to store boot loader code
  - — 2 kbytes of static RAM data memory
- On-Chip Peripherals
  - — One Universal Synchronous/Asynchronous Receiver/Transmitter (USART) device
  - — Programmable Idle Timer and real-time timer
  - — Two dual 16-bit multi-function timers (MFT1 and MFT2)
  - — SPI/MICROWIRE-PLUS serial interface
  - — Integrated WATCHDOG logic
- I/O Features
  - — Up to 33 general-purpose I/O pins (shared with on-chip peripheral I/O pins)
  - — Programmable I/O pin characteristics: TRI-STATE output, push-pull output, weak pull-up input, high-impedance input
  - — Software-configurable Schmitt triggers on inputs
- Power Supply
  - — 4.5V to 5.5V single-supply operation
- Temperature Range
  - — –40°C to +85°C
  - — 0°C to +70°C
- Development Support
  - — Real-time emulation and full program debug capabilities available
  - — CompactRISC tools provide C programming and debugging support

CR16 CompactRISC microcontroller Family Selection Guide

Programmable devices

NSID	Speed (MHz)	Flash (kByte)	EEPROM Data Memory (Bytes)	SRAM (kBytes)	USART	Timer	I/Os	Temp. Range	Peripherals	Package Type
CR16MNS944Vx	20	48	None	2	1	2	33	C, I	None	44PLCC

ROM devices

NSID	Speed (MHz)	ROM (kByte)	EEPROM Data Memory (Bytes)	SRAM (kBytes)	USART	Timer	I/Os	Temp. Range	Peripherals	Package Type
CR16MNS544Vxy	20	48	None	2	1	2	33	C, I	None	44PLCC

Note:

- Suffix x in the NSID is defined below:

Temperature Ranges:

I = Industrial	-40°C to +85°C is represented when x is 8
C = Commercial	0°C to +70°C is represented when x is 9

- Suffix y in the NSID defines the ROM code.

Note: All devices contains Clock and Reset, MICROWIRE/SPI, Multi-Input Wake-Up (MIWU), Power Management (PMM), and the Real-Time Timer and Watchdog (TWM) modules.

44-Pin PLCC versus 80-Pin PQFP

For 44PLCC packages, MICROWIRE/SPI slave mode, the first 4 MIWU channels and the Vref pin are not available. 80-pin PQFP packages provide the MICROWIRE/SPI master and slave modes, 8 MIWU channels, Vref pin, and two USARTs and two MFTs.

CR16MNS9 Derivatives

National Semiconductor currently offers a variety of the CR16 CompactRISC Microcontrollers. The CR16MHS offer complete functionality in an 80-pin PQFP package. The CR16MNS offers limited functionality described in the above sections and tables in a 44-pin PLCC package.

3.0 Device Overview

The CR16MNS9 and CR16MNS5 CompactRISC microcontrollers are complete microcomputers with all system timing, interrupt logic, program memory, and I/O ports included on-chip, making it well-suited to a wide range of embedded controller applications. The block diagram on page 1 of the data sheet shows the major on-chip components of the CR16MNS9 and CR16MNS5.

3.1 CR16B CPU CORE

The CR16MNS9 and CR16MNS5 uses the CR16B CPU core module. This is the same core used in other CompactRISC family members.

The high performance of the CPU core results from the implementation of a pipelined architecture with a two-bytes-per-cycle pipelined system bus. As a result, the CPU can support a peak execution rate of one instruction per clock cycle.

Compared with conventional RISC processors, the CR16MNS9 and CR16MNS5 differ in the following ways:

- The CPU core uses on-chip rather than external memory. This eliminates the need for large and complex bus interface units.
- Most instructions are 16 bits, so all basic instructions are just two bytes long. (Additional bytes are sometimes required for immediate values, so instructions can be two or four bytes long.)
- Non-aligned word access is allowed. Each instruction can operate on 8-bit or 16-bit.
- The device is designed to operate with a clock rate in the 10 to 25 MHz range rather than 100 MHz or more. Most embedded systems face EMI and noise constraints that limit clock speed to these lower ranges. A lower clock speed means a simpler, less costly silicon implementation.
- The instruction pipeline uses three stages. A smaller pipeline eliminates the need for costly branch prediction mechanisms and bypass registers, while maintaining adequate performance for typical embedded controller applications.

3.2 MEMORY

The CompactRISC architecture supports a uniform linear address space of 2 megabytes. The CR16MNS9 implementation of this architecture uses only the lowest 64 kbytes of address space. Three types of on-chip memory occupy specific intervals within this address space: 48 kbytes of flash program memory, 1.5 kbytes of ISP memory, and 2 kbytes of static RAM.

The 48 kbytes of flash program memory are used to store the application program. It has security features to prevent unintentional programming and to prevent unauthorized access to the program code. This memory can be programmed either with CR16MNS9 plugged into an EPROM programmer unit (external programming) or with the CR16MNS9 installed in the application system (in-system programming).

The 2 kbytes of static RAM are used for temporary storage of data and for the program stack and interrupt stack. Read and write operations can be byte-wide or word-wide, depending on the instruction executed by the CPU. Each memory access requires one clock cycle; no wait cycles or hold cycles are required.

There is a factory programmed boot memory used to store In-System-Programming (ISP) code. (this code allows programming of the program memory via one of the USART interfaces in the final application.)

For the flash program memory, the CR16MNS9 device internally generates the necessary voltages for programming. No additional power supply is required.

3.3 INPUT/OUTPUT PORTS

Each CR16MNS9 and CR16MNS5 devices have 33 software-configurable I/O pins, organized into five 8-pin ports called Port B, Port C, Port F, Port G, and Port I. Each pin can be configured to operate as a general-purpose input or general-purpose output. In addition, many I/O pins can be configured to operate as a designated input or output for an on-chip peripheral module such as the USART, timer, A/D converter, or MICROWIRE/SPI interface.

The I/O pin characteristics are fully programmable. Each pin can be configured to operate as a TRI-STATE output, push-pull output, weak pull-up input, or high-impedance input. Input pins can be software-configured to use Schmitt triggers for noise resistance.

Each 44-pin device has a subset of the pins available in the 80-pin device. This results in the loss of some features that are available in the larger-package device:

- USARTs and multi-function timers
- Synchronous mode in the remaining USART(s)
- Slave mode operation for the MICROWIRE/SPI interface
- Separate external V_{REF} for the A/D converter
- Comparators
- Four of the eight Multi-Input Wakeup pins
- $\overline{\text{NMI}}$ interrupt input pin

3.4 BUS INTERFACE UNIT

The Bus Interface Unit (BIU) controls the interface between the on-chip modules to the internal core bus. It determines the configured parameters for bus access (such as the number of wait states for memory access) and issues the appropriate bus signals for each requested access.

The BIU uses a set of control registers to determine how many wait states and hold states are to be used when accessing EEPROM memory. Upon start-up of the device, these registers must be programmed with appropriate values so that the minimum allowable number states is used. This number varies with the clock frequency and the type of on-chip device being accessed.

3.5 INTERRUPTS

The Interrupt Control Unit (ICU) receives interrupt requests from internal and external sources and generates interrupts to the CPU. An interrupt is an event that temporarily stops the normal flow of program execution and causes a separate interrupt service routine to be executed. After the interrupt is serviced, CPU execution continues with the next instruction in the program following the point of interruption.

Interrupts from the timers, USART, MICROWIRE/SPI interface, and multi-input wake-up are all maskable interrupts; they can be enabled or disabled by the software. There are 16 of these maskable interrupts, organized into 16 predetermined levels of priority.

The highest-priority interrupt is the Non-Maskable Interrupt ($\overline{\text{NMI}}$), which is generated by a signal received on the $\overline{\text{NMI}}$ input pin. This interrupt is not available in the 44-pin packages.

3.6 MULTI-INPUT WAKE-UP

The Multi-Input Wake-up (MIWU) module can be used for either of two purposes: to provide inputs for waking up (exiting) from the HALT, IDLE, or Power Save mode; or to provide general-purpose edge-triggered maskable interrupts from external sources. This eight-channel module generates one combined interrupt to the CPU based on the signals received on its eight input channels. Channels can be individually enabled or disabled, and programmed to respond to positive or negative edges.

3.7 DUAL CLOCK AND RESET

The Dual Clock and Reset (CLK2RES) module generates a high-speed main system clock from an external crystal network. It also provides the main system reset signal and a power-on reset function.

For the 44-pin devices and for devices not using a secondary crystal network, the slow clock can be generated by dividing the high-speed main clock by a prescaler factor.

3.8 POWER MANAGEMENT

The Power Management Module (PMM) improves the efficiency of the CR16MNS9 and CR16MNS5 devices by changing the operating mode (and therefore the power consumption) according to the current level of activity.

The CR16MNS9 device can operate in any of four power modes:

- Active: The device operates at full speed using the high-frequency clock. All device functions are fully operational.
- Power Save: The device operates at reduced speed using the slow clock. The CPU and some modules can continue to operate at this low speed.
- IDLE: The device is inactive except for the Power Management Module and Timing and Watchdog Module, which continue to operate using the slow clock.
- HALT: The device is inactive but still retains its internal state (RAM and register contents).

3.9 MULTI-FUNCTION TIMER

The Multi-Function Timer (MFT16) module contains two independent timer/counter units called MFT1 and MFT2, each containing a pair of 16-bit timer/counter registers. Each timer/counter unit can be configured to operate in any of the following modes:

- Processor-Independent Pulse Width Modulation (PWM) mode, which generates pulses of a specified width and duty cycle, and which also provides a general-purpose timer/counter
- Dual Input Capture mode, which measures the elapsed time between occurrences of external events, and which also provides a general-purpose timer/counter
- Dual Independent Timer mode, which generates system timing signals or counts occurrences of external events
- Single Input Capture and Single Timer mode, which provides one external event counter and one system timer

3.10 REAL-TIME TIMER AND WATCHDOG

The Timing and Watchdog Module (TWM) generates the clocks and interrupts used for timing periodic functions in the system. It also provides Watchdog protection against software errors. The module operates on the slow (32.768 KHz) clock.

The real-time timer generates a periodic interrupt to the CPU at a software-programmed interval. This can be used for real-time functions such as a time-of-day clock.

The Watchdog is designed to detect program execution errors such as an infinite loop or a “runaway” program. Once Watchdog operation is initiated, the application program must periodically write a specific value to a Watchdog register, within specific time intervals. If the software fails to do so, a Watchdog error is triggered, which resets the device.

3.11 USART

The USART is a Universal Synchronous/Asynchronous Receiver-Transmitter, a device used for serial communications. It supports a wide range of programmable baud rates and data formats, and handles parity generation and several error detection schemes. The baud rate is generated on-chip, under software control.

The synchronous mode of operation is not available in the 44-pin devices.

3.12 MICROWIRE/SPI

The MICROWIRE/SPI (MWSPI) interface module supports asynchronous serial communications with other devices that conform to MICROWIRE or Serial Peripheral Interface (SPI) specifications.

The MICROWIRE interface allows several devices to communicate over a single system consisting of three wires: serial in, serial out, and shift clock. At any given time, one device on the MICROWIRE interface operates as the master, while all other devices operate as slaves. An 80-pin CR16MHS supports the full set of slave select and Ready lines for multi-slave implementation, while a 44-pin CR16MNS has only the basic Data-in/Data-out/Clock lines, limiting its implementation to master mode.

3.13 DEVELOPMENT SUPPORT

A powerful cross-development tool set is available from National Semiconductor and third parties to support the development and debugging of application software for the CR16MNS9 and CR16MNS5 . The tool set lets you program the application software in C and is designed to take full advantage of the CompactRISC architecture.

There are In-System Emulation (ISE) devices available for the CR16MNS9 and CR16MNS5 from iSYSTEM™, as well as lower-cost evaluation boards. See your National Semiconductor sales representative for current information on availability of various features of emulation equipment and evaluation boards.

4.0 Memory Map

The CompactRISC architecture supports a uniform linear address space of 2 megabytes. The device implementation of this architecture uses only the lowest 64 kbytes of address space, ranging from 0000 to FFFF hex.

Table 1 Device Memory Map

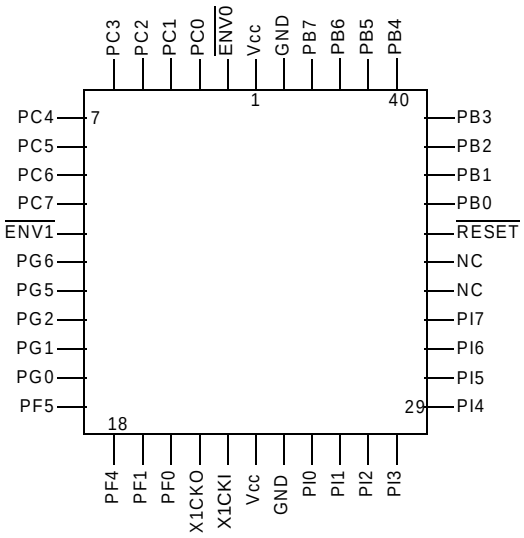
Address Range (hex)	Description
0000-BFFF	Flash Program Memory (48 kbytes)
DA00-DFF7	ISP Memory (1.5 kbytes)
DFF8-DFFF	Program ROM control/status
E000-E7FF	Static RAM (2 kbytes)
F900-F930	Device configuration registers
FB00-FB06	Port B registers
FB10-FB16	Port C registers
FC40-FC88	Clock, Power Management, and Wake-up registers
FCA0-FCA8	Port G registers
FD20-FD28	Port F registers
FE00-FE0C	Interrupt registers
FE40-FE4E	USART 1 registers
FE60-FE68	MICROWIRE registers
FEE0-FEE8	Port I registers
FF20-FF2A	Timer and WATCHDOG registers
FF40-FF50	T1 Timer registers
FF60-FF70	T2 Timer registers

5.0 Device Pinouts

The CR16MNS9 and CR16MNS5 are available in the following package:

x represents 8, or 9

y represents ROM codes; for programmable devices, leave out y.

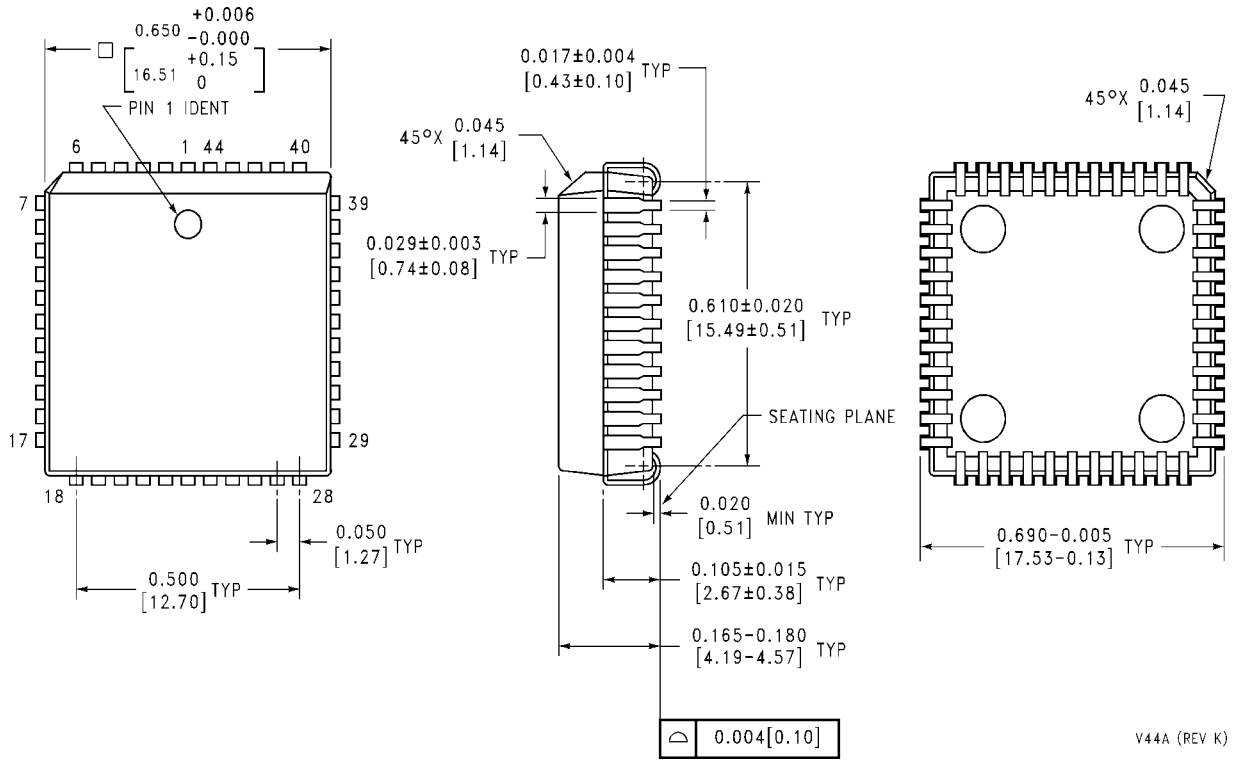


Top View

Order Number CR16MNS944Vx, CR16MNS544Vxy

See NS Package Number V44A

6.0 Physical Dimension inches (millimeters) unless otherwise noted



44 Lead Molded Plastic Leaded Chip Carrier

Order Number CR16MNS944Vx, CR16MNS544Vxy

See NS Package Number V44A

- Suffix x in the NSID is defined below:

Temperature Ranges:

x = 8 is -40°C to +85°C
= 9 is 0°C to +70°C

- Suffix y in the NSID defines the ROM code.

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