Hitachi 16-Bit Single-Chip Microcomputer

H8S/2339,
H8S/2338 Series,
H8S/2339 F-ZTAT™,
H8S/2338 F-ZTAT™

H8S/2339 F-ZTAT™	HD64F2339
H8S/2338 F-ZTAT™	HD64F2338
H8S/2338	HD6432338,
H8S/2337	HD6432337
H8S/2332	HD6412332

Reference Manual

— Individual Product Specifications —

HITACHI

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Revisions and Additions in this Edition

Page	Item	Revisions (See Manual for Details)
All		H8S/2339 (F-ZTAT version) product added
2	Table 1.1 Overview	Item "CPU" Maximum clock rate: 25 MHz
6	Figure 1.1 Internal Block Diagram	Port 5 I/O pins amended
6	1.2 Block Diagram	• H8S/2339F-ZTAT version EMLE pin added
7	1.3 Pin Arrangement	(FP-144G pin 97)
11	1.4 Pin Functions in Each Operating Mode	
15, 16	1.5 Pin Functions	MD2-MD0 function description amended
16		EMLE added
31	2.3 Operating Mode Descriptions	Modes 8 and 9 description amended
32		Modes 12 and 13 description amended
34	Figure 2.1 H8S/2339 Memory Map in Each Operating Mode	H8S/2339 address map added
56	Table 3.10 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs	Interrupt sources DMTEND0A, 0B, 1A, 1B added
73	4.2.5 Bus Control Register L (BCRL)	Bit 5: H8S/2339 address Note 2 added
98	Figure 4.15 CBR Refresh Timing	Note added
98	Figure 4.16 CBR Refresh Timing	Note added
100	Figure 4.18 $\overline{\text{DACK}}$ Output Timing when DDS = 1	Note added
101	Figure 4.19 $\overline{\text{DACK}}$ Output Timing when DDS = 0	Note added
109	Table 4.7 Pin States in Idle Cycle	$\overline{\text{CSn}}$, $\overline{\text{DACKm}}$ Note added
110	Figure 4.26 Example of Timing when Write Data Buffer Function is Used	Note added
112	Table 4.8 Pin States in Bus-Released State	$\overline{\text{CSn}}$, $\overline{\text{DACKm}}$ Note added
117	5.1 Overview	Ports 1 and F descriptions amended (driving one TTL load and 50 pF capacitive load)
149	Figure 5.4 Port 4 Pin Functions	$P4_7$ and $P4_6$ I/O amended

Page	Item	Revisions (See Manual for Details)
231	Table 5.34 I/O Port States in Each Processing State	[Notation] amendments, additions
298	Figure 6.11 Block Diagram of D/A Converter	Amended
300	6.12 RAM (H8S/2339)	Added
302, 303	6.14 ROM (H8S/2339)	Added
308	Table 7.2 DC Characteristics	V_{IH} min value amended
		V_{OL} max value amended
		$\lvert I_{in} \rvert$ max value amended
309		$-I_P$ min and max values amended
		I_{CC} typ and max values amended
		Analog/reference power supply current
		AI_{CC} typ and max values amended
		Note 4 amended
314	Figure 7.5 Interrupt Input Timing	$\overline{IRQi} \rightarrow \overline{IRQ}$
320	Figure 7.9 DRAM Bus Timing	$\overline{HWR}$, $\overline{LWR} \rightarrow \overline{HWR}$ ($\overline{WE}$)
322	Figure 7.12 Burst ROM Access Timing	$\overline{CS7}$–$\overline{CS0} \rightarrow \overline{CS0}$
323	Figure 7.13 Burst ROM Access Timing	$\overline{CS7}$–$\overline{CS0} \rightarrow \overline{CS0}$
334	Table 7.9 A/D Conversion Characteristics	Conversion time and absolute accuracy values (nonlinearity error, offset error, full-scale error) amended
336	Table 7.11 Absolute Maximum Ratings	V_{CC} and AV_{CC} rated values amended
		Note amended
337	Table 7.12 DC Characteristics	Test conditions (V_{CC}, AV_{CC}, V_{ref}) amended
338		V_{IH} min value amended
		$\lvert I_{in} \rvert$ max value amended
		$-I_P$ test conditions amended
		I_{CC} typ and max values amended
		Analog/reference power supply current
		AI_{CC} typ and max values amended
		Notes 2, 3, and 4 amended
339	Table 7.13 Permissible Output Currents	Test conditions (V_{CC}, AV_{CC}, V_{ref}) amended
347	Table 7.19 A/D Conversion Characteristics	Conversion time and absolute accuracy values (nonlinearity error, offset error, full-scale error) amended

Page	Item	Revisions (See Manual for Details)
348	Table 7.20 D/A Conversion Characteristics	Test conditions B (V_{ref}) amended
349	Table 7.21 Flash Memory Characteristics	All items amended
351	8.1 List of Registers (Address Order)	HF800-H'FBFF DAR, CRA, CRB amended
353		H'FED5 BCRL bit 5 added
		H'FEDB RAMER Note added
360		H'FFCB EBR2 bits 5 and 4 added
363 to 365	8.2 List of Registers (By Module)	Common to DMAC, TPU0-TPU5, and TPU added
368		Power-down mode added
369		Port 4 added
404	8.3 Functions	BCRL bit 5 H8S/2339 description added
		DRAMCR bit 6 description amended
		TRr $\rightarrow$ Tr, TRC1 $\rightarrow$ Tc1
426		DTVECR R/W Note amendment, addition
493		FLMCR1 bit 7 H8S/2339 Note added
495		EBR2 bits 5 and 4 added

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Organization of H8S/2339, H8S/2338 Series Reference Manual

The following manuals are available for H8S/2339 and H8S/2338 Series products.

Table 1 H8S/2339, H8S/2338 Series Manuals

Title	Document Code
H8S/2600 Series, H8S/2000 Series Programming Manual	ADE-602-083A
H8S/2339, H8S/2338 Series, H8S/2329, H8S/2328 Series, H8S/2318 Series Hardware Manual	ADE-602-171A (in preparation)
H8S/2339, H8S/2338 Series, H8S/2339 F-ZTAT™, H8S/2338 F-ZTAT™ Reference Manual	ADE-602-162A

The H8S/2600 Series, H8S/2000 Series Programming Manual gives a detailed description of the architecture and instruction set of the H8S/2000 CPU.

The H8S/2339, H8S/2338 Series, H8S/2329, H8S/2328 Series, H8S/2318 Series Hardware Manual describes the operation of on-chip functions, and gives a detailed description of the related registers.

The H8S/2339, H8S/2338 Series, H8S/2339 F-ZTAT™, H8S/2338 F-ZTAT™ Reference Manual mainly covers information, including pin arrangement, I/O ports, MCU operating modes (address maps), interrupt vectors, bus control, and electrical characteristics, and also includes a brief description of all I/O registers for the convenience of the user.

The contents of the H8S/2339, H8S/2338 Series, H8S/2329, H8S/2328 Series, H8S/2318 Series Hardware Manual and the H8S/2339, H8S/2338 Series, H8S/2339 F-ZTAT™, H8S/2338 F-ZTAT™ Reference Manual are summarized in table 2.

Table 2 Contents of Hardware Manual and Reference Manual

No.	Item	Hardware Manual	Reference Manual
1	Overview	○	○ (including pin arrangement)
2	MCU operating modes (including address maps)	—	◎
3	Exception handling	○	○
4	Interrupt controller	◎	○
5	Bus controller	◎	◎
6	DMA controller (DMAC)	◎	—
7	Data transfer controller (DTC)	◎	—
8	16-bit timer pulse unit (TPU)	◎	—
9	Programmable pulse generator (PPG)	◎	—
10	8-bit timers	◎	—
11	Watchdog timer	◎	—
12	Serial communication interface (SCI)	◎	—
13	Smart card interface	◎	—
14	A/D converter	◎	—
15	D/A converter	◎	—
16	RAM	◎	—
17	ROM (flash memory)	◎	—
18	Clock pulse generator	◎	—
19	Power-down modes	◎	—
20	I/O ports (including port block diagrams)	—	◎
21	Electrical characteristics	—	○
22	Register reference chart (in address order, with function summary)	—	○
23	Instruction set	○	—
24	Package dimension diagrams	—	○

○: Included

◎: Included (with detailed register descriptions)

—: Not included

The following chart shows where to find various kinds of information for different purposes.

For product evaluation information, or comparative specification information for current users of Hitachi products

For product specifications

Overview	1.1 Overview
Pin arrangement diagram	1.3 Pin Arrangement
Block diagrams of function modules	Section 6 Peripheral Block Diagrams
Pin functions	1.5 Pin Functions
Electrical characteristics	Section 7 Electrical Characteristics

For detailed information on functions

For details of operation of modules

I/O port information	Section 5 I/O Ports
Interrupts and exception handling	Section 3 Exception Handling and Interrupt Controller
Information on other modules	H8S/2339, H8S/2338 Series, H8S/2329, H8S/2328 Series, H8S/2318 Series Hardware Manual

For information on operating modes

Pin functions	1.5 Pin Functions
List	1.4 Pin Functions in Each Operating Mode
Detailed descriptions	Section 2 MCU Operating Modes

For use as design material

For information on registers

List	Section 8 registers
To find a register from its address	8.1 List of Registers (Address Order)
To find register information by function	8.2 List of Registers (By Module)
Setting procedure and notes	H8S/2339, H8S/2338 Series, H8S/2329, H8S/2328 Series, H8S/2318 Series Hardware Manual

For information on instructions

List	
Operation description and notes	H8S/2600 Series, H8S/2000 Series Programming Manual
Program examples	

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Contents

Section 1 Overview

1.1 Overview

The H8S/2339 and H8S/2338 Series are series of microcomputers (MCUs: microcomputer units), built around the H8S/2000 CPU, employing Hitachi's proprietary architecture, and equipped with peripheral functions on-chip.

The H8S/2000 CPU has an internal 32-bit architecture, is provided with sixteen 16-bit general registers and a concise, optimized instruction set designed for high-speed operation, and can address a 16-Mbyte linear address space. The instruction set is upward-compatible with H8/300 and H8/300H CPU instructions at the object-code level, facilitating migration from the H8/300, H8/300L, or H8/300H Series.

On-chip peripheral functions required for system configuration include DMA controller (DMAC) and data transfer controller (DTC) bus masters, ROM and RAM memory, a 16-bit timer pulse unit (TPU), programmable pulse generator (PPG), 8-bit timer, watchdog timer (WDT), serial communication interface (SCI), A/D converter, D/A converter, and I/O ports.

A high-functionality bus controller is also provided, enabling fast and easy connection of DRAM and other kinds of memory.

Single-power-supply flash memory (F-ZTAT™*) and mask ROM versions are available, providing a quick and flexible response to conditions from ramp-up through full-scale volume production, even for applications with frequently changing specifications. ROM is connected to the CPU via a 16-bit data bus, enabling both byte and word data to be accessed in one state. Instruction fetching is thus speeded up, and processing speed increased.

The features of the H8S/2339 and H8S/2338 Series are shown in table 1.1.

Note: * F-ZTAT is a trademark of Hitachi, Ltd.

Table 1.1 Overview

Item	Specification
CPU	• General-register machine — Sixteen 16-bit general registers (also usable as sixteen 8-bit registers or eight 32-bit registers) • High-speed operation suitable for realtime control — Maximum clock rate: 25 MHz — High-speed arithmetic operations 8/16/32-bit register-register add/subtract: 40 ns (at 25 MHz operation) 16 × 16-bit register-register multiply: 800 ns (at 25 MHz operation) 32 ÷ 16-bit register-register divide: 800 ns (at 25 MHz operation) • Instruction set suitable for high-speed operation — Sixty-five basic instructions — 8/16/32-bit data transfer, arithmetic, and logic instructions — Unsigned/signed multiply and divide instructions — Powerful bit-manipulation instructions • CPU operating mode — Advanced mode: 16-Mbyte address space
Bus controller	• Address space divided into 8 areas, with bus specifications settable independently for each area • Chip select output possible for each area • Choice of 8-bit or 16-bit access space for each area • 2-state or 3-state access space can be designated for each area • Number of program wait states can be set for each area • Maximum 8-Mbyte DRAM directly connectable (or use of interval timer possible) • External bus release function
DMA controller (DMAC)	• Choice of short address mode or full address mode • 4 channels in short address mode • 2 channels in full address mode • Transfer possible in repeat mode, block transfer mode, etc. • Single address mode transfer possible • Can be activated by internal interrupt
Data transfer controller (DTC)	• Can be activated by internal interrupt or software • Multiple transfers or multiple types of transfer possible for one activation source • Transfer possible in repeat mode, block transfer mode, etc. • Request can be sent to CPU for interrupt that activated DTC

Item	Specification
16-bit timer pulse unit (TPU)	• 6-channel 16-bit timer on-chip • Pulse I/O processing capability for up to 16 pins • Automatic 2-phase encoder count capability
Programmable pulse generator (PPG)	• Maximum 16-bit pulse output possible with TPU as time base • Output trigger selectable in 4-bit groups • Non-overlap margin can be set • Direct output or inverse output setting possible
8-bit timer, 2 channels	• 8-bit up-counter (external event count capability) • Two time constant registers • Two-channel connection possible
Watchdog timer	• Watchdog timer or interval timer selectable
Serial communication interface (SCI), 3 channels	• Asynchronous mode or synchronous mode selectable • Multiprocessor communication function • Smart card interface function
A/D converter	• Resolution: 10 bits • Input: 12 channels • 6.7 µs minimum conversion time (at 20 MHz operation) • Single or scan mode selectable • Sample-and-hold function • A/D conversion can be activated by external trigger or timer trigger
D/A converter	• Resolution: 8 bits • Output: 4 channels
I/O ports	• 106 input/output pins, 12 input-only pins
Memory	• Flash memory and mask ROM • High-speed static RAM
Interrupt controller	• Nine external interrupt pins (NMI, $\overline{IRQ}_0$ to $\overline{IRQ}_7$) • 52 internal interrupt sources • Eight priority levels settable

Product Name	ROM	RAM
H8S/2339*	384 kbytes	32 kbytes
H8S/2338	256 kbytes	8 kbytes
H8S/2337	128 kbytes	8 kbytes
H8S/2332	—	8 kbytes

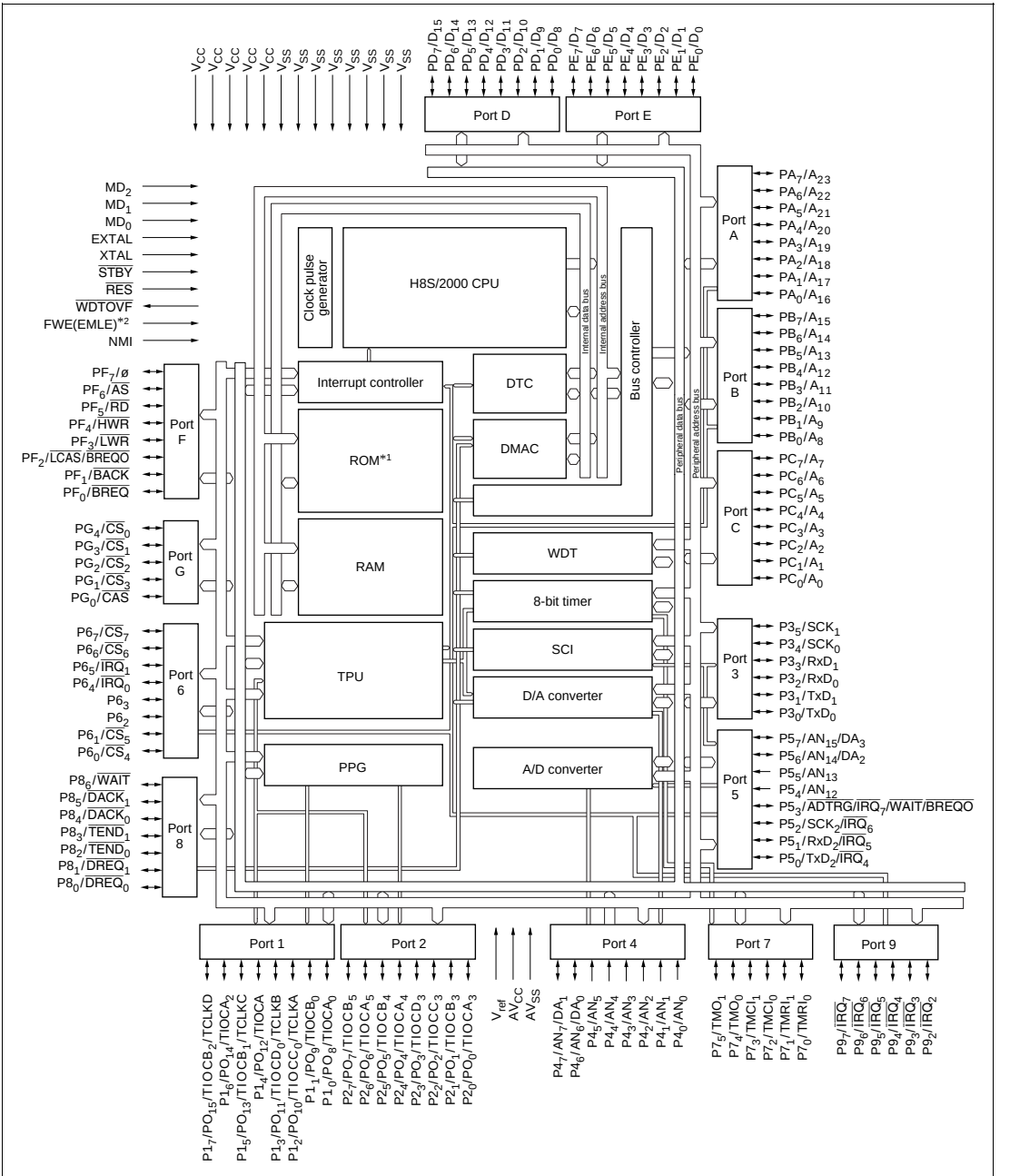
Note: * Under development

Item	Specification
Power-down state	• Medium-speed mode • Sleep mode • Module stop mode • Software standby mode • Hardware standby mode • Variable clock division ratio
Operating modes	• Eight MCU operating modes (H8S/2338 F-ZTAT version)

Mode	CPU Operating Mode	Description	On-Chip ROM	External Data Bus: Initial Value	External Data Bus: Maximum Value
0	—	—	—	—	—
1					
2					
3					
4	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
5				8 bits	16 bits
6		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
7		Single-chip mode		—	—
8	—	—	—	—	—
9					
10	Advanced	Boot mode	Enabled	8 bits	16 bits
11				—	—
12	—	—	—	—	—
13					
14	Advanced	User program mode	Enabled	8 bits	16 bits
15				—	—

Item	Specification				
Operating modes	• Four MCU operating modes (H8S/2339 F-ZTAT version, Mask ROM, and ROMless versions)				
					External Data Bus
	Mode	**CPU Operating Mode**	**Description**	**On-Chip ROM**	**Initial Value**	**Maximum Value**
	1	—	—	—	—	—
	2					
	3					
	4*	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
	5*		Expanded mode with on-chip ROM disabled	Disabled	8 bits	16 bits
	6		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
	7		Single-chip mode	Enabled	—	—
	Note: * Only modes 4 and 5 are provided in the ROMless version.					
Clock pulse generator	• Built-in duty correction circuit					
Package	• 144-pin plastic QFP (FP-144)					

1.2 Block Diagram

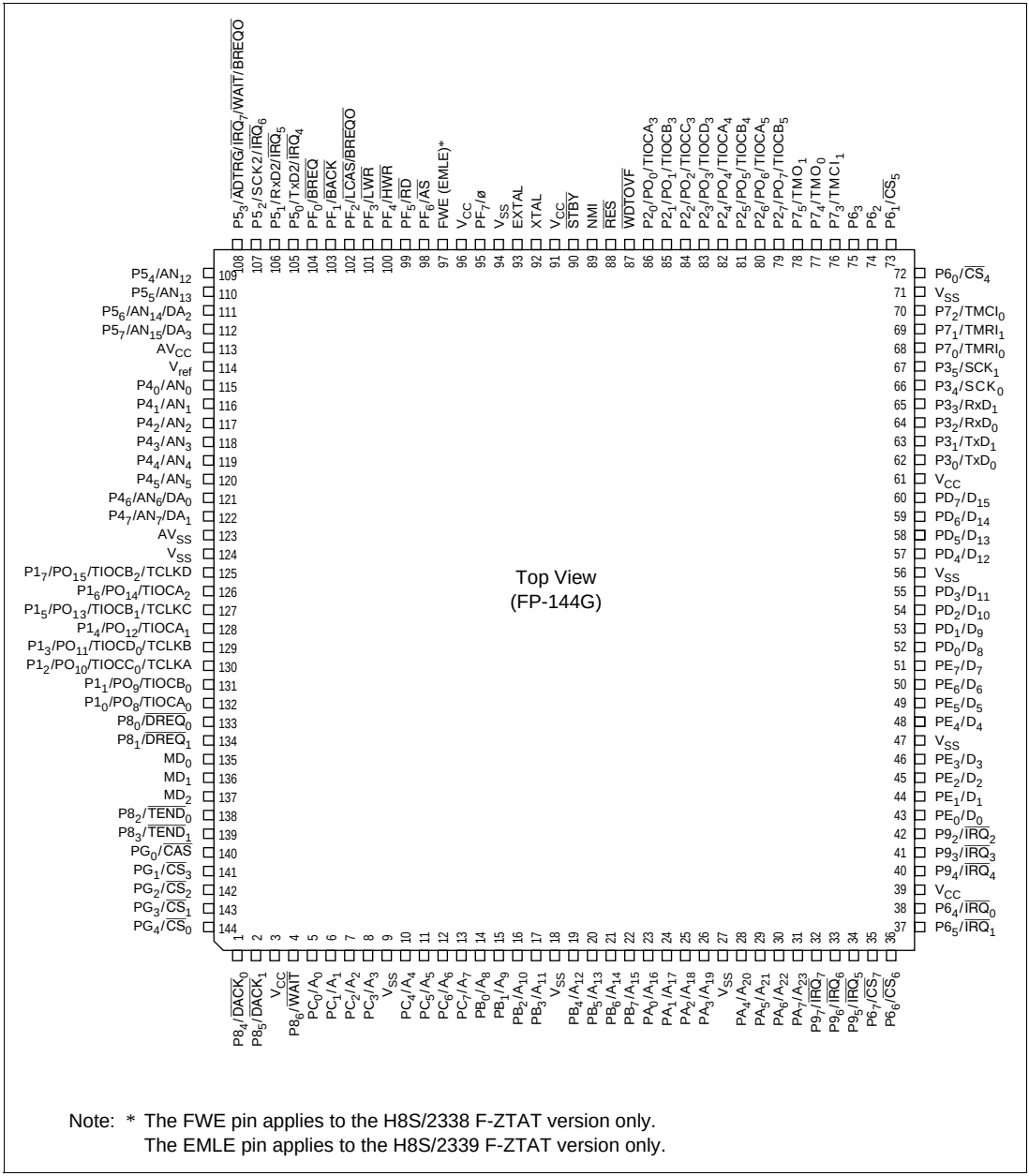


Notes: 1. ROM is not supported in the ROMless version.
2. The FWE pin applies to the H8S/2338 F-ZTAT version only.
The EMLE pin applies to the H8S/2339 F-ZTAT version only.

Figure 1.1 Internal Block Diagram

1.3 Pin Arrangement

Figure 1.2 shows the pin arrangement of the H8S/2339 and H8S/2338 Series.



Note: * The FWE pin applies to the H8S/2338 F-ZTAT version only.
The EMLE pin applies to the H8S/2339 F-ZTAT version only.

Figure 1.2 Pin Arrangement (TFP-144G: Top View)

1.4 Pin Functions in Each Operating Mode

Table 1.2 Pin Functions in Each Operating Mode

Pin No.	Pin Name				
FP-144	Mode 4*	Mode 5*	Mode 6	Mode 7	Flash Memory Programmer Mode
1	$P8_4/\overline{DACK_0}$	$P8_4/\overline{DACK_0}$	$P8_4/\overline{DACK_0}$	$P8_4/\overline{DACK_0}$	NC
2	$P8_5/\overline{DACK_1}$	$P8_5/\overline{DACK_1}$	$P8_5/\overline{DACK_1}$	$P8_5/\overline{DACK_1}$	NC
3	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
4	$P8_6/\overline{WAIT}$	$P8_6/\overline{WAIT}$	$P8_6/\overline{WAIT}$	$P8_6$	NC
5	A_0	A_0	PC_0/A_0	PC_0	A_0
6	A_1	A_1	PC_1/A_1	PC_1	A_1
7	A_2	A_2	PC_2/A_2	PC_2	A_2
8	A_3	A_3	PC_3/A_3	PC_3	A_3
9	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
10	A_4	A_4	PC_4/A_4	PC_4	A_4
11	A_5	A_5	PC_5/A_5	PC_5	A_5
12	A_6	A_6	PC_6/A_6	PC_6	A_6
13	A_7	A_7	PC_7/A_7	PC_7	A_7
14	A_8	A_8	PB_0/A_8	PB_0	A_8
15	A_9	A_9	PB_1/A_9	PB_1	A_9
16	A_{10}	A_{10}	PB_2/A_{10}	PB_2	A_{10}
17	A_{11}	A_{11}	PB_3/A_{11}	PB_3	A_{11}
18	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
19	A_{12}	A_{12}	PB_4/A_{12}	PB_4	A_{12}
20	A_{13}	A_{13}	PB_5/A_{13}	PB_5	A_{13}
21	A_{14}	A_{14}	PB_6/A_{14}	PB_6	A_{14}
22	A_{15}	A_{15}	PB_7/A_{15}	PB_7	A_{15}
23	A_{16}	A_{16}	PA_0/A_{16}	PA_0	A_{16}
24	A_{17}	A_{17}	PA_1/A_{17}	PA_1	A_{17}
25	A_{18}	A_{18}	PA_2/A_{18}	PA_2	A_{18}
26	A_{19}	A_{19}	PA_3/A_{19}	PA_3	NC
27	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}

Note: * Only modes 4 and 5 are provided in the ROMless version.

Pin No.	Pin Name				
FP-144	Mode 4*	Mode 5*	Mode 6	Mode 7	Flash Memory Programmer Mode
28	A_{20}	A_{20}	PA_4/A_{20}	PA_4	NC
29	PA_5/A_{21}	PA_5/A_{21}	PA_5/A_{21}	PA_5	NC
30	PA_6/A_{22}	PA_6/A_{22}	PA_6/A_{22}	PA_6	NC
31	PA_7/A_{23}	PA_7/A_{23}	PA_7/A_{23}	PA_7	NC
32	$P9_7/\overline{IRQ}_7$	$P9_7/\overline{IRQ}_7$	$P9_7/\overline{IRQ}_7$	$P9_7/\overline{IRQ}_7$	NC
33	$P9_6/\overline{IRQ}_6$	$P9_6/\overline{IRQ}_6$	$P9_6/\overline{IRQ}_6$	$P9_6/\overline{IRQ}_6$	NC
34	$P9_5/\overline{IRQ}_5$	$P9_5/\overline{IRQ}_5$	$P9_5/\overline{IRQ}_5$	$P9_5/\overline{IRQ}_5$	NC
35	$P6_7/\overline{CS}_7$	$P6_7/\overline{CS}_7$	$P6_7/\overline{CS}_7$	$P6_7$	NC
36	$P6_6/\overline{CS}_6$	$P6_6/\overline{CS}_6$	$P6_6/\overline{CS}_6$	$P6_6$	V_{CC}
37	$P6_5/\overline{IRQ}_1$	$P6_5/\overline{IRQ}_1$	$P6_5/\overline{IRQ}_1$	$P6_5/\overline{IRQ}_1$	V_{SS}
38	$P6_4/\overline{IRQ}_0$	$P6_4/\overline{IRQ}_0$	$P6_4/\overline{IRQ}_0$	$P6_4/\overline{IRQ}_0$	V_{SS}
39	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
40	$P9_4/\overline{IRQ}_4$	$P9_4/\overline{IRQ}_4$	$P9_4/\overline{IRQ}_4$	$P9_4/\overline{IRQ}_4$	NC
41	$P9_3/\overline{IRQ}_3$	$P9_3/\overline{IRQ}_3$	$P9_3/\overline{IRQ}_3$	$P9_3/\overline{IRQ}_3$	NC
42	$P9_2/\overline{IRQ}_2$	$P9_2/\overline{IRQ}_2$	$P9_2/\overline{IRQ}_2$	$P9_2/\overline{IRQ}_2$	NC
43	PE_0/D_0	PE_0/D_0	PE_0/D_0	PE_0	NC
44	PE_1/D_1	PE_1/D_1	PE_1/D_1	PE_1	NC
45	PE_2/D_2	PE_2/D_2	PE_2/D_2	PE_2	NC
46	PE_3/D_3	PE_3/D_3	PE_3/D_3	PE_3	NC
47	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
48	PE_4/D_4	PE_4/D_4	PE_4/D_4	PE_4	NC
49	PE_5/D_5	PE_5/D_5	PE_5/D_5	PE_5	NC
50	PE_6/D_6	PE_6/D_6	PE_6/D_6	PE_6	NC
51	PE_7/D_7	PE_7/D_7	PE_7/D_7	PE_7	NC
52	D_8	D_8	D_8	PD_0	I/O_0
53	D_9	D_9	D_9	PD_1	I/O_1
54	D_{10}	D_{10}	D_{10}	PD_2	I/O_2
55	D_{11}	D_{11}	D_{11}	PD_3	I/O_3
56	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}

Note: * Only modes 4 and 5 are provided in the ROMless version.

Pin No.	Pin Name				
FP-144	Mode 4*	Mode 5*	Mode 6	Mode 7	Flash Memory Programmer Mode
57	D_{12}	D_{12}	D_{12}	PD_4	I/O_4
58	D_{13}	D_{13}	D_{13}	PD_5	I/O_5
59	D_{14}	D_{14}	D_{14}	PD_6	I/O_6
60	D_{15}	D_{15}	D_{15}	PD_7	I/O_7
61	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
62	$P3_0/TxD_0$	$P3_0/TxD_0$	$P3_0/TxD_0$	$P3_0/TxD_0$	NC
63	$P3_1/TxD_1$	$P3_1/TxD_1$	$P3_1/TxD_1$	$P3_1/TxD_1$	NC
64	$P3_2/RxD_0$	$P3_2/RxD_0$	$P3_2/RxD_0$	$P3_2/RxD_0$	V_{CC}
65	$P3_3/RxD_1$	$P3_3/RxD_1$	$P3_3/RxD_1$	$P3_3/RxD_1$	NC
66	$P3_4/SCK_0$	$P3_4/SCK_0$	$P3_4/SCK_0$	$P3_4/SCK_0$	NC
67	$P3_5/SCK_1$	$P3_5/SCK_1$	$P3_5/SCK_1$	$P3_5/SCK_1$	NC
68	$P7_0/TMRI_0$	$P7_0/TMRI_0$	$P7_0/TMRI_0$	$P7_0/TMRI_0$	NC
69	$P7_1/TMRI_1$	$P7_1/TMRI_1$	$P7_1/TMRI_1$	$P7_1/TMRI_1$	NC
70	$P7_2/TMCI_0$	$P7_2/TMCI_0$	$P7_2/TMCI_0$	$P7_2/TMCI_0$	NC
71	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
72	$P6_0/\overline{CS}_4$	$P6_0/\overline{CS}_4$	$P6_0/\overline{CS}_4$	$P6_0$	NC
73	$P6_1/\overline{CS}_5$	$P6_1/\overline{CS}_5$	$P6_1/\overline{CS}_5$	$P6_1$	NC
74	$P6_2$	$P6_2$	$P6_2$	$P6_2$	NC
75	$P6_3$	$P6_3$	$P6_3$	$P6_3$	NC
76	$P7_3/TMCI_1$	$P7_3/TMCI_1$	$P7_3/TMCI_1$	$P7_3/TMCI_1$	NC
77	$P7_4/TMO_0$	$P7_4/TMO_0$	$P7_4/TMO_0$	$P7_4/TMO_0$	NC
78	$P7_5/TMO_1$	$P7_5/TMO_1$	$P7_5/TMO_1$	$P7_5/TMO_1$	NC
79	$P2_7/PO_7/TIOCB_5$	$P2_7/PO_7/TIOCB_5$	$P2_7/PO_7/TIOCB_5$	$P2_7/PO_7/TIOCB_5$	NC
80	$P2_6/PO_6/TIOCA_5$	$P2_6/PO_6/TIOCA_5$	$P2_6/PO_6/TIOCA_5$	$P2_6/PO_6/TIOCA_5$	NC
81	$P2_5/PO_5/TIOCB_4$	$P2_5/PO_5/TIOCB_4$	$P2_5/PO_5/TIOCB_4$	$P2_5/PO_5/TIOCB_4$	V_{SS}
82	$P2_4/PO_4/TIOCA_4$	$P2_4/PO_4/TIOCA_4$	$P2_4/PO_4/TIOCA_4$	$P2_4/PO_4/TIOCA_4$	$\overline{WE}$
83	$P2_3/PO_3/TIOCD_3$	$P2_3/PO_3/TIOCD_3$	$P2_3/PO_3/TIOCD_3$	$P2_3/PO_3/TIOCD_3$	$\overline{CE}$
84	$P2_2/PO_2/TIOCC_3$	$P2_2/PO_2/TIOCC_3$	$P2_2/PO_2/TIOCC_3$	$P2_2/PO_2/TIOCC_3$	$\overline{OE}$
85	$P2_1/PO_1/TIOCB_3$	$P2_1/PO_1/TIOCB_3$	$P2_1/PO_1/TIOCB_3$	$P2_1/PO_1/TIOCB_3$	NC

Note: * Only modes 4 and 5 are provided in the ROMless version.

Pin No.	Pin Name				
FP-144	Mode 4*[1]	Mode 5*[1]	Mode 6	Mode 7	Flash Memory Programmer Mode
86	$P2_0/PO_0/TIOCA_3$	$P2_0/PO_0/TIOCA_3$	$P2_0/PO_0/TIOCA_3$	$P2_0/PO_0/TIOCA_3$	NC
87	$\overline{WDTOVF}$	$\overline{WDTOVF}$	$\overline{WDTOVF}$	$\overline{WDTOVF}$	NC
88	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$
89	NMI	NMI	NMI	NMI	V_{CC}
90	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	V_{CC}
91	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
92	XTAL	XTAL	XTAL	XTAL	XTAL
93	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL
94	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
95	$PF_7/ø$	$PF_7/ø$	$PF_7/ø$	$PF_7/ø$	NC
96	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
97	FWE (EMLE)*[2]	FWE (EMLE)*[2]	FWE (EMLE)*[2]	FWE (EMLE)*[2]	FWE (EMLE)*[2]
98	$PF_6/\overline{AS}$	$PF_6/\overline{AS}$	$PF_6/\overline{AS}$	PF_6	NC
99	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	PF_5	NC
100	$\overline{HWR}$	$\overline{HWR}$	$\overline{HWR}$	PF_4	NC
101	$PF_3/\overline{LWR}$	$PF_3/\overline{LWR}$	$PF_3/\overline{LWR}$	PF_3	NC
102	$PF_2/\overline{LCAS}/\overline{BREQO}$	$PF_2/\overline{LCAS}/\overline{BREQO}$	$PF_2/\overline{LCAS}/\overline{BREQO}$	PF_2	NC
103	$PF_1/\overline{BACK}$	$PF_1/\overline{BACK}$	$PF_1/\overline{BACK}$	PF_1	NC
104	$PF_0/\overline{BREQ}$	$PF_0/\overline{BREQ}$	$PF_0/\overline{BREQ}$	PF_0	NC
105	$P5_0/TxD_2/\overline{IRQ_4}$	$P5_0/TxD_2/\overline{IRQ_4}$	$P5_0/TxD_2/\overline{IRQ_4}$	$P5_0/TxD_2/\overline{IRQ_4}$	NC
106	$P5_1/RxD_2/\overline{IRQ_5}$	$P5_1/RxD_2/\overline{IRQ_5}$	$P5_1/RxD_2/\overline{IRQ_5}$	$P5_1/RxD_2/\overline{IRQ_5}$	NC
107	$P5_2/SCK_2/\overline{IRQ_6}$	$P5_2/SCK_2/\overline{IRQ_6}$	$P5_2/SCK_2/\overline{IRQ_6}$	$P5_2/SCK_2/\overline{IRQ_6}$	NC
108	$P5_3/\overline{ADTRG}/\overline{IRQ_7}/\overline{WAIT}/\overline{BREQO}$	$P5_3/\overline{ADTRG}/\overline{IRQ_7}/\overline{WAIT}/\overline{BREQO}$	$P5_3/\overline{ADTRG}/\overline{IRQ_7}/\overline{WAIT}/\overline{BREQO}$	$P5_3/\overline{ADTRG}/\overline{IRQ_7}$	NC
109	$P5_4/AN_{12}$	$P5_4/AN_{12}$	$P5_4/AN_{12}$	$P5_4/AN_{12}$	NC
110	$P5_5/AN_{13}$	$P5_5/AN_{13}$	$P5_5/AN_{13}$	$P5_5/AN_{13}$	NC
111	$P5_6/AN_{14}/DA_2$	$P5_6/AN_{14}/DA_2$	$P5_6/AN_{14}/DA_2$	$P5_6/AN_{14}/DA_2$	NC
112	$P5_7/AN_{15}/DA_3$	$P5_7/AN_{15}/DA_3$	$P5_7/AN_{15}/DA_3$	$P5_7/AN_{15}/DA_3$	NC

Notes: 1. Only modes 4 and 5 are provided in the ROMless version.

2. The FWE pin applies to the H8S/2338 F-ZTAT version only. The EMLE pin applies to the H8S/2339 F-ZTAT version only.

Pin No.	Pin Name				
FP-144	Mode 4*	Mode 5*	Mode 6	Mode 7	Flash Memory Programmer Mode
113	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	V_{CC}
114	V_{ref}	V_{ref}	V_{ref}	V_{ref}	V_{CC}
115	$P4_0/AN_0$	$P4_0/AN_0$	$P4_0/AN_0$	$P4_0/AN_0$	NC
116	$P4_1/AN_1$	$P4_1/AN_1$	$P4_1/AN_1$	$P4_1/AN_1$	NC
117	$P4_2/AN_2$	$P4_2/AN_2$	$P4_2/AN_2$	$P4_2/AN_2$	NC
118	$P4_3/AN_3$	$P4_3/AN_3$	$P4_3/AN_3$	$P4_3/AN_3$	NC
119	$P4_4/AN_4$	$P4_4/AN_4$	$P4_4/AN_4$	$P4_4/AN_4$	NC
120	$P4_5/AN_5$	$P4_5/AN_5$	$P4_5/AN_5$	$P4_5/AN_5$	NC
121	$P4_6/AN_6/DA_0$	$P4_6/AN_6/DA_0$	$P4_6/AN_6/DA_0$	$P4_6/AN_6/DA_0$	NC
122	$P4_7/AN_7/DA_1$	$P4_7/AN_7/DA_1$	$P4_7/AN_7/DA_1$	$P4_7/AN_7/DA_1$	NC
123	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	V_{SS}
124	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
125	$P1_7/PO_{15}$/ $TIOCB_2/TCLKD$	$P1_7/PO_{15}$/ $TIOCB_2/TCLKD$	$P1_7/PO_{15}$/ $TIOCB_2/TCLKD$	$P1_7/PO_{15}$/ $TIOCB_2/TCLKD$	NC
126	$P1_6/PO_{14}$/ $TIOCA_2$	$P1_6/PO_{14}$/ $TIOCA_2$	$P1_6/PO_{14}$/ $TIOCA_2$	$P1_6/PO_{14}$/ $TIOCA_2$	NC
127	$P1_5/PO_{13}$/ $TIOCB_1/TCLKC$	$P1_5/PO_{13}$/ $TIOCB_1/TCLKC$	$P1_5/PO_{13}$/ $TIOCB_1/TCLKC$	$P1_5/PO_{13}$/ $TIOCB_1/TCLKC$	NC
128	$P1_4/PO_{12}$/ $TIOCA_1$	$P1_4/PO_{12}$/ $TIOCA_1$	$P1_4/PO_{12}$/ $TIOCA_1$	$P1_4/PO_{12}$/ $TIOCA_1$	NC
129	$P1_3/PO_{11}$/ $TIOCD_0/TCLKB$	$P1_3/PO_{11}$/ $TIOCD_0/TCLKB$	$P1_3/PO_{11}$/ $TIOCD_0/TCLKB$	$P1_3/PO_{11}$/ $TIOCD_0/TCLKB$	NC
130	$P1_2/PO_{10}$/ $TIOCC_0/TCLKA$	$P1_2/PO_{10}$/ $TIOCC_0/TCLKA$	$P1_2/PO_{10}$/ $TIOCC_0/TCLKA$	$P1_2/PO_{10}$/ $TIOCC_0/TCLKA$	NC
131	$P1_1/PO_9/TIOCB_0$	$P1_1/PO_9/TIOCB_0$	$P1_1/PO_9/TIOCB_0$	$P1_1/PO_9/TIOCB_0$	NC
132	$P1_0/PO_8/TIOCA_0$	$P1_0/PO_8/TIOCA_0$	$P1_0/PO_8/TIOCA_0$	$P1_0/PO_8/TIOCA_0$	NC
133	$P8_0/\overline{DREQ}_0$	$P8_0/\overline{DREQ}_0$	$P8_0/\overline{DREQ}_0$	$P8_0/\overline{DREQ}_0$	NC
134	$P8_1/\overline{DREQ}_1$	$P8_1/\overline{DREQ}_1$	$P8_1/\overline{DREQ}_1$	$P8_1/\overline{DREQ}_1$	NC
135	MD_0	MD_0	MD_0	MD_0	V_{SS}
136	MD_1	MD_1	MD_1	MD_1	V_{SS}

Note: * Only modes 4 and 5 are provided in the ROMless version.

Pin No.	Pin Name				
FP-144	Mode 4*	Mode 5*	Mode 6	Mode 7	Flash Memory Programmer Mode
137	MD_2	MD_2	MD_2	MD_2	V_{SS}
138	$P8_2/\overline{TEND}_0$	$P8_2/\overline{TEND}_0$	$P8_2/\overline{TEND}_0$	$P8_2/\overline{TEND}_0$	NC
139	$P8_3/\overline{TEND}_1$	$P8_3/\overline{TEND}_1$	$P8_3/\overline{TEND}_1$	$P8_3/\overline{TEND}_1$	NC
140	$PG_0/\overline{CAS}$	$PG_0/\overline{CAS}$	$PG_0/\overline{CAS}$	PG_0	NC
141	$PG_1/\overline{CS}_3$	$PG_1/\overline{CS}_3$	$PG_1/\overline{CS}_3$	PG_1	NC
142	$PG_2/\overline{CS}_2$	$PG_2/\overline{CS}_2$	$PG_2/\overline{CS}_2$	PG_2	NC
143	$PG_3/\overline{CS}_1$	$PG_3/\overline{CS}_1$	$PG_3/\overline{CS}_1$	PG_3	NC
144	$PG_4/\overline{CS}_0$	$PG_4/\overline{CS}_0$	$PG_4/\overline{CS}_0$	PG_4	NC

Note: * Only modes 4 and 5 are provided in the ROMless version.

1.5 Pin Functions

Table 1.3 Pin Functions

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Power	V_{CC}	3, 39, 61, 91, 96	Input	**Power supply:** For connection to the power supply. All V_{CC} pins should be connected to the system power supply.
	V_{SS}	9, 18, 27, 47, 56, 71, 94, 124	Input	**Ground:** For connection to ground (0 V). All V_{SS} pins should be connected to the system power supply (0 V).
Clock	XTAL	92	Input	Connects to a crystal resonator. See section 18, Clock Pulse Generator, in the Hardware Manual, for typical connection diagrams for a crystal resonator and external clock input.
	EXTAL	93	Input	Connects to a crystal resonator. The EXTAL pin can also input an external clock. See section 18, Clock Pulse Generator, in the Hardware Manual, for typical connection diagrams for a crystal resonator and external clock input.
	ø	95	Output	**System clock:** Supplies the system clock to an external device.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Operating mode control	MD_2 to MD_0	137 to 135	Input	**Mode pins:** These pins set the operating mode. The relation between the settings of pins MD_2 to MD_0 and the operating mode is shown below. These pins should not be changed while the chip is operating.

H8S/2338 F-ZTAT version:

FWE	MD_2	MD_1	MD_0	Operating Mode
0	0	0	0	—
			1	—
		1	0	—
			1	—
	1	0	0	Mode 4
			1	Mode 5
		1	0	Mode 6
			1	Mode 7
1	0	0	0	—
			1	—
		1	0	Mode 10
			1	Mode 11
	1	0	0	—
			1	—
		1	0	Mode 14
			1	Mode 15

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Operating mode control	MD_2 to MD_0	137 to 135	Input	H8S/2339 F-ZTAT version, Mask ROM, and ROMless versions:

MD_2	MD_1	MD_0	Operating Mode
0	0	0	—
		1	—
	1	0	—
		1	—
1	0	0	Mode 4
		1	Mode 5
	1	0	Mode 6*
		1	Mode 7*

Note: * Modes 6 and 7 are not provided in the ROMless version.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
System control	$\overline{RES}$	88	Input	**Reset input:** When this pin is driven low, the chip is reset.
	$\overline{STBY}$	90	Input	**Standby:** When this pin is driven low, a transition is made to hardware standby mode.
	$\overline{BREQ}$	104	Input	**Bus request:** Used by an external bus master to issue a bus request to the chip.
	$\overline{BREQO}$	102,108	Output	**Bus request output:** The external bus request signal used when an internal bus master accesses external space in the external bus-released state.
	$\overline{BACK}$	103	Output	**Bus request acknowledge:** Indicates that the bus has been released to an external bus master.
	FWE*[1]	97	Input	**Flash write enable:** Enables/disables flash memory programming. In the mask ROM version and ROMless versions, connect this pin to ground.
	EMLE*[2]	97	Input	**Emulator enable:** For connection to ground (0 V).

Notes: 1. Applies to the H8S/2338 F-ZTAT version only.
2. Applies to the H8S/2339 F-ZTAT version only.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Interrupts	NMI	89	Input	**Nonmaskable interrupt:** Requests a nonmaskable interrupt. When this pin is not used, it should be fixed high.
	$\overline{IRQ}_7$ to $\overline{IRQ}_0$	32 to 34, 40 to 42, 37, 38 108 to 105	Input	**Interrupt request 7 to 0:** These pins request a maskable interrupt.
Address bus	A_{23} to A_0	31 to 28, 26 to 19, 17 to 10, 8 to 5	Output	**Address bus:** These pins output an address.
Data bus	D_{15} to D_0	60 to 57, 55 to 48, 46 to 43	I/O	**Data bus:** These pins constitute a bidirectional data bus.
Bus control	$\overline{CS}_7$ to $\overline{CS}_0$	35, 36, 61, 60, 141 to 144	Output	**Chip select:** Signals for selecting areas 7 to 0.
	$\overline{AS}$	98	Output	**Address strobe:** When this pin is low, it indicates that address output on the address bus is enabled.
	$\overline{RD}$	99	Output	**Read:** When this pin is low, it indicates that the external address space can be read.
	$\overline{HWR}$	100	Output	**High write/write enable:** A strobe signal that writes to external space and indicates that the upper half (D_{15} to D_8) of the data bus is enabled. The 2-CAS type DRAM write enable signal.
	$\overline{LWR}$	101	Output	**Low write:** A strobe signal that writes to external space and indicates that the lower half (D_7 to D_0) of the data bus is enabled.
	$\overline{CAS}$	140	Output	**Upper column address strobe/column address strobe:** The 2-CAS type DRAM upper column address strobe signal.
	$\overline{LCAS}$	102	Output	**Lower column address strobe:** The 2-CAS type DRAM lower column address strobe signal.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Bus control	$\overline{WAIT}$	4,108	Input	**Wait:** Requests insertion of a wait state in the bus cycle when accessing external 3-state address space.
DMA controller (DMAC)	$\overline{DREQ}_1$, $\overline{DREQ}_0$	134,133	Input	**DMA request 1 and 0:** These pins request DMAC activation.
	$\overline{TEND}_1$, $\overline{TEND}_0$	139,138	Output	**DMA transfer end 1 and 0:** These pins indicate the end of DMAC data transfer.
	$\overline{DACK}_1$, $\overline{DACK}_0$	2,1	Output	**DMA transfer acknowledge 1 and 0:** These are the DMAC single address transfer acknowledge pins.
16-bit timer pulse unit (TPU)	TCLKD to TCLKA	125, 127, 129, 130	Input	**Clock input D to A:** These pins input an external clock.
	$TIOCA_0$, $TIOCB_0$, $TIOCC_0$, $TIOCD_0$	132 to 129	I/O	**Input capture/output compare match A0 to D0:** The TGR0A to TGR0D input capture input or output compare output, or PWM output pins.
	$TIOCA_1$, $TIOCB_1$	128, 127	I/O	**Input capture/output compare match A1 and B1:** The TGR1A and TGR1B input capture input or output compare output, or PWM output pins.
	$TIOCA_2$, $TIOCB_2$	126, 125	I/O	**Input capture/output compare match A2 and B2:** The TGR2A and TGR2B input capture input or output compare output, or PWM output pins.
	$TIOCA_3$, $TIOCB_3$, $TIOCC_3$, $TIOCD_3$	86 to 83	I/O	**Input capture/output compare match A3 to D3:** The TGR3A to TGR3D input capture input or output compare output, or PWM output pins.
	$TIOCA_4$, $TIOCB_4$	82, 81	I/O	**Input capture/output compare match A4 and B4:** The TGR4A and TGR4B input capture input or output compare output, or PWM output pins.
	$TIOCA_5$, $TIOCB_5$	80, 79	I/O	**Input capture/output compare match A5 and B5:** The TGR5A and TGR5B input capture input or output compare output, or PWM output pins.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Programmable pulse generator (PPG)	PO_{15} to PO_0	125 to 132, 79 to 86	Output	**Pulse output 15 to 0:** Pulse output pins.
8-bit timer	TMO_0, TMO_1	77, 78	Output	**Compare match output:** The compare match output pins.
	$TMCI_0$, $TMCI_1$	70, 76	Input	**Counter external clock input:** Input pins for the external clock input to the counter.
	$TMRI_0$, $TMRI_1$	68, 69	Input	**Counter external reset input:** The counter reset input pins.
Watchdog timer (WDT)	$\overline{WDTOVF}$	87	Output	**Watchdog timer overflow:** The counter overflow signal output pin in watchdog timer mode.
Serial communication interface (SCI)/ smart card interface	TxD_2, TxD_1, TxD_0	105, 63, 62	Output	**Transmit data (channel 0, 1, 2):** Data output pins.
	RxD_2, RxD_1, RxD_0	106, 65, 64	Input	**Receive data (channel 0, 1, 2):** Data input pins.
	SCK_2, SCK_1, SCK_0	107, 67, 66	I/O	**Serial clock (channel 0, 1, 2):** Clock I/O pins.
A/D converter	AN_{15} to AN_{12}, AN_7 to AN_0	112 to 109, 122 to 115	Input	**Analog 15 to 12, and 7 to 0:** Analog input pins.
	$\overline{ADTRG}$	108	Input	**A/D conversion external trigger input:** Pin for input of an external trigger to start A/D conversion.
D/A converter	DA_3, DA_2, DA_1, DA_0	112, 111, 122, 121	Output	**Analog output:** D/A converter analog output pins.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
A/D converter and D/A converter	AV_{CC}	113	Input	This is the power supply pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (+3 V).
	AV_{SS}	123	Input	This is the ground pin for the A/D converter and D/A converter. This pin should be connected to the system power supply (0 V).
	V_{ref}	114	Input	This is the reference voltage input pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (+3 V).
I/O ports	$P1_7$ to $P1_0$	125 to 132	I/O	**Port 1:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port 1 data direction register (P1DDR).
	$P2_7$ to $P2_0$	79 to 86	I/O	**Port 2:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port 2 data direction register (P2DDR).
	$P3_5$ to $P3_0$	67 to 62	I/O	**Port 3:** A 6-bit I/O port. Input or output can be designated for each bit by means of the port 3 data direction register (P3DDR).
	$P4_7$ to $P4_0$	122 to 115	Input	**Port 4:** An 8-bit input port.
	$P5_7$ to $P5_0$	112 to 109, 108 to 105	Input I/O	**Port 5:** A 4-bit input port and a 4-bit I/O port. For $P5_3$ to $P5_0$, input or output can be designated for each bit by means of the port 5 data direction register (P5DDR).
	$P6_7$ to $P6_0$	35 to 38, 75 to 72	I/O	**Port 6:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port 6 data direction register (P6DDR).
	$P7_5$ to $P7_0$	78 to 76, 70 to 68	I/O	**Port 7:** A 6-bit I/O port. Input or output can be designated for each bit by means of the port 7 data direction register (P7DDR).
	$P8_6$ to $P8_0$	4, 2, 1, 139, 138, 134, 133	I/O	**Port 8:** A 7-bit I/O port. Input or output can be designated for each bit by means of the port 8 data direction register (P8DDR).

Type	Symbol	Pin No. FP-144	I/O	Name and Function
I/O ports	$P9_7$ to $P9_2$	32 to 34, 40 to 42	I/O	**Port 9:** A 6-bit I/O port. Input or output can be designated for each bit by means of the port 9 data direction register (P9DDR).
	PA_7 to PA_0	31 to 28, 26 to 23	I/O	**Port A:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port A data direction register (PADDR).
	PB_7 to PB_0	22 to 19, 17 to 14	I/O	**Port B:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port B data direction register (PBDDR).
	PC_7 to PC_0	13 to 10, 8 to 5	I/O	**Port C:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port C data direction register (PCDDR).
	PD_7 to PD_0	60 to 57, 55 to 52	I/O	**Port D:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port D data direction register (PDDDR).
	PE_7 to PE_0	51 to 48, 46 to 43	I/O	**Port E:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port E data direction register (PEDDR).
	PF_7 to PF_0	95, 98 to 104	I/O	**Port F:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port F data direction register (PFDDR).
	PG_4 to PG_0	144 to 140	I/O	**Port G:** A 5-bit I/O port. Input or output can be designated for each bit by means of the port G data direction register (PGDDR).

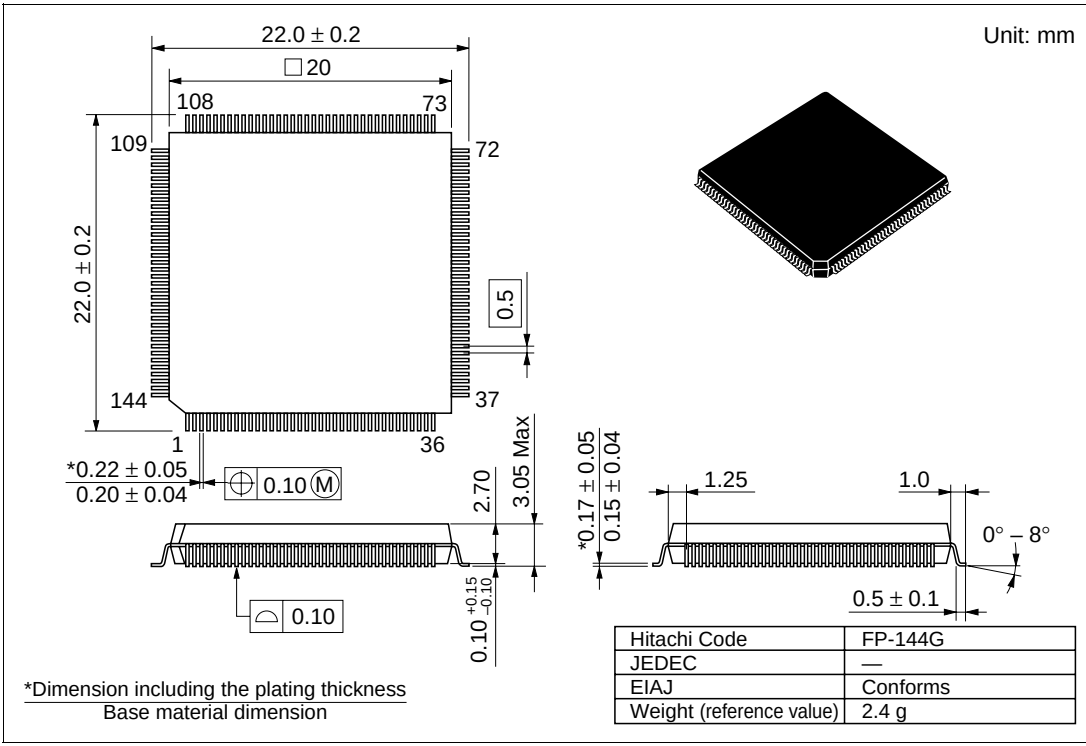
1.6 Product Lineup

Table 1.4 H8S/2339, H8S/2338 Series Product Lineup

Product Type		Model	Marking	Package (Hitachi Package Code)
H8S/2339*	F-ZTAT™ version	HD64F2339	HD64F2339VFC	144-pin QFP (FP-144G)
H8S/2338	Mask ROM version	HD6432338	HD6432338FC	144-pin QFP (FP-144G)
	F-ZTAT™ version	HD64F2338	HD64F2338VFC	144-pin QFP (FP-144G)
H8S/2337	Mask ROM version	HD6432337	HD6432337FC	144-pin QFP (FP-144G)
H8S/2332	ROMless version	HD6412332	HD6412332VFC	144-pin QFP (FP-144G)

Note: * Under development

1.7 Package Dimensions



Hitachi Code	FP-144G
JEDEC	—
EIAJ	Conforms
Weight (reference value)	2.4 g

Figure 1.3 FP-144G Package Dimensions

Section 2 MCU Operating Modes

2.1 Overview

2.1.1 Operating Mode Selection (H8S/2338 F-ZTAT Version)

This version has eight operating modes (modes 4 to 7, 10, 11, 14 and 15). These modes are determined by the mode pin (MD_2 to MD_0) and flash write enable pin (FWE) settings. The CPU operating mode and initial bus width can be selected as shown in table 2.1.

Table 2.1 lists the MCU operating modes.

Table 2.1 MCU Operating Mode Selection (H8S/2338 F-ZTAT Version)

MCU Operating Mode	FWE	MD_2	MD_1	MD_0	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
								Initial Value	Max. Value
0	0	0	0	0	—	—	—	—	—
1				1					
2			1	0					
3				1					
4		1	0	0	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
5				1				8 bits	16 bits
6			1	0		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
7				1		Single-chip mode		—	—
8	1	0	0	0	—	—	—	—	—
9				1					
10			1	0	Advanced	Boot mode	Enabled	8 bits	16 bits
11				1				—	—
12		1	0	0	—	—	—	—	—
13				1					
14			1	0	Advanced	User program mode	Enabled	8 bits	16 bits
15				1				—	—

The CPU's architecture allows for 4 Gbytes of address space, but this version actually accesses a maximum of 16 Mbytes.

Modes 4 to 6 are externally expanded modes that allow access to external memory and peripheral devices.

The external expansion modes allow switching between 8-bit and 16-bit bus modes. After program execution starts, an 8-bit or 16-bit address space can be set for each area, depending on the bus controller setting. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. Note that the functions of each pin depend on the operating mode.

Modes 10, 11, 14, and 15 are boot modes and user program modes in which the flash memory can be programmed and erased. For details, see section 17, ROM, in the Hardware Manual

This version can only be used in modes 4 to 7, 10, 11, 14, and 15. This means that the flash write enable pin and mode pins must be set to select one of these modes.

Do not change the inputs at the mode pins during operation.

2.1.2 Operating Mode Selection (H8S/2339 F-ZTAT Version, Mask ROM, and ROMless Versions)

These versions have four operating modes (modes 4 to 7). The operating mode is determined by the mode pins (MD_2 to MD_0). The CPU operating mode, enabling or disabling of on-chip ROM, and the initial bus width setting can be selected as shown in table 2.2.

Table 2.2 lists the MCU operating modes.

Table 2.2 MCU Operating Mode Selection (H8S/2339 F-ZTAT Version, Mask ROM, and ROMless Versions)

MCU Operating Mode	MD_2	MD_1	MD_0	CPU Operating Mode	Description	On-Chip ROM	External Data Bus Initial Value	External Data Bus Max. Value
0	0	0	0	—	—	—	—	—
1			1					
2		1	0					
3			1					
4*	1	0	0	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
5*			1				8 bits	16 bits
6		1	0		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
7			1		Single-chip mode		—	—

Note: * Only modes 4 and 5 are provided in the ROMless version.

The CPU's architecture allows for 4 Gbytes of address space, but these versions actually access a maximum of 16 Mbytes.

Modes 4 to 6 are externally expanded modes that allow access to external memory and peripheral devices.

The external expansion modes allow switching between 8-bit and 16-bit bus modes. After program execution starts, an 8-bit or 16-bit address space can be set for each area, depending on the bus controller setting. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. Note that the functions of each pin depend on the operating mode.

These versions can only be used in modes 4 to 7. This means that the mode pins must be set to select one of these modes. However, note that only mode 4 or 5 can be set for the ROMless version.

Do not change the inputs at the mode pins during operation.

2.1.3 Register Configuration

The H8S/2339 and H8S/2338 Series have a mode control register (MDCR) that indicates the inputs at the mode pins (MD_2 to MD_0), and a system control register (SYSCR) and system control register 2 (SYSCR2)*[2] that control the operation of the chip. Table 2.3 summarizes these registers.

Table 2.3 Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Mode control register	MDCR	R	Undefined	H'FF3B
System control register	SYSCR	R/W	H'01	H'FF39
System control register 2*[2]	SYSCR2	R/W	H'00	H'FF42

Notes: 1. Lower 16 bits of the address.

2. The SYSCR2 register can only be used in the F-ZTAT version. In the mask ROM and ROMless versions this register will return an undefined value if read, and cannot be modified.

2.2 Register Descriptions

2.2.1 Mode Control Register (MDCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	:	1	0	0	0	0	—*	—*	—*
R/W	:	—	—	—	—	—	R	R	R

Note: * Determined by pins MD_2 to MD_0.

MDCR is an 8-bit read-only register that indicates the current operating mode of the H8S/2338 Series chip.

Bit 7—Reserved: This bit is always read as 1, and cannot be modified.

Bits 6 to 3—Reserved: These bits are always read as 0, and cannot be modified.

Bits 2 to 0—Mode Select 2 to 0 (MDS2 to MDS0): These bits indicate the input levels at pins MD_2 to MD_0 (the current operating mode). Bits MDS2 to MDS0 correspond to pins MD_2 to MD_0. MDS2 to MDS0 are read-only bits, and cannot be written to. The mode pin (MD_2 to MD_0) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

2.2.2 System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7—Reserved: Only 0 should be written to this bit.

Bit 6—Reserved: This bit is always read as 0, and cannot be modified.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select the control mode of the interrupt controller. For details of the interrupt control modes, see section 3.4.1, Interrupt Control Modes and Interrupt Operation, in the Hardware Manual.

Bit 5 INTM1	Bit 4 INTM0	Interrupt Control Mode	Description	
0	0	0	Control of interrupts by I bit	(Initial value)
	1	—	Setting prohibited	
1	0	2	Control of interrupts by I2 to I0 bits and IPR	
	1	—	Setting prohibited	

Bit 3—NMI Edge Select (NMIEG): Selects the valid edge of the NMI interrupt input.

Bit 3 NMIEG	Description	
0	An interrupt is requested at the falling edge of NMI input	(Initial value)
1	An interrupt is requested at the rising edge of NMI input	

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{\text{LWR}}$ output.

Bit 2 LWROD	Description	
0	PF_3 is designated as $\overline{\text{LWR}}$ output pin	(Initial value)
1	PF_3 is designated as I/O port, and does not function as $\overline{\text{LWR}}$ output pin	

Bit 1—IRQ Port Switching Select (IRQPAS): Selects switching of input pins for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$. $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input is always performed from one of the ports.

Bit 1 IRQPAS	Description	
0	$P9_4$ to $P9_7$ are used for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input	(Initial value)
1	$P5_3$ to $P5_0$ are used for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input	

Bit 0—RAM Enable (RAME): Enables or disables the on-chip RAM. The RAME bit is initialized when the reset state is released. It is not initialized in software standby mode.

Bit 0 RAME	Description	
0	On-chip RAM is disabled	
1	On-chip RAM is enabled	(Initial value)

2.2.3 System Control Register 2 (SYSCR2) (F-ZTAT Version Only)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	FLSHE	—	—	—
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	—	—	—	—	R/W	—	—	—

SYSCR2 is an 8-bit readable/writable register that performs on-chip flash memory control.

SYSCR2 is initialized to H'00 by a reset, and in hardware standby mode.

Bits 7 to 4—Reserved: These bits are always read as 0, and cannot be modified.

Bit 3—Flash Memory Control Register Enable (FLSHE): Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). For details, see section 17, ROM, in the Hardware Manual.

Bit 3 FLSHE	Description
0	Flash control registers are not selected for addresses H'FFFFC8 to H'FFFFCB (Initial value)
1	Flash control registers are selected for addresses H'FFFFC8 to H'FFFFCB

Bits 2 to 0—Reserved: These bits are always read as 0, and cannot be modified.

2.3 Operating Mode Descriptions

2.3.1 Modes 1 to 3

Modes 1 to 3 are not supported in the H8S/2339 and H8S/2338 Series, and must not be set.

2.3.2 Mode 4 (Expanded Mode with On-Chip ROM Disabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Ports A, B, and C function as an address bus, port D functions as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. However, note that if 8-bit access is designated by the bus controller for all areas, the bus mode switches to 8 bits.

2.3.3 Mode 5 (Expanded Mode with On-Chip ROM Disabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Ports A, B and C function as an address bus, port D functions as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. However, note that if at least one area is designated for 16-bit access by the bus controller, the bus mode switches to 16 bits and port E becomes a data bus.

2.3.4 Mode 6 (Expanded Mode with On-Chip ROM Enabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled.

Ports A, B, and C function as input ports immediately after a reset. These pins can be set to output addresses by setting the corresponding data direction register (DDR) bits to 1. Port D functions as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. However, note that if at least one area is designated for 16-bit access by the bus controller, the bus mode switches to 16 bits and port E becomes a data bus.

2.3.5 Mode 7 (Single-Chip Mode)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled, but external addresses cannot be accessed.

All I/O ports are available for use as input/output ports.

2.3.6 Modes 8 and 9

Modes 8 and 9 are not supported and must not be set.

2.3.7 Mode 10 (H8S/2338 F-ZTAT Version Only)

This is a flash memory boot mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced expanded mode with on-chip ROM enabled.

2.3.8 Mode 11 (H8S/2338 F-ZTAT Version Only)

This is a flash memory boot mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced single-chip mode.

2.3.9 Modes 12 and 13

Modes 12 and 13 are not supported and must not be set.

2.3.10 Mode 14 (H8S/2338 F-ZTAT Version Only)

This is a flash memory user program mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced expanded mode with on-chip ROM enabled.

2.3.11 Mode 15 (H8S/2338 F-ZTAT Version Only)

This is a flash memory user program mode. For details, see section 17, ROM, in the Hardware Manual.

Except for the fact that flash memory programming and erasing can be performed, operation in this mode is the same as in advanced single-chip mode.

2.4 Pin Functions in Each Operating Mode

The pin functions of ports A to F vary depending on the operating mode. Table 2.4 shows their functions in each operating mode.

Table 2.4 Pin Functions in Each Mode

Port		Mode 4	Mode 5	Mode 6	Mode 7	Mode 10	Mode 11	Mode 14	Mode 15
Port A	PA_7 to PA_5	P*/A	P*/A	P*/A	P	P*/A	P	P*/A	P
	PA_4 to PA_0	A	A						
Port B		A	A	P*/A	P	P*/A	P	P*/A	P
Port C		A	A	P*/A	P	P*/A	P	P*/A	P
Port D		D	D	D	P	D	P	D	P
Port E		P/D*	P*/D	P*/D	P	P*/D	P	P*/D	P
Port F	PF_7	P/C*	P/C*	P/C*	P*/C	P/C*	P*/C	P/C*	P*/C
	PF_6	P/C*	P/C*	P/C*	P	P/C*	P	P/C*	P
	PF_5 to PF_4	C	C	C		C		C	
	PF_3	P/C*	P/C*	P/C*		P/C*		P/C*	
	PF_2 to PF_0	P*/C	P*/C	P*/C		P*/C		P*/C	

Legend

P: I/O port

A: Address bus output

D: Data bus I/O

C: Control signals, clock I/O

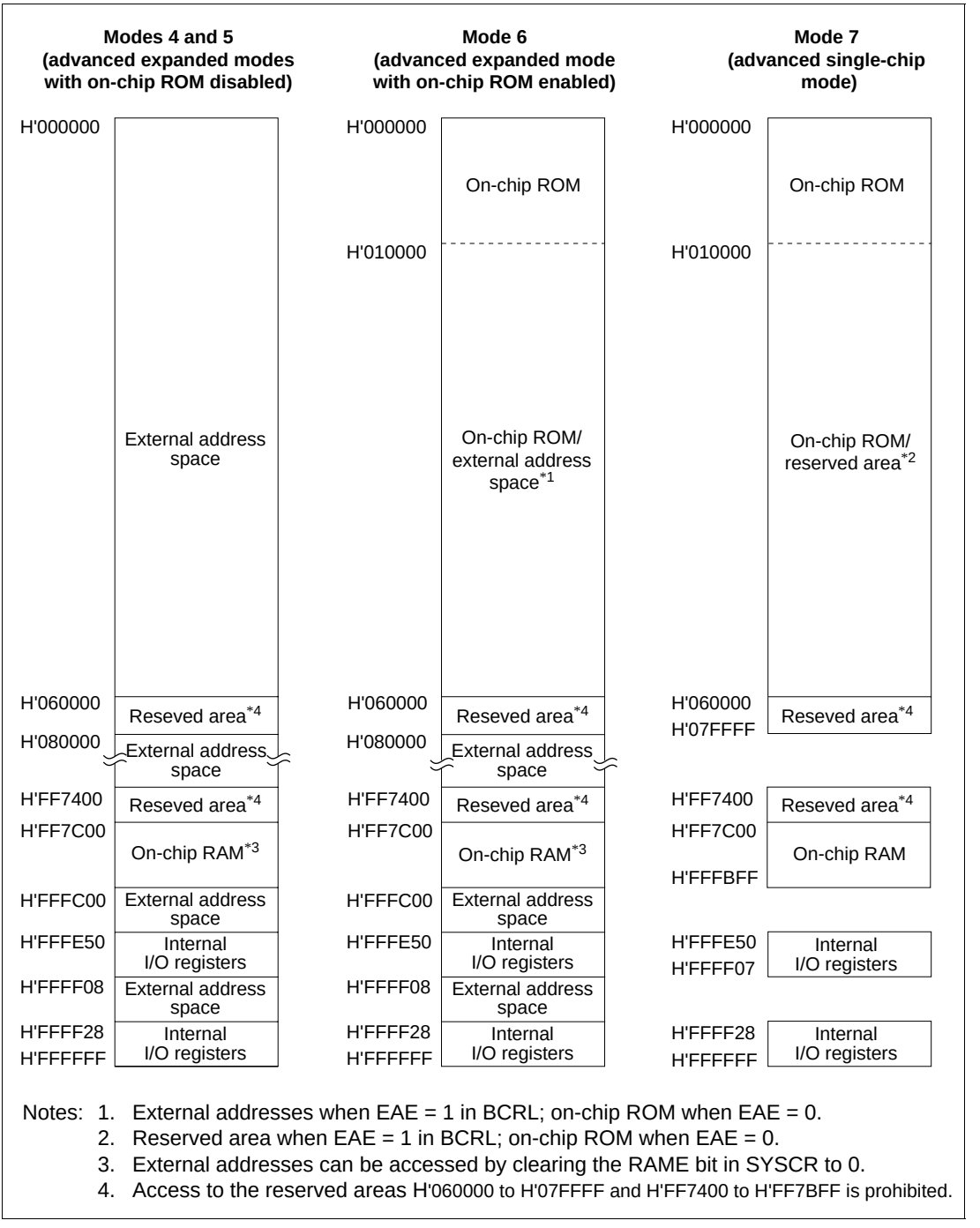
Note: * After reset

2.5 Memory Map in Each Operating Mode

Figures 2.1 to 2.4 show memory maps for each of the operating modes.

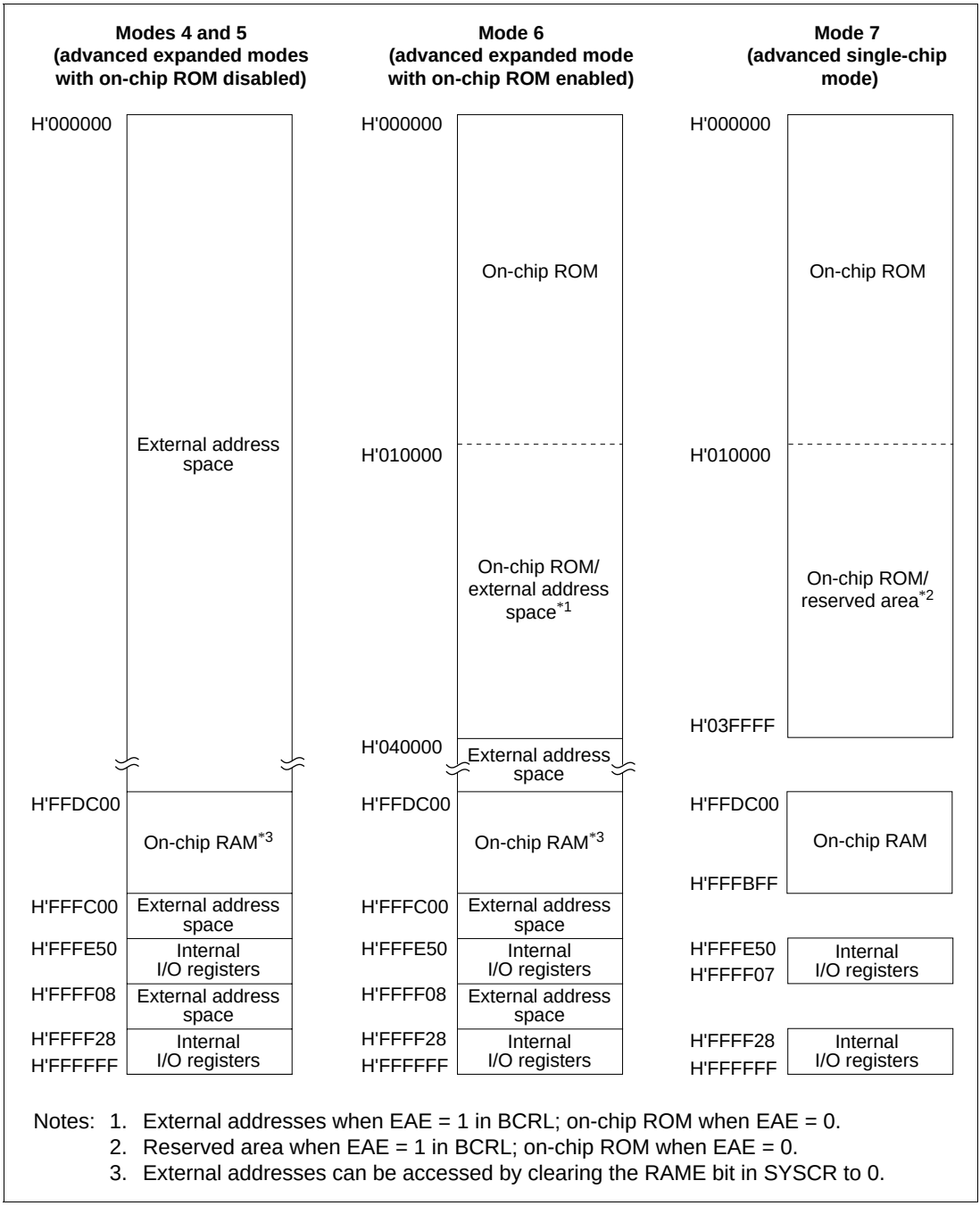
The address space is 16 Mbytes.

The address space is divided into eight areas.



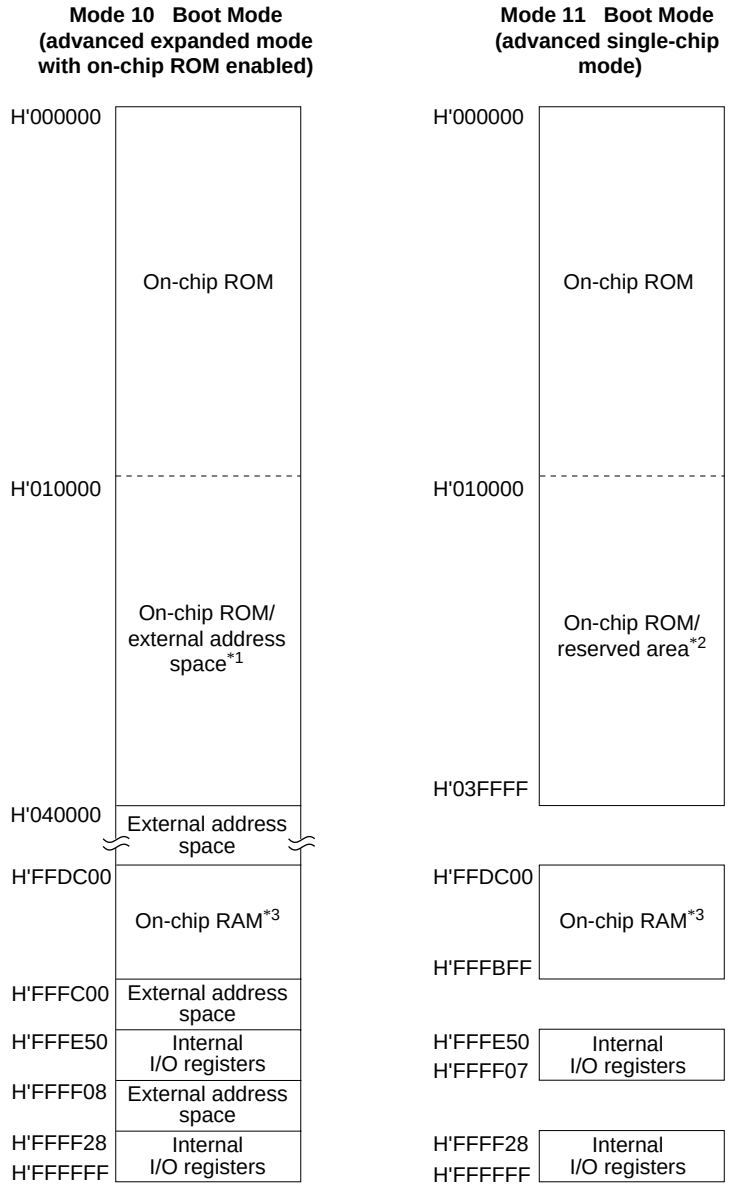
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Access to the reserved areas H'060000 to H'07FFFF and H'FF7400 to H'FF7BFF is prohibited.

Figure 2.1 H8S/2339 Memory Map in Each Operating Mode



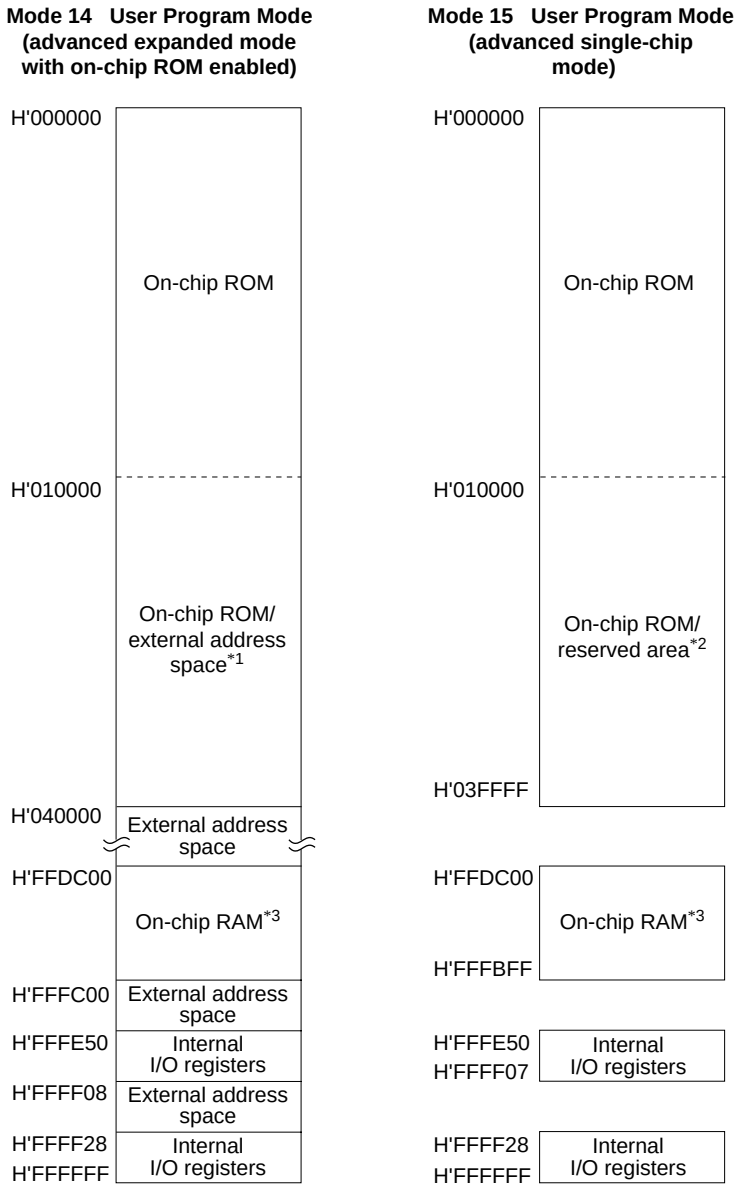
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.2 H8S/2338 Memory Map in Each Operating Mode



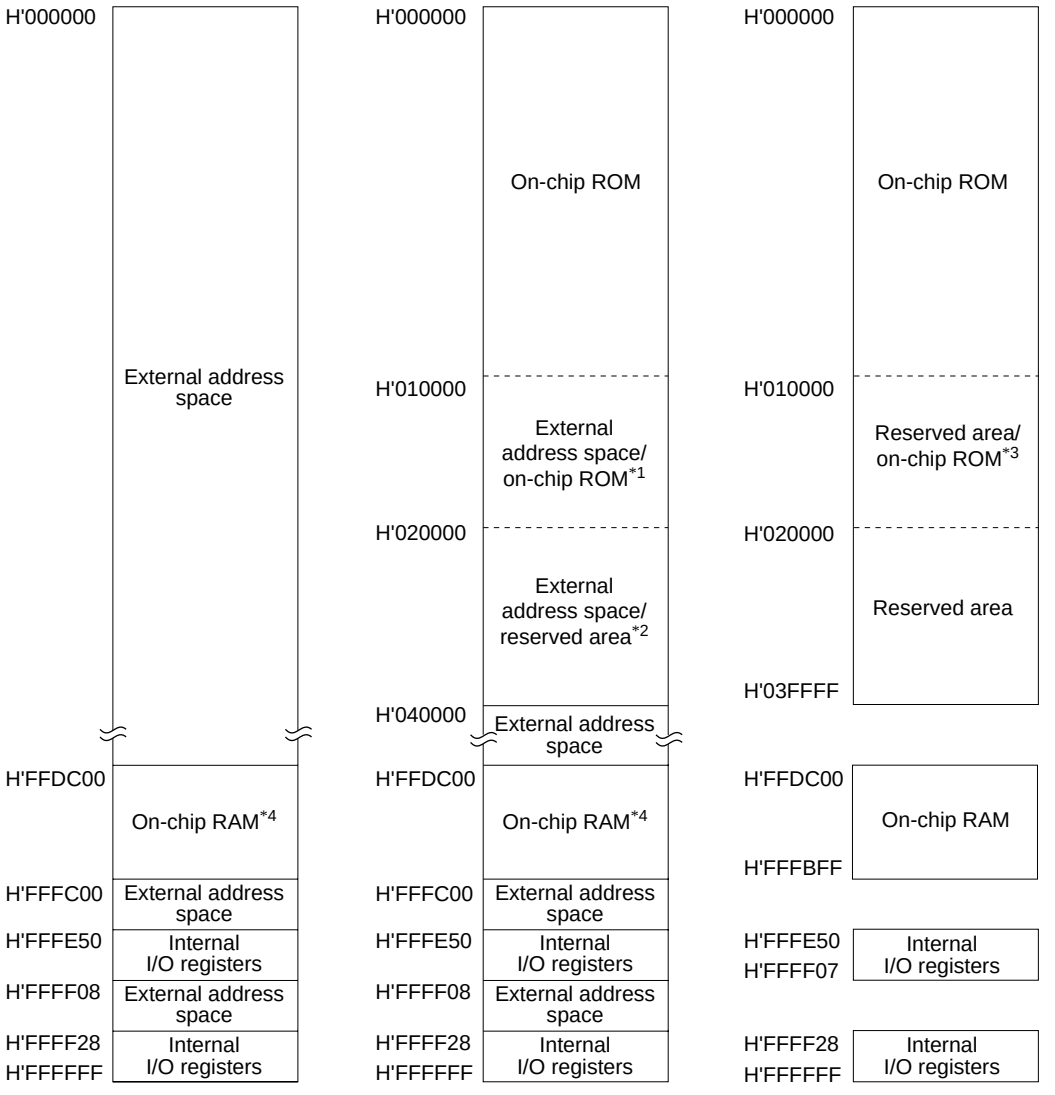
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.

Figure 2.2 H8S/2338 Memory Map in Each Operating Mode (cont)
(F-ZTAT Version Only)



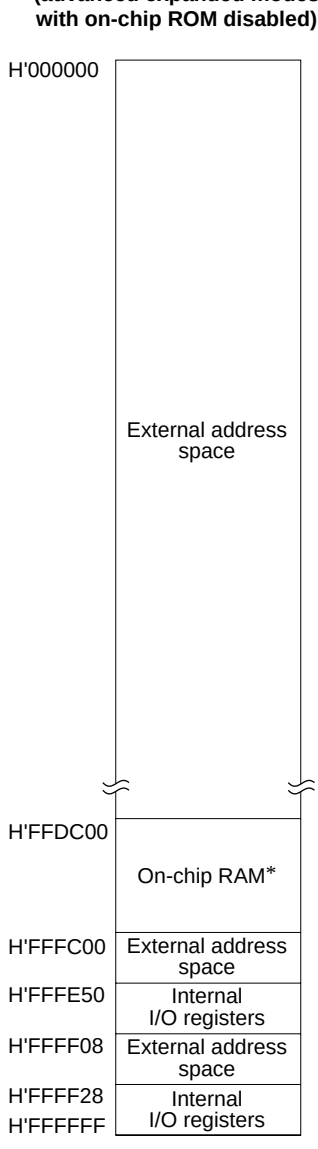
Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.

Figure 2.2 H8S/2338 Memory Map in Each Operating Mode (cont)
(F-ZTAT Version Only)



Notes: 1. External addresses when EAE = 1 in BCRL;on-chip ROM when EAE = 0.
2. External addresses when EAE = 1 in BCRL; reserved area when EAE = 0.
3. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
4. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.3 H8S/2337 Memory Map in Each Operating Mode



Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.4 H8S/2332 Memory Map in Each Operating Mode

Section 3 Exception Handling and Interrupt Controller

3.1 Overview

3.1.1 Exception Handling Types and Priority

As table 3.1 indicates, exception handling may be caused by a reset, trap instruction, or interrupt. Exception handling is prioritized as shown in table 3.1. If two or more exceptions occur simultaneously, they are accepted and processed in order of priority. Trap instruction exceptions are accepted at all times in the program execution state.

Exception handling sources, the stack structure, and the operation of the CPU vary depending on the interrupt control mode set by the INTM0 and INTM1 bits in SYSCR.

For details of exception handling and the interrupt controller, see section 2, Exception Handling, and section 3, Interrupt Controller, in the Hardware Manual.

Table 3.1 Exception Types and Priority

Priority	Exception Type	Start of Exception Handling
High ▲	Reset	Starts after a low-to-high transition at the $\overline{\text{RES}}$ pin, or when the watchdog timer overflows
	Trace*[1]	Starts when execution of the current instruction or exception handling ends, if the trace (T) bit is set to 1
	Interrupt	Starts when execution of the current instruction or exception handling ends, if an interrupt request has been issued*[2]
Low	Trap instruction*[3] (TRAPA)	Started by execution of a trap instruction (TRAPA)

Notes: 1. Traces are enabled only in interrupt control mode 2. Trace exception handling is not executed after execution of an RTE instruction.
2. Interrupt detection is not performed on completion of ANDC, ORC, XORC, or LDC instruction execution, or on completion of reset exception handling.
3. Trap instruction exception handling requests are accepted at all times in the program execution state.

3.2 Interrupt Controller

3.2.1 Interrupt Controller Features

- Two interrupt control modes
  - — Either of two interrupt control modes can be set by means of the INTM1 and INTM0 bits in the system control register (SYSCR).
- Priorities settable with IPRs
  - — Interrupt priority registers (IPRs) are provided for setting interrupt priorities. Eight priority levels can be set for each module for all interrupts except NMI.
  - — NMI is assigned the highest priority level of 8, and can be accepted at all times.
- Independent vector addresses
  - — All interrupt sources are assigned independent vector addresses, making it unnecessary for the source to be identified in the interrupt handling routine.
- Nine external interrupt pins
  - — NMI is the highest-priority interrupt, and is accepted at all times. Rising edge or falling edge can be selected for NMI.
  - — Falling edge, rising edge, or both edge detection, or level sensing, can be selected independently for IRQ_7 to IRQ_0.
- DTC and DMAC control
  - — DTC and DMAC activation is controlled by means of interrupts.

3.2.2 Pin Configuration

Table 3.2 Interrupt Controller Pins

Name	Symbol	I/O	Function
Nonmaskable interrupt	NMI	Input	Nonmaskable external interrupt; rising or falling edge can be selected
External interrupt requests 7 to 0	$\overline{IRQ_7}$ to $\overline{IRQ_0}$	Input	Maskable external interrupts; rising, falling, or both edges, or level sensing, can be selected

3.3 Interrupt Sources

Interrupt sources comprise external interrupts (NMI and IRQ_7 to IRQ_0) and internal interrupts (52 sources).

3.3.1 External Interrupts

There are nine external interrupts: NMI and IRQ_7 to IRQ_0. The pins that can be used for IRQ_7 to IRQ_4 interrupt input can be switched by means of the IRQPAS bit in SYSCR. NMI and IRQ_7 to IRQ_0 can be used to restore the chip from software standby mode. (IRQ_7 to IRQ_3 can be used as software standby mode clearing sources by setting the IRQ37S bit in SBYCR to 1.)

NMI Interrupt: NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of the status of the CPU interrupt mask bits. The NMIEG bit in SYSCR can be used to select whether an interrupt is requested at a rising edge or a falling edge on the NMI pin.

The vector number for NMI interrupt exception handling is 7.

Interrupts IRQ_7 to IRQ_0: Interrupts IRQ_7 to IRQ_0 are requested by an input signal at pins $\overline{IRQ}_7$ to $\overline{IRQ}_0$. Interrupts IRQ_7 to IRQ_0 have the following features:

- Using ISCR, it is possible to select whether an interrupt is generated by a low level, falling edge, rising edge, or both edges, at pins $\overline{IRQ}_7$ to $\overline{IRQ}_0$.
- Enabling or disabling of interrupt requests IRQ_7 to IRQ_0 can be selected with IER.
- The interrupt priority level can be set with the IPR registers.
- The status of interrupt requests IRQ_7 to IRQ_0 is indicated in ISR. ISR flags can be cleared to 0 by software.

A block diagram of interrupts IRQ_7 to IRQ_0 is shown in figure 3.1.

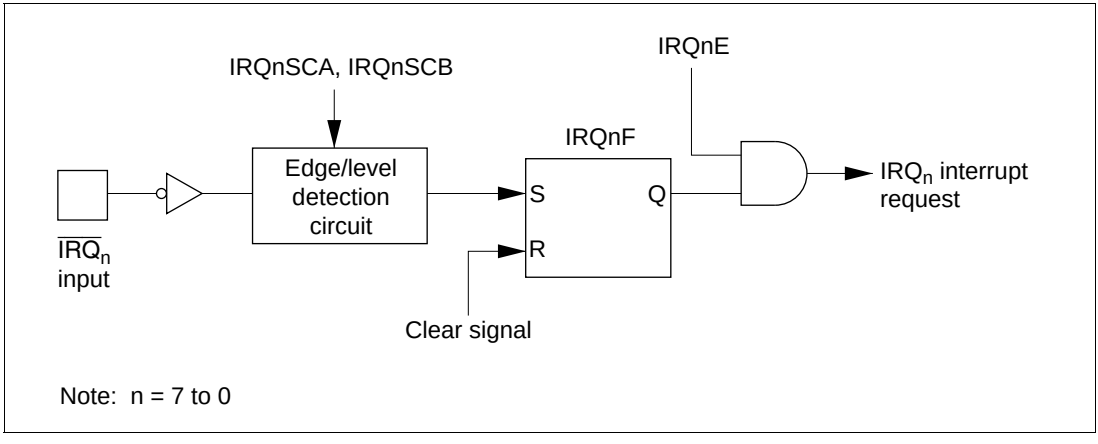


Figure 3.1 Block Diagram of Interrupts IRQ_7 to IRQ_0

Figure 3.2 shows the timing of IRQnF setting.

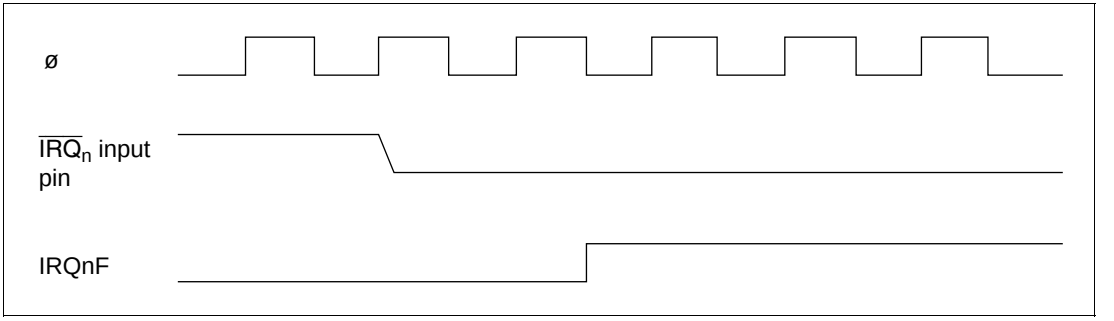


Figure 3.2 Timing of IRQnF Setting

The vector numbers for IRQ_7 to IRQ_0 interrupt exception handling are 23 to 16.

Detection of IRQ_7 to IRQ_0 interrupts does not depend on whether the relevant pin has been set for input or output. When a pin is used as an external interrupt input pin, clear the corresponding DDR bit to 0 and do not use the pin as an I/O pin for another function. Interrupts IRQ_7 to IRQ_4 can be input at pins $P9_7$ to $P9_4$ when the IRQPAS bit in SYSCR is cleared to 0, and at pins $P5_3$ to $P5_0$ when the IRQPAS bit is set to 1.

3.3.2 Internal Interrupts

There are 52 sources for internal interrupts from on-chip supporting modules.

1. For each on-chip supporting module there are flags that indicate the interrupt request status, and enable bits that select enabling or disabling of these interrupts. If any one of these is set to 1, an interrupt request is issued to the interrupt controller.
2. The interrupt priority level can be set by means of the IPR registers.
3. The DMAC and DTC can be activated by a TPU, SCI, or other interrupt request. When the DMAC or DTC is activated by an interrupt, the interrupt control mode and interrupt mask bits have no effect.

3.3.3 Interrupt Exception Vector Table

Table 3.3 shows interrupt sources, vector addresses, and interrupt priorities. For default priorities, the lower the vector number, the higher the priority. The DMAC or DTC can be activated by an interrupt request.

Priorities among modules can be set by means of the IPR registers. The situation when two or more modules are set to the same priority, and priorities within a module, are fixed as shown in table 3.3.

Table 3.3 Interrupt Sources, Vector Addresses, and Interrupt Priorities

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
Power-on reset		0	H'0000	—	High	—	—
Reserved		1	H'0004				
Reserved for system use		2	H'0008				
		3	H'000C				
		4	H'0010				
Trace		5	H'0014				
Reserved for system use		6	H'0018				
NMI	External pin	7	H'001C				
Trap instruction (4 sources)		8	H'0020				
		9	H'0024				
		10	H'0028				
		11	H'002C				
Reserved for system use		12	H'0030				
		13	H'0034				
		14	H'0038				
		15	H'003C				
IRQ_0	External pin	16	H'0040	IPRA6 to IPRA4		○	—
IRQ_1		17	H'0044	IPRA2 to IPRA0		○	—
IRQ_2		18	H'0048	IPRB6 to IPRB4		○	—
IRQ_3		19	H'004C			○	—
IRQ_4		20	H'0050	IPRB2 to IPRB0		○	—
IRQ_5		21	H'0054			○	—
IRQ_6		22	H'0058	IPRC6 to IPRC4		○	—
IRQ_7		23	H'005C		Low	○	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
SWDTEND (software-activated data transfer end)	DTC	24	H'0060	IPRC2 to IPRC0	High	○	—
WOVI (interval timer)	Watchdog timer	25	H'0064	IPRD6 to IPRD4		—	—
CMI (compare match)	Refresh controller	26	H'0068	IPRD2 to IPRD0		—	—
Reserved	—	27	H'006C	IPRE6 to IPRE4		—	—
ADI (A/D conversion end)	A/D	28	H'0070	IPRE2 to IPRE0		○	○
Reserved	—	29	H'0074			—	—
		30	H'0078				
		31	H'007C				
TGI0A (TGR0A input capture/compare match)	TPU channel 0	32	H'0080	IPRF6 to IPRF4		○	○
TGI0B (TGR0B input capture/compare match)		33	H'0084			○	—
TGI0C (TGR0C input capture/compare match)		34	H'0088			○	—
TGI0D (TGR0D input capture/compare match)		35	H'008C			○	—
TCI0V (overflow 0)		36	H'0090			—	—
Reserved	—	37	H'0094			—	—
		38	H'0098				
		39	H'009C		Low		

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
TGI1A (TGR1A input capture/compare match)	TPU channel 1	40	H'00A0	IPRF2 to IPRF0	High	○	○
TGI1B (TGR1B input capture/compare match)		41	H'00A4			○	—
TCI1V (overflow 1)		42	H'00A8			—	—
TCI1U (underflow 1)		43	H'00AC			—	—
TGI2A (TGR2A input capture/compare match)	TPU channel 2	44	H'00B0	IPRG6 to IPRG4		○	○
TGI2B (TGR2B input capture/compare match)		45	H'00B4			○	—
TCI2V (overflow 2)		46	H'00B8			—	—
TCI2U (underflow 2)		47	H'00BC			—	—
TGI3A (TGR3A input capture/compare match)	TPU channel 3	48	H'00C0	IPRG2 to IPRG0		○	○
TGI3B (TGR3B input capture/compare match)		49	H'00C4			○	—
TGI3C (TGR3C input capture/compare match)		50	H'00C8			○	—
TGI3D (TGR3D input capture/compare match)		51	H'00CC			○	—
TCI3V (overflow 3)		52	H'00D0			—	—
Reserved	—	53	H'00D4			—	—
		54	H'00D8				
		55	H'00DC		Low		

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
TGI4A (TGR4A input capture/compare match)	TPU channel 4	56	H'00E0	IPRH6 to IPRH4	High	○	○
TGI4B (TGR4B input capture/compare match)		57	H'00E4			○	—
TCI4V (overflow 4)		58	H'00E8			—	—
TCI4U (underflow 4)		59	H'00EC			—	—
TGI5A (TGR5A input capture/compare match)	TPU channel 5	60	H'00F0	IPRH2 to IPRH0		○	○
TGI5B (TGR5B input capture/compare match)		61	H'00F4			○	—
TCI5V (overflow 5)		62	H'00F8			—	—
TCI5U (underflow 5)		63	H'00FC			—	—
CMIA0 (compare match A)	8-bit timer channel 0	64	H'0100	IPRI6 to IPRI4		○	—
CMIB0 (compare match B)		65	H'0104			○	—
OVI0 (overflow 0)		66	H'0108			—	—
Reserved	—	67	H'010C			—	—
CMIA1 (compare match A)	8-bit timer channel 1	68	H'0110	IPRI2 to IPRI0		○	—
CMIB1 (compare match B)		69	H'0114			○	—
OVI1 (overflow 1)		70	H'0118			—	—
Reserved	—	71	H'011C		Low	—	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
DEND0A (channel 0/channel 0A transfer end)	DMAC	72	H'0120	IPRJ6 to IPRJ4	High	○	—
DEND0B (channel 0B transfer end)		73	H'0124			○	—
DEND1A (channel 1/channel 1A transfer end)		74	H'0128			○	—
DEND1B (channel 1B transfer end)		75	H'012C			○	—
Reserved	—	76	H'0130			—	—
		77	H'0134				
		78	H'0138				
		79	H'013C				
ERI0 (receive error 0)	SCI channel 0	80	H'0140	IPRJ2 to IPRJ0		—	—
RXI0 (reception complete 0)		81	H'0144			○	○
TXI0 (transmit data empty 0)		82	H'0148			○	○
TEI0 (transmit end 0)		83	H'014C			—	—
ERI1 (receive error 1)	SCI channel 1	84	H'0150	IPRK6 to IPRK4		—	—
RXI1 (reception complete 1)		85	H'0154			○	○
TXI1 (transmit data empty 1)		86	H'0158			○	○
TEI1 (transmit end 1)		87	H'015C			—	—
ERI2 (receive error 2)	SCI channel 2	88	H'0160	IPRK2 to IPRK0		—	—
RXI2 (reception complete 2)		89	H'0164			○	—
TXI2 (transmit data empty 2)		90	H'0168			○	—
TEI2 (transmit end 2)		91	H'016C		Low	—	—

Note: * Lower 16 bits of the start address.

3.4 Interrupt Control Modes and Interrupt Operation

Interrupt operations in the H8S/2339 and H8S/2338 Series differ depending on the interrupt control mode.

NMI interrupts are accepted at all times except in the reset state and the hardware standby state. In the case of IRQ interrupts and on-chip supporting module interrupts, an enable bit is provided for each interrupt. Clearing an enable bit to 0 disables the corresponding interrupt request. Interrupt sources for which the enable bit is set to 1 are controlled by the interrupt controller.

The interrupt control modes are shown in table 3.4, the interrupts selected in each interrupt control mode in tables 3.5 and 3.6, and operations and control signal functions in each interrupt control mode in table 3.7.

The interrupt controller performs interrupt control according to the interrupt control mode set by the INTM1 and INTM0 bits in SYSCR, the priorities set in the IPR registers, and the masking state indicated by the I bit in the CPU's CCR and bits I2 to I0 in EXR.

Table 3.4 Interrupt Control Modes

Interrupt Control Mode	INTM1	INTM0	Priority Setting Registers	Interrupt Mask Bits	Description
0	0	0	—	I	Interrupt mask control is performed by the I bit.
—		1	—	—	Setting prohibited
2	1	0	IPR	I2 to I0	8-level interrupt mask control is performed by bits I2 to I0. 8 priority levels can be set with IPR.
—		1	—	—	Setting prohibited

Table 3.5 Interrupts Selected in Each Interrupt Control Mode (1)

Interrupt Control Mode	Interrupt Mask Bits	
	I	Selected Interrupts
0	0	All interrupts
	1	NMI interrupts
2	*	All interrupts

*: Don't care

Table 3.6 Interrupts Selected in Each Interrupt Control Mode (2)

Interrupt Control Mode	Selected Interrupts
0	All interrupts
2	Highest-priority-level (IPR) interrupt with priority level greater than the mask level (IPR > I2 to I0)

Table 3.7 Operations and Control Signal Functions in Each Interrupt Control Mode

Interrupt Control Mode	Settings		Interrupt Acceptance Control		8-Level Control			Default Priority Determination	T (Trace)
	INTM1	INTM0		I		I2 to I0	IPR		
0	0	0	O	IM	x	—	—*[2]	O	—
2	1	0	x	—*[1]	O	IM	PR	O	T

Legend

O: Interrupt operation control performed

x: No operation (all interrupts enabled)

IM: Used as interrupt mask bit

PR: Sets priority

—: Not used

Notes: 1. Set to 1 when interrupt is accepted.

2. Keep the initial setting.

3.5 Interrupt Response Times

The H8S/2339 and H8S/2338 Series are capable of fast word access to on-chip memory, and the program area is provided in on-chip ROM and the stack area in on-chip RAM, enabling high-speed processing.

Table 3.8 shows interrupt response times—the interval between generation of an interrupt request and execution of the first instruction in the interrupt handling routine. The execution phase symbols used in table 3.8 are explained in table 3.9.

Table 3.8 Interrupt Response Times

		Advanced Mode	
No.	**Execution Phase**	**INTM1 = 0**	**INTM1 = 1**
1	Interrupt priority determination*[1]	3	3
2	Number of wait states until executing instruction ends*[2]	1 to 19 + 2 · S_I	1 to 19 + 2 · S_I
3	PC, CCR, and EXR stacking	2 · S_K	3 · S_K
4	Vector fetch	2 · S_I	2 · S_I
5	Instruction fetch*[3]	2 · S_I	2 · S_I
6	Internal processing*[4]	2	2
Total (when using on-chip memory)		12 to 32	13 to 33

Notes: 1. Two states in case of internal interrupt.
2. Refers to MULXS and DIVXS instructions.
3. Prefetch after interrupt acceptance and interrupt handling routine prefetch.
4. Internal processing after interrupt acceptance and internal processing after vector fetch.

Table 3.9 Number of States in Interrupt Handling Routine Execution Phases

	Access To				
		External Device			
		8-Bit Bus		16-Bit Bus	
Symbol	**Internal Memory**	**2-State Access**	**3-State Access**	**2-State Access**	**3-State Access**
Instruction fetch S_I	1	4	6 + 2m	2	3 + m
Branch address read S_J					
Stack manipulation S_K					

Legend
m: Number of wait states in an external device access

3.6 DTC and DMAC Activation by Interrupt

3.6.1 Overview

In the H8S/2339 and H8S/2338 Series, the DTC and DMAC can be activated by an interrupt. In this case, the following options are available:

1. Interrupt request to CPU
2. Activation request to DTC
3. Activation request to DMAC
4. Selection of a number of the above

See table 3.3 for the interrupt requests that can be used to activate the DTC or DMAC. For details, see section 5, DMA Controller, and section 6, Data Transfer Controller, in the Hardware Manual.

3.6.2 Block Diagram

Figure 3.3 shows a block diagram of the DTC, DMAC, and interrupt controller.

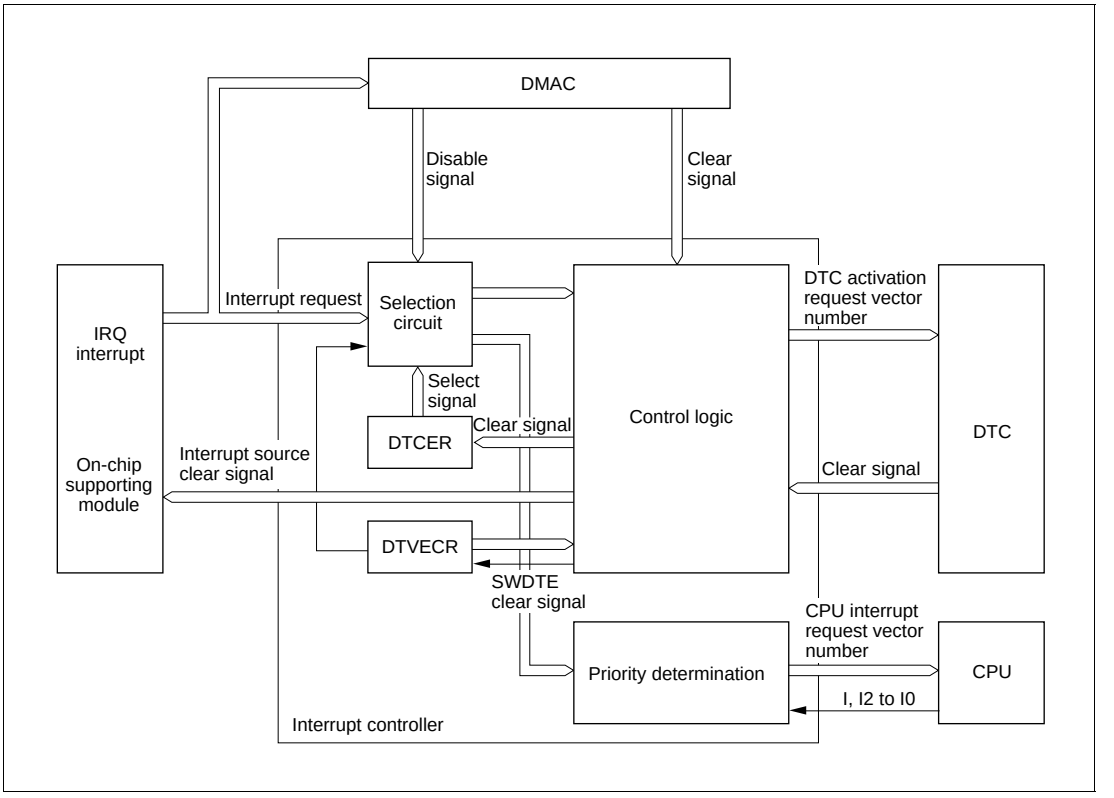


Figure 3.3 Interrupt Control for DTC and DMAC

3.6.3 Operation

The interrupt controller has three main functions in DTC and DMAC control, as described below.

Selection of Interrupt Source: With the DMAC, the activation source is input directly to each channel. The activation source for each DMAC channel is selected with bits DTF3 to DTF0 in DMACR. The selected activation source can be managed by the DMAC or selected with the DTA bit in DMABCR. When the DTA bit is set to 1, the interrupt source constituting that DMAC activation source does not function as a DTC activation source or CPU interrupt source.

For interrupt sources other than interrupts managed by the DMAC, it is possible to select DTC activation request or CPU interrupt request with the DTCE bit in DTC registers DTCERA to DTCERF.

After a DTC data transfer, the DTCE bit can be cleared to 0 and an interrupt request sent to the CPU in accordance with the specification of the DISEL bit in the DTC's MRB register.

When the DTC has performed the specified number of data transfers and the transfer counter value is 0, the DTCE bit is cleared to 0 after the DTC data transfer and an interrupt request is sent to the CPU.

Determination of Priority: The DTC activation source is selected in accordance with the default priority order, and is not affected by mask or priority levels. See table 3.10, Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs, for the respective priorities.

With the DMAC, the activation source is input directly to each channel.

Table 3.10 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address	DTCE*	Priority
Write to DTVECR	Software	DTVECR	H'0400 + (DTVECR [6:0]<<1)	—	High
IRQ_0	External pin	16	H'0420	DTCEA7	
IRQ_1		17	H'0422	DTCEA6	
IRQ_2		18	H'0424	DTCEA5	
IRQ_3		19	H'0426	DTCEA4	
IRQ_4		20	H'0428	DTCEA3	
IRQ_5		21	H'042A	DTCEA2	
IRQ_6		22	H'042C	DTCEA1	
IRQ_7		23	H'042E	DTCEA0	
ADI (A/D conversion end)	A/D	28	H'0438	DTCEB6	
TGI0A (GR0A compare match/input capture)	TPU channel 0	32	H'0440	DTCEB5	
TGI0B (GR0B compare match/input capture)		33	H'0442	DTCEB4	
TGI0C (GR0C compare match/input capture)		34	H'0444	DTCEB3	
TGI0D (GR0D compare match/input capture)		35	H'0446	DTCEB2	Low

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address	DTCE*	Priority
TGI1A (GR1A compare match/input capture)	TPU channel 1	40	H'0450	DTCEB1	High
TGI1B (GR1B compare match/input capture)		41	H'0452	DTCEB0	
TGI2A (GR2A compare match/input capture)	TPU channel 2	44	H'0458	DTCEC7	
TGI2B (GR2B compare match/input capture)		45	H'045A	DTCEC6	
TGI3A (GR3A compare match/input capture)	TPU channel 3	48	H'0460	DTCEC5	
TGI3B (GR3B compare match/input capture)		49	H'0462	DTCEC4	
TGI3C (GR3C compare match/input capture)		50	H'0464	DTCEC3	
TGI3D (GR3D compare match/input capture)		51	H'0466	DTCEC2	
TGI4A (GR4A compare match/input capture)	TPU channel 4	56	H'0470	DTCEC1	
TGI4B (GR4B compare match/input capture)		57	H'0472	DTCEC0	
TGI5A (GR5A compare match/input capture)	TPU channel 5	60	H'0478	DTCED5	
TGI5B (GR5B compare match/input capture)		61	H'047A	DTCED4	
CMIA0	8-bit timer channel 0	64	H'0480	DTCED3	
CMIB0		65	H'0482	DTCED2	
CMIA1	8-bit timer channel 1	68	H'0488	DTCED1	
CMIB1		69	H'048A	DTCED0	
DMTEND0A (DMAC transfer end 0)	DMAC	72	H'0490	DTCEE7	
DMTEND0B (DMAC transfer end 1)		73	H'0492	DTCEE6	
DMTEND1A (DMAC transfer end 2)		74	H'0494	DTCEE5	
DMTEND1B (DMAC transfer end 3)		75	H'0496	DTCEE4	Low

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address	DTCE*	Priority
RXI0 (reception complete 0)	SCI timer channel 0	81	H'04A2	DTCEE3	High
TXI0 (transmit data empty 0)		82	H'04A4	DTCEE2	
RXI1 (reception complete 1)	SCI timer channel 1	85	H'04AA	DTCEE1	
TXI1 (transmit data empty 1)		86	H'04AC	DTCEE0	
RXI2 (reception complete 2)	SCI timer channel 2	89	H'04B2	DTCEF7	
TXI2 (transmit data empty 2)		90	H'04B4	DTCEF6	Low

Note: * DTCE bits with no corresponding interrupt are reserved, and should be written with 0.

Operation Order: If the same interrupt is selected as a DTC activation source and a CPU interrupt source, the DTC data transfer is performed first, followed by CPU interrupt exception handling.

If the same interrupt is selected as a DMAC activation source and a DTC activation source or CPU interrupt source, operations are performed for them independently according to their respective operating statuses and bus mastership priorities.

Table 3.11 summarizes interrupt source selection and interrupt source clearance control according to the setting of the DTA bit in the DMAC's DMABCR register, the DTCE bit of DTC registers DTCERA to DTCERF, and the DISEL bit in the DTC's MRB register.

Table 3.11 Interrupt Source Selection and Clearing Control

Settings					
DMAC	DTC		Interrupt Source Selection/Clearing Control		
DTA	DTCE	DISEL	DMAC	DTC	CPU
0	0	*	○	X	◎
	1	0	○	◎	X
		1	○	○	◎
1	*	*	◎	X	X

Legend

◎: The relevant interrupt is used. Interrupt source clearing is performed.
(The CPU should clear the source flag in the interrupt handling routine.)

○: The relevant interrupt is used. The interrupt source is not cleared.

X: The relevant bit cannot be used.

*: Don't care

Usage Note: SCI and A/D converter interrupt sources are cleared when the DMAC or DTC reads or writes to the prescribed register, and are not dependent on the DTA and DISEL bits.

Section 4 Bus Controller

4.1 Overview

The H8S/2339 and H8S/2338 Series have an on-chip bus controller (BSC) that manages the external address space divided into eight areas. The bus specifications, such as bus width and number of access states, can be set independently for each area, enabling multiple memories to be connected easily.

The bus controller also has a bus arbitration function, and controls the operation of the internal bus masters—the CPU, DMA controller (DMAC), and data transfer controller (DTC).

4.1.1 Features

The features of the bus controller are listed below.

- Manages external address space in area units
  - In advanced mode, manages the external space as 8 areas of 2 Mbytes
  - Bus specifications can be set independently for each area
  - DRAM and burst ROM interfaces can be set
- Basic bus interface
  - Chip select signals ($\overline{CS}_0$ to $\overline{CS}_7$) can be output for areas 0 to 7
  - 8-bit access or 16-bit access can be selected for each area
  - 2-state access or 3-state access can be selected for each area
  - Program wait states can be inserted for each area
- DRAM interface
  - DRAM interface can be set for areas 2 to 5 (in advanced mode)
  - Row address/column address multiplexed output (8/9/10 bits)
  - 2-CAS access method
  - Burst operation (fast page mode)
  - TP cycle insertion to secure RAS precharging time
  - Selection of CAS-before-RAS refreshing or self-refreshing
- Burst ROM interface
  - Burst ROM interface can be set for area 0
  - Selection of 1- or 2-state burst access

- Idle cycle insertion
  - An idle cycle can be inserted in case of external read cycles in different areas
  - An idle cycle can be inserted in case of an external write cycle immediately after an external read cycle
- Write buffer function
  - External write cycle and internal access can be executed in parallel
  - DMAC single address mode and internal access can be executed in parallel
- Bus arbitration function
  - Includes a bus arbiter that arbitrates bus mastership between the CPU, DMAC, and DTC
- Other features
  - Refresh counter (refresh timer) can be used as an interval timer
  - External bus release function

4.1.2 Block Diagram

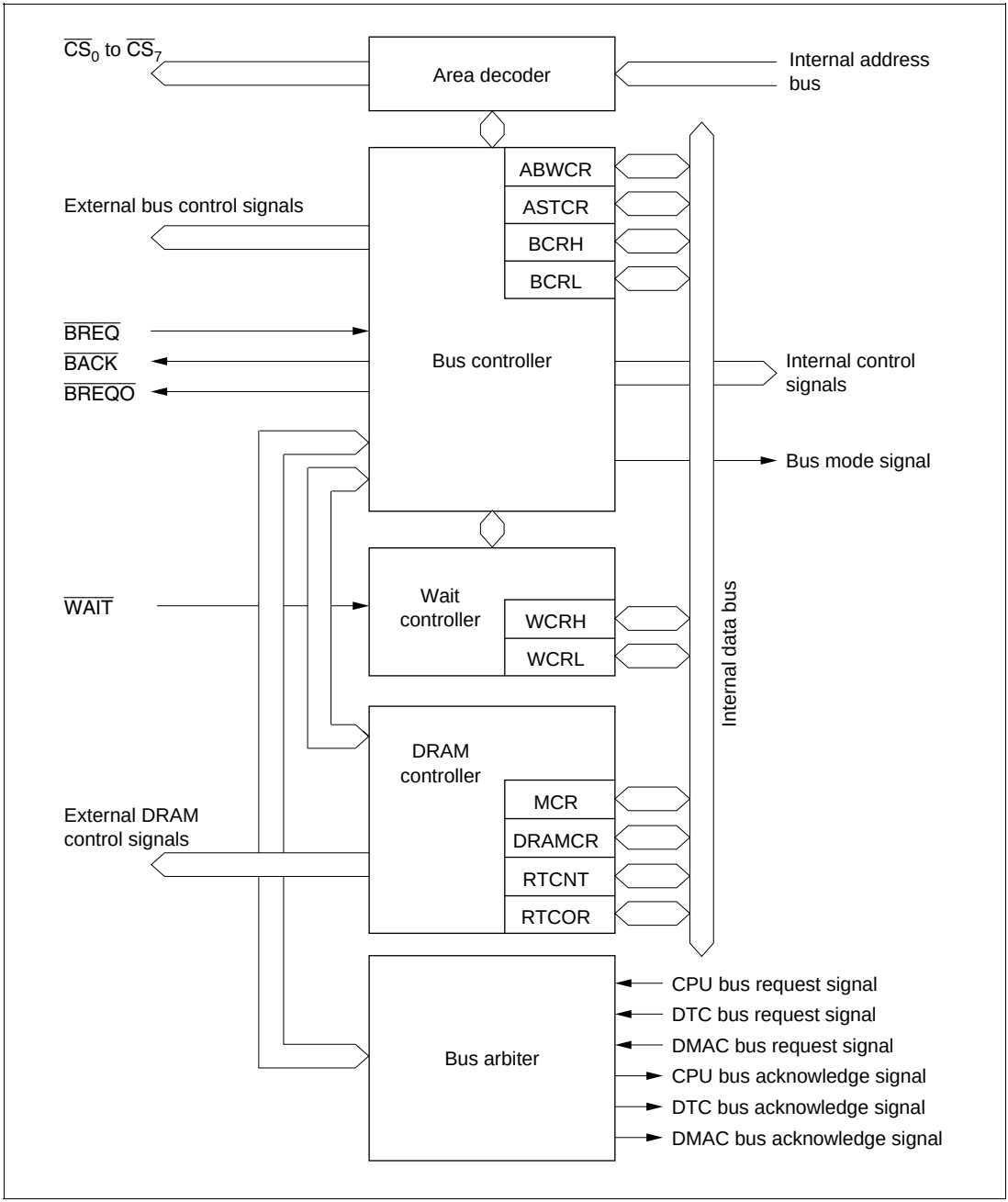


Figure 4.1 Block Diagram of Bus Controller

4.1.3 Pin Configuration

Table 4.1 summarizes the pins of the bus controller.

Table 4.1 Bus Controller Pins

Name	Symbol	I/O	Function
Address strobe	$\overline{AS}$	Output	Strobe signal indicating that address output on address bus is enabled.
Read	$\overline{RD}$	Output	Strobe signal indicating that external space is being read.
High write/write enable	$\overline{HWR}$	Output	Strobe signal indicating that external space is to be written, and upper half (D_{15} to D_8) of data bus is enabled. 2-CAS DRAM write enable signal.
Low write	$\overline{LWR}$	Output	Strobe signal indicating that external space is to be written, and lower half (D_7 to D_0) of data bus is enabled.
Chip select 0	$\overline{CS}_0$	Output	Strobe signal indicating that area 0 is selected.
Chip select 1	$\overline{CS}_1$	Output	Strobe signal indicating that area 1 is selected.
Chip select 2/row address strobe 2	$\overline{CS}_2$	Output	Strobe signal indicating that area 2 is selected. DRAM row address strobe signal when area 2 is in DRAM space.
Chip select 3/row address strobe 3	$\overline{CS}_3$	Output	Strobe signal indicating that area 3 is selected. DRAM row address strobe signal when area 3 is in DRAM space.
Chip select 4/row address strobe 4	$\overline{CS}_4$	Output	Strobe signal indicating that area 4 is selected. DRAM row address strobe signal when area 4 is in DRAM space.
Chip select 5/row address strobe 5	$\overline{CS}_5$	Output	Strobe signal indicating that area 5 is selected. DRAM row address strobe signal when area 5 is in DRAM space.
Chip select 6	$\overline{CS}_6$	Output	Strobe signal indicating that area 6 is selected.
Chip select 7	$\overline{CS}_7$	Output	Strobe signal indicating that area 7 is selected.
Upper column address strobe	$\overline{CAS}$	Output	2-CAS DRAM upper column address strobe signal.
Lower column strobe	$\overline{LCAS}$	Output	DRAM lower column address strobe signal.
Wait	$\overline{WAIT}$	Input	Wait request signal when accessing external 3-state access space.

Name	Symbol	I/O	Function
Bus request	$\overline{\text{BREQ}}$	Input	Request signal for release of bus to external device.
Bus request acknowledge	$\overline{\text{BACK}}$	Output	Acknowledge signal indicating that bus has been released.
Bus request output	$\overline{\text{BREQO}}$	Output	External bus request signal used when internal bus master accesses external space when external bus is released.

4.1.4 Register Configuration

Table 4.2 summarizes the registers of the bus controller.

Table 4.2 Bus Controller Registers

Name	Abbreviation	R/W	Initial Value: Reset	Address*[1]
Bus width control register	ABWCR	R/W	H'FF/H'00*[2]	H'FED0
Access state control register	ASTCR	R/W	H'FF	H'FED1
Wait control register H	WCRH	R/W	H'FF	H'FED2
Wait control register L	WCRL	R/W	H'FF	H'FED3
Bus control register H	BCRH	R/W	H'D0	H'FED4
Bus control register L	BCRL	R/W	H'3C	H'FED5
Memory control register	MCR	R/W	H'00	H'FED6
DRAM control register	DRAMCR	R/W	H'00	H'FED7
Refresh timer counter	RTCNT	R/W	H'00	H'FED8
Refresh time constant register	RTCOR	R/W	H'FF	H'FED9

Notes: 1. Lower 16 bits of the address.
2. Determined by the MCU operating mode.

4.2 Register Descriptions

4.2.1 Bus Width Control Register (ABWCR)

Bit	:	7	6	5	4	3	2	1	0
		ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 5 to 7									
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 4									
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ABWCR is an 8-bit readable/writable register that designates each area as either 8-bit access space or 16-bit access space.

ABWCR sets the data bus width for the external memory space. The bus width for on-chip memory and internal I/O registers is fixed regardless of the settings in ABWCR.

After a reset and in hardware standby mode, ABWCR is initialized to H'FF in modes 5 to 7*, and to H'00 in mode 4. It is not initialized in software standby mode.

Note: * Modes 6 and 7 cannot be used in the ROMless version.

Bits 7 to 0—Area 7 to 0 Bus Width Control (ABW7 to ABW0): These bits select whether the corresponding area is to be designated as 8-bit access space or 16-bit access space.

Bit n **ABWn**	**Description**
0	Area n is designated for 16-bit access
1	Area n is designated for 8-bit access

(n = 7 to 0)

4.2.2 Access State Control Register (ASTCR)

Bit	:	7	6	5	4	3	2	1	0
		AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASTCR is an 8-bit readable/writable register that designates each area as either 2-state access space or 3-state access space.

ASTCR sets the number of access states for the external memory space. The number of access states for on-chip memory and internal I/O registers is fixed regardless of the settings in ASTCR.

ASTCR is initialized to H'FF by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 0—Area 7 to 0 Access State Control (AST7 to AST0): These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space.

Wait state insertion is enabled or disabled at the same time.

Bit n ASTn	Description	
0	Area n is designated for 2-state access Wait state insertion in area n external space access is disabled	
1	Area n is designated for 3-state access Wait state insertion in area n external space access is enabled	(Initial value)

(n = 7 to 0)

4.2.3 Wait Control Registers H and L (WCRH, WCRL)

WCRH and WCRL are 8-bit readable/writable registers that select the number of program wait states for each area.

Program waits are not inserted in on-chip memory or internal I/O register access.

WCRH and WCRL are initialized to H'FF by a reset, and in hardware standby mode. They are not initialized in software standby mode.

WCRH

Bit	:	7	6	5	4	3	2	1	0
		W71	W70	W61	W60	W51	W50	W41	W40
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—Area 7 Wait Control 1 and 0 (W71, W70): These bits select the number of program wait states when area 7 in external space is accessed while the AST7 bit in ASTCR is set to 1.

Bit 7 W71	Bit 6 W70	Description
0	0	Program wait not inserted when external space area 7 is accessed
	1	1 program wait state inserted when external space area 7 is accessed
1	0	2 program wait states inserted when external space area 7 is accessed
	1	3 program wait states inserted when external space area 7 is accessed (Initial value)

Bits 5 and 4—Area 6 Wait Control 1 and 0 (W61, W60): These bits select the number of program wait states when area 6 in external space is accessed while the AST6 bit in ASTCR is set to 1.

Bit 5 W61	Bit 4 W60	Description
0	0	Program wait not inserted when external space area 6 is accessed
	1	1 program wait state inserted when external space area 6 is accessed
1	0	2 program wait states inserted when external space area 6 is accessed
	1	3 program wait states inserted when external space area 6 is accessed (Initial value)

Bits 3 and 2—Area 5 Wait Control 1 and 0 (W51, W50): These bits select the number of program wait states when area 5 in external space is accessed while the AST5 bit in ASTCR is set to 1.

Bit 3 W51	Bit 2 W50	Description
0	0	Program wait not inserted when external space area 5 is accessed
	1	1 program wait state inserted when external space area 5 is accessed
1	0	2 program wait states inserted when external space area 5 is accessed
	1	3 program wait states inserted when external space area 5 is accessed (Initial value)

Bits 1 and 0—Area 4 Wait Control 1 and 0 (W41, W40): These bits select the number of program wait states when area 4 in external space is accessed while the AST4 bit in ASTCR is set to 1.

Bit 1 W41	Bit 0 W40	Description
0	0	Program wait not inserted when external space area 4 is accessed
	1	1 program wait state inserted when external space area 4 is accessed
1	0	2 program wait states inserted when external space area 4 is accessed
	1	3 program wait states inserted when external space area 4 is accessed (Initial value)

WCRL

Bit	:	7	6	5	4	3	2	1	0
		W31	W30	W21	W20	W11	W10	W01	W00
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—Area 3 Wait Control 1 and 0 (W31, W30): These bits select the number of program wait states when area 3 in external space is accessed while the AST3 bit in ASTCR is set to 1.

Bit 7 W31	Bit 6 W30	Description
0	0	Program wait not inserted when external space area 3 is accessed
	1	1 program wait state inserted when external space area 3 is accessed
1	0	2 program wait states inserted when external space area 3 is accessed
	1	3 program wait states inserted when external space area 3 is accessed (Initial value)

Bits 5 and 4—Area 2 Wait Control 1 and 0 (W21, W20): These bits select the number of program wait states when area 2 in external space is accessed while the AST2 bit in ASTCR is set to 1.

Bit 5 W21	Bit 4 W20	Description
0	0	Program wait not inserted when external space area 2 is accessed
	1	1 program wait state inserted when external space area 2 is accessed
1	0	2 program wait states inserted when external space area 2 is accessed
	1	3 program wait states inserted when external space area 2 is accessed (Initial value)

Bits 3 and 2—Area 1 Wait Control 1 and 0 (W11, W10): These bits select the number of program wait states when area 1 in external space is accessed while the AST1 bit in ASTCR is set to 1.

Bit 3 W11	Bit 2 W10	Description
0	0	Program wait not inserted when external space area 1 is accessed
	1	1 program wait state inserted when external space area 1 is accessed
1	0	2 program wait states inserted when external space area 1 is accessed
	1	3 program wait states inserted when external space area 1 is accessed (Initial value)

Bits 1 and 0—Area 0 Wait Control 1 and 0 (W01, W00): These bits select the number of program wait states when area 0 in external space is accessed while the AST0 bit in ASTCR is set to 1.

Bit 1 W01	Bit 0 W00	Description
0	0	Program wait not inserted when external space area 0 is accessed
	1	1 program wait state inserted when external space area 0 is accessed
1	0	2 program wait states inserted when external space area 0 is accessed
	1	3 program wait states inserted when external space area 0 is accessed (Initial value)

4.2.4 Bus Control Register H (BCRH)

Bit	:	7	6	5	4	3	2	1	0
		ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2	RMTS1	RMTS0
Initial value	:	1	1	0	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCRH is an 8-bit readable/writable register that selects enabling or disabling of idle cycle insertion, and the memory interface for areas 2 to 5 and area 0.

BCRH is initialized to H'D0 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Idle Cycle Insert 1 (ICIS1): Selects whether or not one idle cycle state is to be inserted between bus cycles when successive external read cycles are performed in different areas.

Bit 7 ICIS1	Description
0	Idle cycle not inserted in case of successive external read cycles in different areas.
1	Idle cycle inserted in case of successive external read cycles in different areas. (Initial value)

Bit 6—Idle Cycle Insert 0 (ICIS0): Selects whether or not one idle cycle state is to be inserted between bus cycles when successive external read and external write cycles are performed .

Bit 6 ICIS0	Description
0	Idle cycle not inserted in case of successive external read and external write cycles.
1	Idle cycle inserted in case of successive external read and external write cycles. (Initial value)

Bit 5—Burst ROM Enable (BRSTRM): Selects whether area 0 is used as a burst ROM interface area.

Bit 5 BRSTRM	Description
0	Area 0 is basic bus interface area (Initial value)
1	Area 0 is burst ROM interface area

Bit 4—Burst Cycle Select 1 (BRSTS1): Selects the number of burst cycles for the burst ROM interface.

Bit 4 BRSTS1	Description	
0	Burst cycle comprises 1 state	
1	Burst cycle comprises 2 states	(Initial value)

Bit 3—Burst Cycle Select 0 (BRSTS0): Selects the number of words that can be accessed in a burst access on the burst ROM interface.

Bit 3 BRSTS0	Description	
0	Max. 4 words in burst access	(Initial value)
1	Max. 8 words in burst access	

Bits 2 to 0—RAM Type Select (RMTS2 to RMTS0): These bits select the memory interface for areas 2 to 5 in advanced mode.

When DRAM space is selected, the relevant area is designated as a DRAM interface area.

Bit 2	Bit 1	Bit 0	Description			
RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	0	Normal space	Normal space	Normal space	Normal space
		1	Normal space	Normal space	Normal space	DRAM space
	1	0	Normal space	Normal space	DRAM space	DRAM space
		1	DRAM space	DRAM space	DRAM space	DRAM space
1	—	—	—	—	—	—

The $\overline{\text{LCAS}}$ pin is used for the $\overline{\text{LCAS}}$ signal on the 2-CAS DRAM interface. If it is wished to use $\overline{\text{BREQO}}$ output when using the $\overline{\text{LCAS}}$ signal, it is possible to switch to the P53 pin by means of the BREQOPS bit in PFCR2. For details, see section 5.6, Port 5 and section 5.16, Port F.

4.2.5 Bus Control Register L (BCRL)

Bit	:	7	6	5	4	3	2	1	0
		BRLE	BREQOE	EAE	—	DDS	—	WDBE	WAITE
Initial value	:	0	0	1	1	1	1	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCRL is an 8-bit readable/writable register that performs selection of the external bus-released state protocol, selection of the area partition unit, enabling or disabling of the write data buffer function, and enabling or disabling of $\overline{\text{WAIT}}$ pin input.

BCRL is initialized to H'3C by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Bus Release Enable (BRLE): Enables or disables external bus release.

Bit 7 BRLE	Description
0	External bus release disabled. $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, and $\overline{\text{BREQO}}$ pins can be used as I/O ports (Initial value)
1	External bus release enabled

Bit 6—BREQO Pin Enable (BREQOE): Outputs a signal that requests the external bus master to drop the bus request signal ($\overline{\text{BREQ}}$) in the external bus-released state, when an internal bus master performs an external space access, or when a refresh request is generated.

Bit 6 BREQOE	Description
0	$\overline{\text{BREQO}}$ output disabled. $\overline{\text{BREQO}}$ pin can be used as I/O port (Initial value)
1	$\overline{\text{BREQO}}$ output enabled

Bit 5—External Address Enable (EAE): Designates addresses H'010000 to H'03FFFF*[2] as either internal or external addresses.

Bit 5	Description		
EAE	**H8S/2339, H8S/2338**	**H8S/2337**	**H8S/2332**
0	On-chip ROM	Addresses H'010000 to H'01FFFF are on-chip ROM or addresses H'020000 to H'03FFFF are reserved area*[1]	Reserved area*[1]
1	Addresses H'010000 to H'03FFFF are external addresses in external expanded mode or reserved area*[1] in single-chip mode		

Notes: 1. Do not access a reserved area..
2. Addresses H'010000 to H'05FFFF in the H8S/2339.

Bit 4—Reserved

Bit 3—DACK Timing Select (DDS): Selects the DMAC single address transfer bus timing for the DRAM interface.

Bit 3 DDS	Description	
0	When DMAC single address transfer is performed in DRAM space, full access is always executed. $\overline{\text{DACK}}$ signal goes low from Tr or T1 cycle	
1	Burst access is possible when DMAC single address transfer is performed in DRAM space. $\overline{\text{DACK}}$ signal goes low from Tc1 or T2 cycle	(Initial value)

Bit 2—Reserved

Bit 1—Write Data Buffer Enable (WDBE): Selects whether or not the write buffer function is used for an external write cycle or DMAC single address cycle.

Bit 1 WDBE	Description	
0	Write data buffer function not used	(Initial value)
1	Write data buffer function used	

Bit 0—WAIT Pin Enable (WAITE): Selects enabling or disabling of wait input by the $\overline{\text{WAIT}}$ pin.

Bit 0 WAITE	Description	
0	Wait input by $\overline{\text{WAIT}}$ pin disabled. $\overline{\text{WAIT}}$ pin can be used as I/O port	(Initial value)
1	Wait input by $\overline{\text{WAIT}}$ pin enabled	

4.2.6 Memory Control Register (MCR)

Bit	:	7	6	5	4	3	2	1	0
		TPC	BE	RCDM	—	MXC1	MXC0	RLW1	RLW0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MCR is an 8-bit readable/writable register that selects the DRAM strobe control method, number of precharge cycles, access mode, address multiplexing shift size, and the number of wait states inserted during refreshing, when areas 2 to 5 are designated as DRAM interface areas.

MCR is initialized to H'00 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—TP Cycle Control (TPC): Selects whether a 1-state or 2-state precharge cycle (T_P) is to be used when areas 2 to 5 designated as DRAM space are accessed.

Bit 7 TPC	Description	
0	1-state precharge cycle is inserted	(Initial value)
1	2-state precharge cycle is inserted	

Bit 6—Burst Access Enable (BE): Selects enabling or disabling of burst access to areas 2 to 5 designated as DRAM space. DRAM space burst access is performed in fast page mode.

Bit 6 BE	Description	
0	Burst disabled (always full access)	(Initial value)
1	DRAM space access performed in fast page mode	

Bit 5—RAS Down Mode (RCDM): When areas 2 to 5 are designated as DRAM space and access to DRAM is interrupted, RCDM selects whether the $\overline{RAS}$ signal is held low while waiting for the next DRAM access (RAS down mode), or is driven high again (RAS up mode).

Bit 5 RCDM	Description	
0	RAS up mode selected for DRAM interface	(Initial value)
1	RAS down mode selected for DRAM interface	

Bit 4—Reserved

Bits 3 and 2—Multiplex Shift Count 1 and 0 (MXC1, MXC0): These bits select the size of the shift toward the lower half of the row address in row address/column address multiplexing for the DRAM interface. In burst operation on the DRAM interface, these bits also select the row address bits to be used for comparison.

Bit 3 MXC1	Bit 2 MXC0	Description
0	0	8-bit shift (Initial value) • When 8-bit access space is designated: Row address bits A_{23} to A_8 used for comparison • When 16-bit access space is designated: Row address bits A_{23} to A_9 used for comparison
	1	9-bit shift • When 8-bit access space is designated: Row address bits A_{23} to A_9 used for comparison • When 16-bit access space is designated: Row address bits A_{23} to A_{10} used for comparison
1	0	10-bit shift • When 8-bit access space is designated: Row address bits A_{23} to A_{10} used for comparison • When 16-bit access space is designated: Row address bits A_{23} to A_{11} used for comparison
	1	—

Bits 1 and 0—Refresh Cycle Wait Control 1 and 0 (RLW1, RLW0): These bits select the number of wait states to be inserted in a DRAM interface CAS-before-RAS refresh cycle. This setting is used for all areas designated as DRAM space. Wait input by the $\overline{\text{WAIT}}$ pin is disabled.

Bit 1 RLW1	Bit 0 RLW0	Description
0	0	No wait state inserted (Initial value)
	1	1 wait state inserted
1	0	2 wait states inserted
	1	3 wait states inserted

4.2.7 DRAM Control Register (DRAMCR)

Bit	:	7	6	5	4	3	2	1	0
		RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DRAMCR is an 8-bit readable/writable register that selects the DRAM refresh mode and refresh counter clock and controls the refresh timer.

DRAMCR is initialized to H'00 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Refresh Control (RFSHE): Selects whether or not refresh control is performed. When refresh control is not performed, the refresh timer can be used as an interval timer.

Bit 7 RFSHE	Description	
0	Refresh control is not performed	(Initial value)
1	Refresh control is performed	

Bit 6—RAS-CAS Wait (RCW): Controls wait state insertion in DRAM interface CAS-before-RAS refreshing.

Bit 6 RCW	Description	
0	Wait state insertion in CAS-before-RAS refreshing disabled $\overline{RAS}$ falls in Tr cycle	(Initial value)
1	One wait state inserted in CAS-before-RAS refreshing $\overline{RAS}$ falls in Tc1 cycle	

Bit 5—Refresh Mode (RMODE): Selects whether self-refreshing is performed in software standby mode.

Bit 5 RMODE	Description	
0	Self-refreshing is not performed in software standby mode	(Initial value)
1	Self-refreshing is performed in software standby mode	

Bit 4—Compare Match Flag (CMF): Status flag that indicates a match between the values of RTCNT and RTCOR.

When refresh control is performed (RFSHE = 1), 1 should be written to the CMF bit when writing to DRAMCR.

Bit 4 CMF	Description	
0	[Clearing condition]	
	When 0 is written to CMF after reading CMF = 1	(Initial value)
1	[Setting condition]	
	When RTCNT = RTCOR	

Bit 3—Compare Match Interrupt Enable (CMIE): Enables or disables interrupt requests (CMI) by the CMF flag when the CMF flag in DRAMCR is set to 1.

When refresh control is performed (RFSHE = 1), the CMIE bit is always cleared to 0.

Bit 3 CMIE	Description	
0	Interrupt request (CMI) by CMF flag disabled	(Initial value)
1	Interrupt request (CMI) by CMF flag enabled	

Bits 2 to 0—Refresh Counter Clock Select (CKS2 to CKS0): These bits select the clock to be input to RTCNT from among seven clocks obtained by dividing the system clock (ø). When the input clock is selected with bits CKS2 to CKS0, RTCNT begins counting up.

Bit 2 CKS2	Bit 1 CKS1	Bit 0 CKS0	Description	
0	0	0	Count operation disabled	(Initial value)
		1	Count uses ø/2	
	1	0	Count uses ø/8	
		1	Count uses ø/32	
1	0	0	Count uses ø/128	
		1	Count uses ø/512	
	1	0	Count uses ø/2048	
		1	Count uses ø/4096	

4.2.8 Refresh Timer Counter (RTCNT)

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCNT is an 8-bit readable/writable up-counter.

RTCNT counts up using the internal clock selected by bits CKS2 to CKS0 in DRAMCR.

When RTCNT matches RTCOR (compare match), the CMF flag in DRAMCR is set to 1 and RTCNT is cleared to H'00. If the RFSHE bit in DRAMCR is set to 1 at this time, a refresh cycle is started. Also, if the CMIE bit in DRAMCR is set to 1, a compare match interrupt (CMI) is generated.

RTCNT is initialized to H'00 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

4.2.9 Refresh Time Control Register (RTCOR)

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCOR is an 8-bit readable/writable register that sets the period for compare match operations with RTCNT.

The values of RTCOR and RTCNT are constantly compared, and if they match, the CMF flag in DRAMCR is set to 1 and RTCNT is cleared to H'00.

RTCOR is initialized to H'FF by a reset, and in hardware standby mode. It is not initialized in software standby mode.

4.3 Overview of Bus Control

4.3.1 Area Partitioning

In advanced mode, the bus controller partitions the 16-Mbyte address space into eight areas, 0 to 7, in 2-Mbyte units, and performs bus control for external space in area units. Figure 4.2 shows an outline of the memory map.

Chip select signals ($\overline{CS}_0$ to $\overline{CS}_7$) can be output for each area.

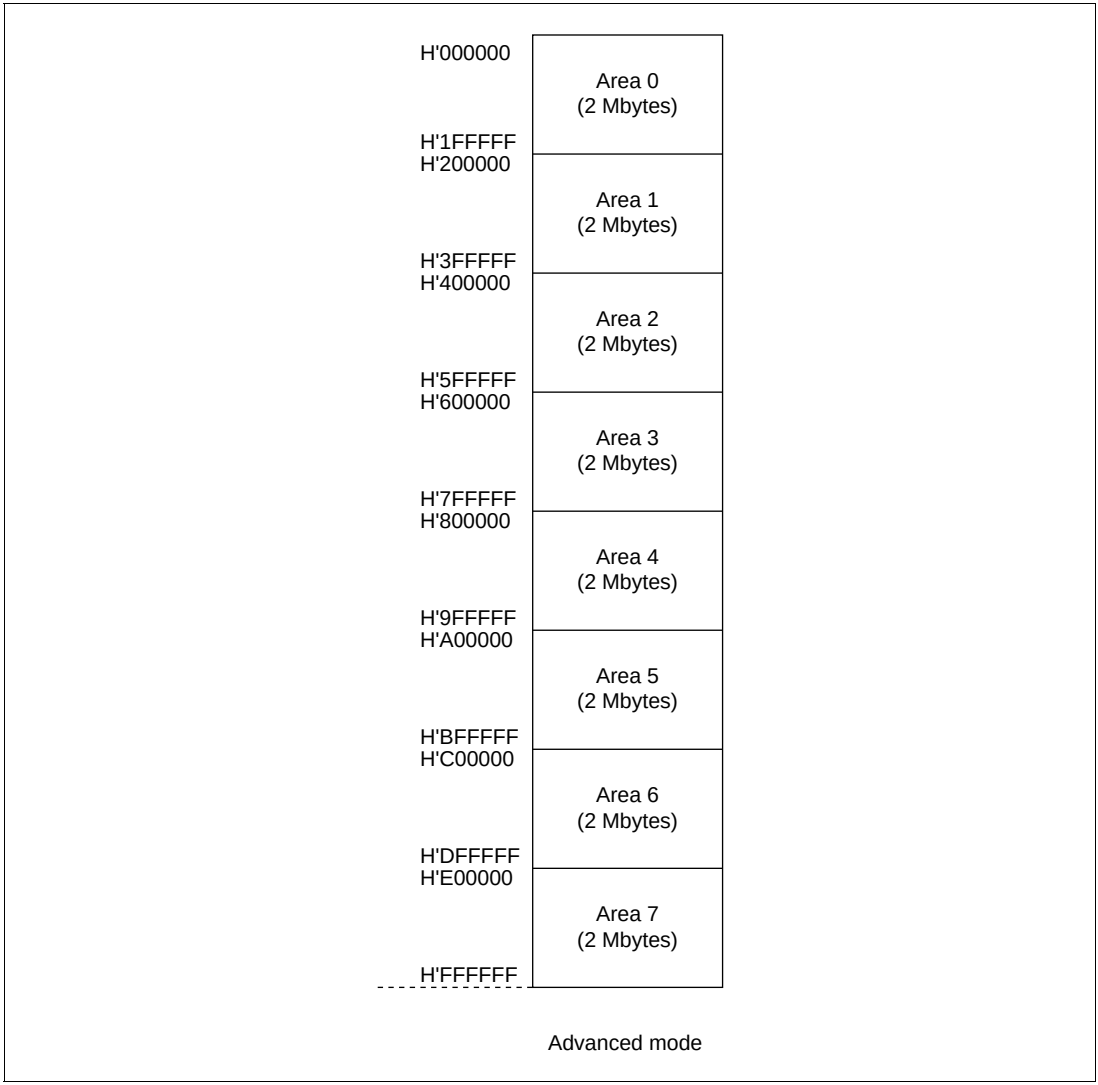


Figure 4.2 Area Partitioning

4.3.2 Bus Specifications

The external space bus specifications consist of three elements: (1) bus width, (2) number of access states, and (3) number of program wait states.

The bus width and number of access states for on-chip memory and internal I/O registers are fixed, and are not affected by the bus controller.

Bus Width: A bus width of 8 or 16 bits can be selected with ABWCR. An area for which an 8-bit bus is selected functions as an 8-bit access space, and an area for which a 16-bit bus is selected functions as a16-bit access space.

If all areas are designated for 8-bit access, 8-bit bus mode is set; if any area is designated for 16-bit access, 16-bit bus mode is always set. When the burst ROM interface is selected, 16-bit bus mode is always set.

Number of Access States: Two or three access states can be selected with ASTCR. An area for which 2-state access is selected functions as a 2-state access space, and an area for which 3-state access is selected functions as a 3-state access space.

With the DRAM interface and burst ROM interface, the number of access states may be determined without regard to ASTCR.

When 2-state access space is designated, wait insertion is disabled.

Number of Program Wait States: When 3-state access space is designated by ASTCR, the number of program wait states to be inserted automatically is selected with WCRH and WCRL. From 0 to 3 program wait states can be selected.

Table 4.3 shows the bus specifications for each basic bus interface area.

Table 4.3 Bus Specifications for Each Area (Basic Bus Interface)

ABWCR	ASTCR	WCRH, WCRL		Bus Specifications (Basic Bus Interface)		
ABWn	ASTn	Wn1	Wn0	Bus Width	Access States	Program Wait States
0	0	—	—	16	2	0
	1	0	0		3	0
			1			1
		1	0			2
			1			3
1	0	—	—	8	2	0
	1	0	0		3	0
			1			1
		1	0			2
			1			3

4.3.3 Memory Interfaces

The memory interfaces of the H8S/2339 and H8S/2338 Series comprise a basic bus interface that allows direct connection of ROM, SRAM, and so on; a DRAM interface that allows direct connection of DRAM; and a burst ROM interface that allows direct connection of burst ROM. The interface can be selected independently for each area.

An area for which the basic bus interface is designated functions as normal space, an area for which the DRAM interface is designated functions as DRAM space, and an area for which the burst ROM interface is designated functions as burst ROM space.

4.3.4 Advanced Mode

The initial state of each area is basic bus interface, 3-state access space. The initial bus width is selected according to the operating mode. The bus specifications described here cover basic items only, and the sections on each memory interface (4.4, 4.5, and 4.7) should be referred to for further details.

Area 0: Area 0 includes on-chip ROM, and in expanded mode with on-chip ROM disabled, all of area 0 is external space. In expanded mode with on-chip ROM enabled, the space excluding on-chip ROM is external space.

When area 0 external space is accessed, the $\overline{CS}_0$ signal can be output.

Either basic bus interface or burst ROM interface can be selected for area 0.

Areas 1 and 6: In external expanded mode, all of area 1 and area 6 is external space.

When area 1 and 6 external space is accessed, the $\overline{CS}_1$ and $\overline{CS}_6$ pin signals can be output, respectively.

Only the basic bus interface can be used for areas 1 and 6.

Areas 2 to 5: In external expanded mode, areas 2 to 5 are all external space.

When area 2 to 5 external space is accessed, signals $\overline{CS}_2$ to $\overline{CS}_5$ can be output.

Basic bus interface or DRAM interface can be selected for areas 2 to 5. With the DRAM interface, signals $\overline{CS}_2$ to $\overline{CS}_5$ are used as $\overline{RAS}$ signals.

Area 7: Area 7 includes the on-chip RAM and internal/O registers. In external expanded mode, the space excluding the on-chip RAM and internal/O registers is external space. The on-chip RAM is enabled when the RAME bit in the system control register (SYSCR) is set to 1; when the RAME bit is cleared to 0, the on-chip RAM is disabled and the corresponding space becomes external space .

When area 7 external space is accessed, the $\overline{CS}_7$ signal can be output.

Only the basic bus interface can be used for the area 7 memory interface.

4.3.5 Chip Select Signals

The chip can output chip select signals ($\overline{CS_0}$ to $\overline{CS_7}$) to areas 0 to 7, the signal being driven low when the corresponding external space area is accessed.

Figure 4.3 shows an example of $\overline{CS_n}$ (n = 0 to 7) output timing.

Enabling or disabling of $\overline{CS_n}$ signal output is performed by setting the data direction register (DDR) bit for the port corresponding to the particular $\overline{CS_n}$ pin.

In expanded mode with on-chip ROM disabled, the $\overline{CS_0}$ pin is placed in the output state after a reset. Pins CS_1 to CS_7 are placed in the input state after a reset, and so the corresponding DDR bits should be set to 1 when outputting signals $\overline{CS_1}$ to $\overline{CS_7}$.

In expanded mode with on-chip ROM enabled, pins $\overline{CS_0}$ to $\overline{CS_7}$ are all placed in the input state after a reset, and so the corresponding DDR bits should be set to 1 when outputting signals $\overline{CS_0}$ to $\overline{CS_7}$.

For details, see section 5, I/O Ports.

When areas 2 to 5 are designated as DRAM space, outputs $\overline{CS_2}$ to $\overline{CS_5}$ are used as $\overline{RAS}$ signals.

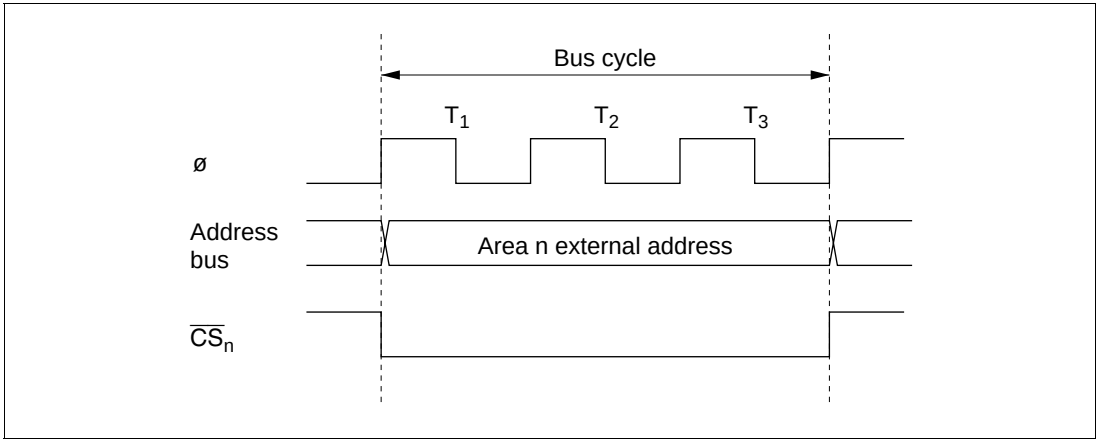


Figure 4.3 $\overline{CS_n}$ Signal Output Timing (n = 0 to 7)

4.4 Basic Bus Interface

4.4.1 Overview

The basic bus interface enables direct connection of ROM, SRAM, and so on.

The bus specifications can be selected with ABWCR, ASTCR, WCRH, and WCRL. For details, see section 4.4, Basic Bus Interface, in the Hardware Manual.

4.4.2 Wait Control

When accessing external space , the chip can extend the bus cycle by inserting one or more wait states (T_w). There are two ways of inserting wait states: program wait insertion and pin wait insertion using the $\overline{\text{WAIT}}$ pin.

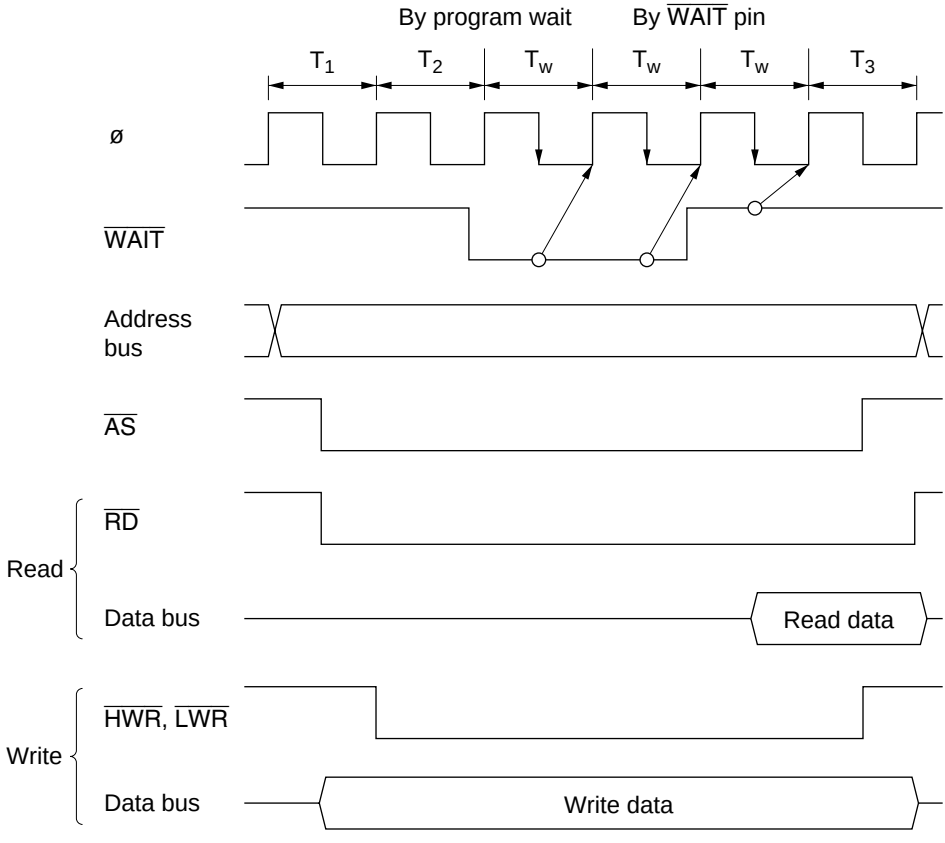
Program Wait Insertion: From 0 to 3 wait states can be inserted automatically between the T_2 state and T_3 state on an individual area basis in 3-state access space, according to the settings in WCRH and WCRL.

Pin Wait Insertion: Setting the WAITE bit in BCRL to 1 enables wait input by means of the $\overline{\text{WAIT}}$ pin. When external space is accessed in this state, a program wait is first inserted in accordance with the settings in WCRH and WCRL. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of ø in the last T_2 or T_w state, another T_w state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_w states are inserted it goes high.

This is useful when inserting four or more T_w states, or when changing the number of T_w states for different external devices.

The WAITE bit setting applies to all areas. The WAITPS bit can be used to change the $\overline{\text{WAIT}}$ input pin from $P8_6$ to $P5_3$. To make this change, select the input pin with the WAITPS bit, then set the WAITE bit.

Figure 4.4 shows an example of wait state insertion timing.



Note: Downward arrows indicates the timing of $\overline{\text{WAIT}}$ pin sampling.

Figure 4.4 Example of Wait State Insertion Timing

The settings after a reset are: 3-state access, 3 program wait state insertion, and WAIT input disabled.

4.5 DRAM Interface

4.5.1 Overview

When the chip is in advanced mode, external space areas 2 to 5 can be designated as DRAM space, and DRAM interfacing performed. With the DRAM interface, DRAM can be directly connected to the chip. A DRAM space of 2, 4, or 8 Mbytes can be set by means of bits RMTS2 to RMTS0 in BCRH. Burst operation is also possible, using fast page mode.

4.5.2 Setting DRAM Space

Areas 2 to 5 are designated as DRAM space by setting bits RMTS2 to RMTS0 in BCRH. The relation between the settings of bits RMTS2 to RMTS0 and DRAM space is shown in table 4.4. Possible DRAM space settings are: one area (area 2), two areas (areas 2 and 3), and four areas (areas 2 to 5).

Table 4.4 DRAM Space Settings by Bits RMTS2 to RMTS0

RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	1	Normal space	Normal space	Normal space	DRAM space
	1	0	Normal space	Normal space	DRAM space	DRAM space
		1	DRAM space	DRAM space	DRAM space	DRAM space

4.5.3 Address Multiplexing

With DRAM space, the row address and column address are multiplexed. In address multiplexing, the size of the shift of the row address is selected with bits MXC1 and MXC0 in MCR. Table 4.5 shows the relation between the settings of MXC1 and MXC0 and the shift size.

Table 4.5 Address Multiplexing Settings by Bits MXC1 and MXC0

	MCR			Address Pins														
	MXC1	MXC0	Shift Size	A_{23} to A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Row address	0	0	8 bits	A_{23} to A_{13}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
		1	9 bits	A_{23} to A_{13}	A_{12}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9
	1	0	10 bits	A_{23} to A_{13}	A_{12}	A_{11}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}
		1	Setting pro-hibited	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Column address	—	—	—	A_{23} to A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

4.5.4 Data Bus

If the bit in ABWCR corresponding to an area designated as DRAM space is set to 1, that area is designated as 8-bit DRAM space; if the bit is cleared to 0, the area is designated as 16-bit DRAM space. In 16-bit DRAM space, ×16-bit configuration DRAM can be connected directly.

In 8-bit DRAM space the upper half of the data bus, D_{15} to D_8, is enabled, while in 16-bit DRAM space both the upper and lower halves of the data bus, D_{15} to D_0, are enabled.

Access sizes and data alignment are the same as for the basic bus interface. For details, see section 4.4.2, Data Size and Data Alignment, in the Hardware Manual.

4.5.5 Pins Used for DRAM Interface

Table 4.6 shows the pins used for DRAM interfacing and their functions.

Table 4.6 DRAM Interface Pins

Pin	With DRAM Setting	Name	I/O	Function
$\overline{HWR}$	$\overline{WE}$	Write enable	Output	Write enable for DRAM space access when 2-CAS access is set
$\overline{LCAS}$	$\overline{LCAS}$	Lower column address strobe	Output	Lower column address strobe signal for 16-bit DRAM space access
$\overline{CS_2}$	$\overline{RAS2}$	Row address strobe 2	Output	Row address strobe when area 2 is designated as DRAM space
$\overline{CS_3}$	$\overline{RAS3}$	Row address strobe 3	Output	Row address strobe when area 3 is designated as DRAM space
$\overline{CS_4}$	$\overline{RAS4}$	Row address strobe 4	Output	Row address strobe when area 4 is designated as DRAM space
$\overline{CS_5}$	$\overline{RAS5}$	Row address strobe 5	Output	Row address strobe when area 5 is designated as DRAM space
$\overline{CAS}$	$\overline{UCAS}$	Upper column address strobe	Output	Upper column address strobe for DRAM space access
$\overline{WAIT}$	$\overline{WAIT}$	Wait	Input	Wait request signal
A_{12} to A_0	A_{12} to A_0	Address pins	Output	Row address/column address multiplexed output
D_{15} to D_0	D_{15} to D_0	Data pins	I/O	Data input/output pins

4.5.6 Basic Timing

Figure 4.5 shows the basic access timing for DRAM space. The basic DRAM access timing is four states. Unlike the basic bus interface, the corresponding bits in ASTCR control only enabling or disabling of wait insertion, and do not affect the number of access states. When the corresponding bit in ASTCR is cleared to 0, wait states cannot be inserted in the DRAM access cycle.

The four states of the basic timing consist of one T_p (precharge cycle) state, one T_r (row address output cycle) state, and the T_{c1} and T_{c2} (column address output cycle) states.

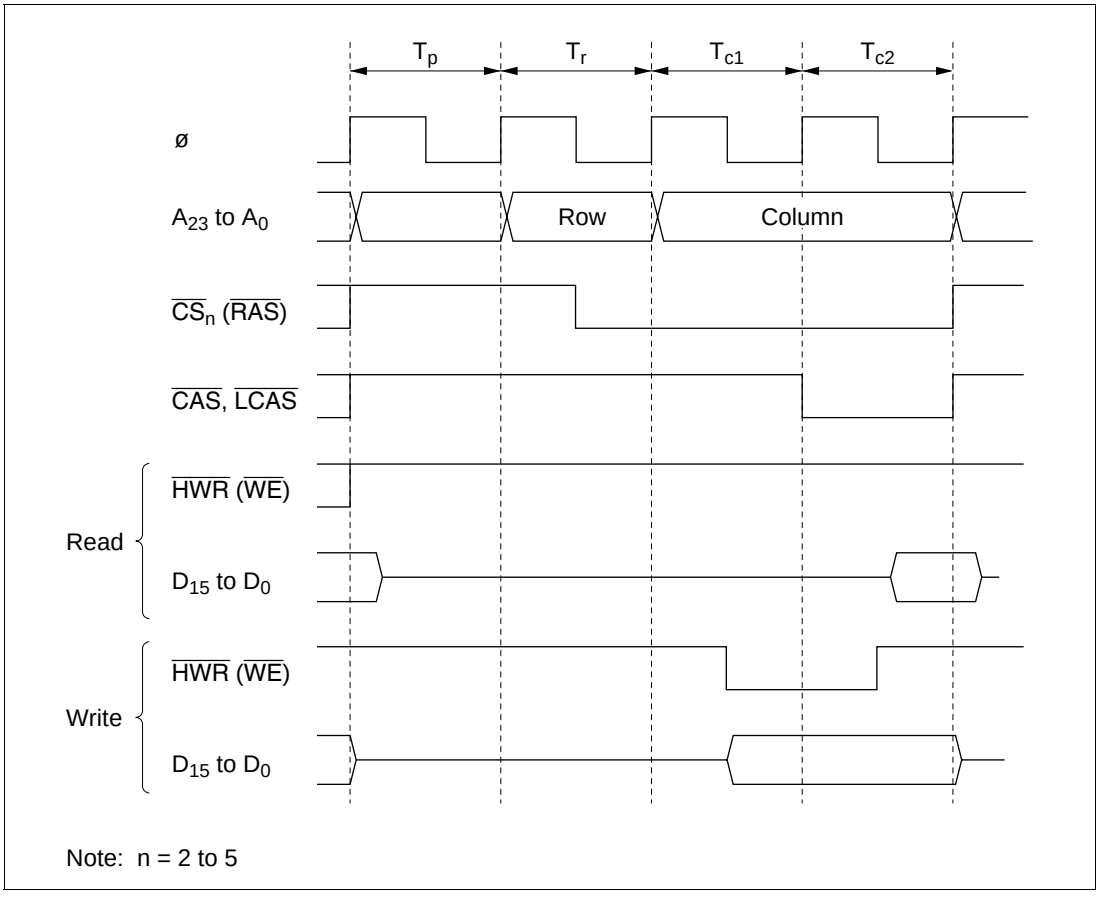


Figure 4.5 Basic Access Timing

4.5.7 Precharge State Control

When DRAM is accessed, RAS precharging time must be secured. With the H8S/2338 Series, one T_p state is always inserted when DRAM space is accessed. This can be changed to two T_p states by setting the TPC bit in MCR to 1. Set the appropriate number of T_p cycles according to the DRAM connected and the operating frequency of the chip. Figure 4.6 shows the timing when two T_p states are inserted.

When the TCP bit is set to 1, two T_p states are also used for refresh cycles.

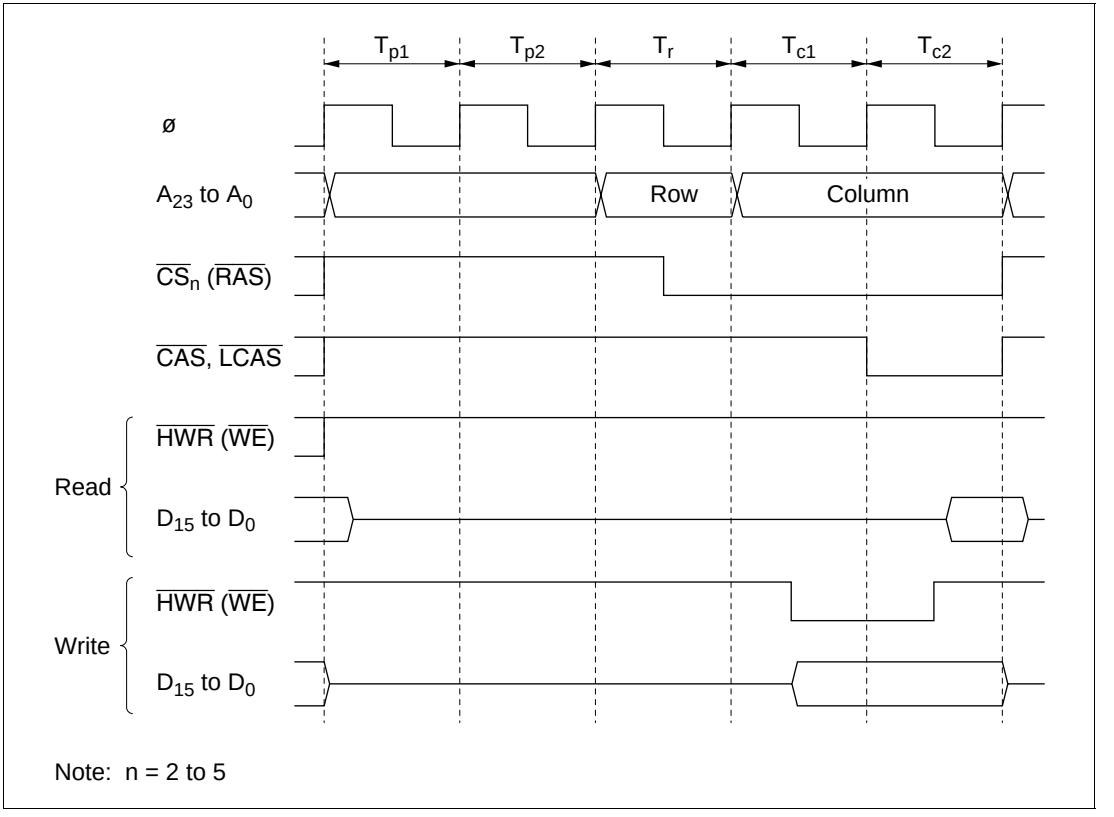


Figure 4.6 Timing with Two-State Precharge Cycle

4.5.8 Wait Control

There are two ways of inserting wait states in a DRAM access cycle: program wait insertion and pin wait insertion using the $\overline{\text{WAIT}}$ pin.

Program Wait Insertion: When the bit in ASTCR corresponding to an area designated as DRAM space is set to 1, from 0 to 3 wait states can be inserted automatically between the T_{c1} state and T_{c2} state, according to the settings of WCRH and WCRL.

Pin Wait Insertion: When the WAITE bit in BCRH is set to 1, wait input by means of the $\overline{\text{WAIT}}$ pin is enabled. When DRAM space is accessed in this state, a program wait is first inserted. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of ø in the last T_{c1} or T_w state, another T_w state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_w states are inserted until it goes high.

Figure 4.7 shows an example of wait state insertion timing.

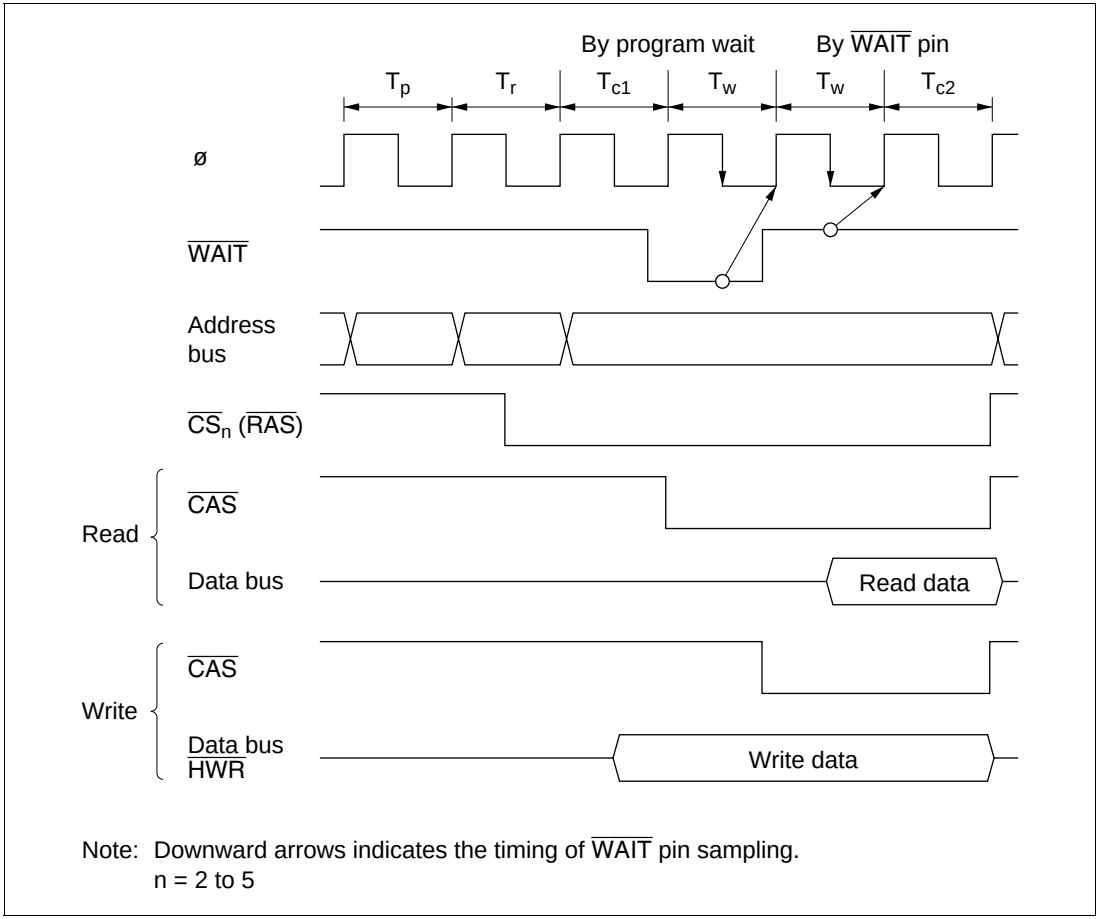


Figure 4.7 Example of Wait State Insertion Timing

4.5.9 Byte Access Control

When DRAM with a ×16 configuration is connected, the 2-CAS access method is used for the control signals needed for byte access.

Figure 4.8 shows the control timing for 2-CAS access, and figure 4.9 shows an example of 2-CAS DRAM connection.

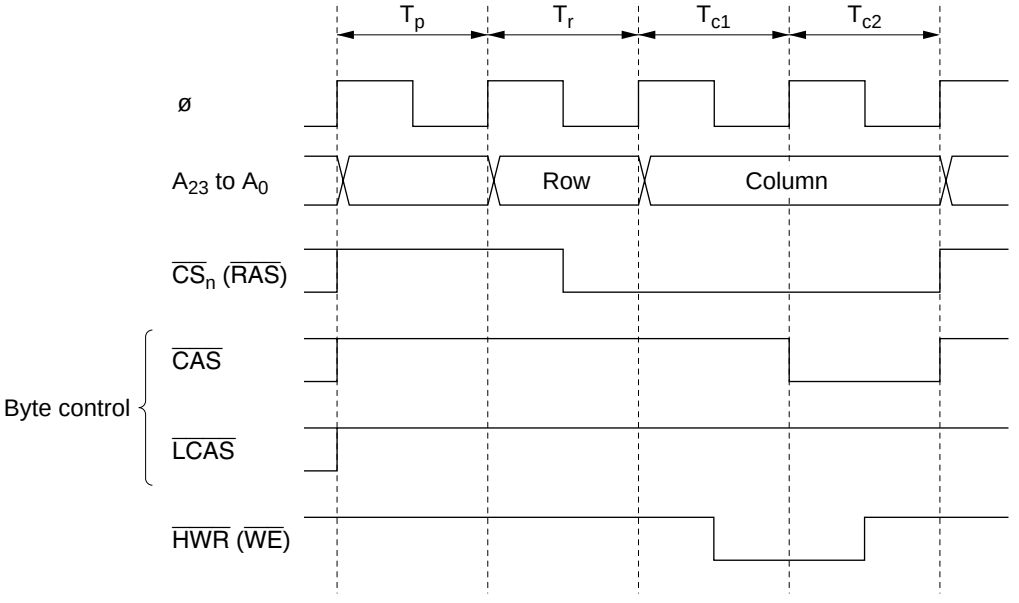


Figure 4.8 2-CAS Control Timing (Upper Byte Write Access)

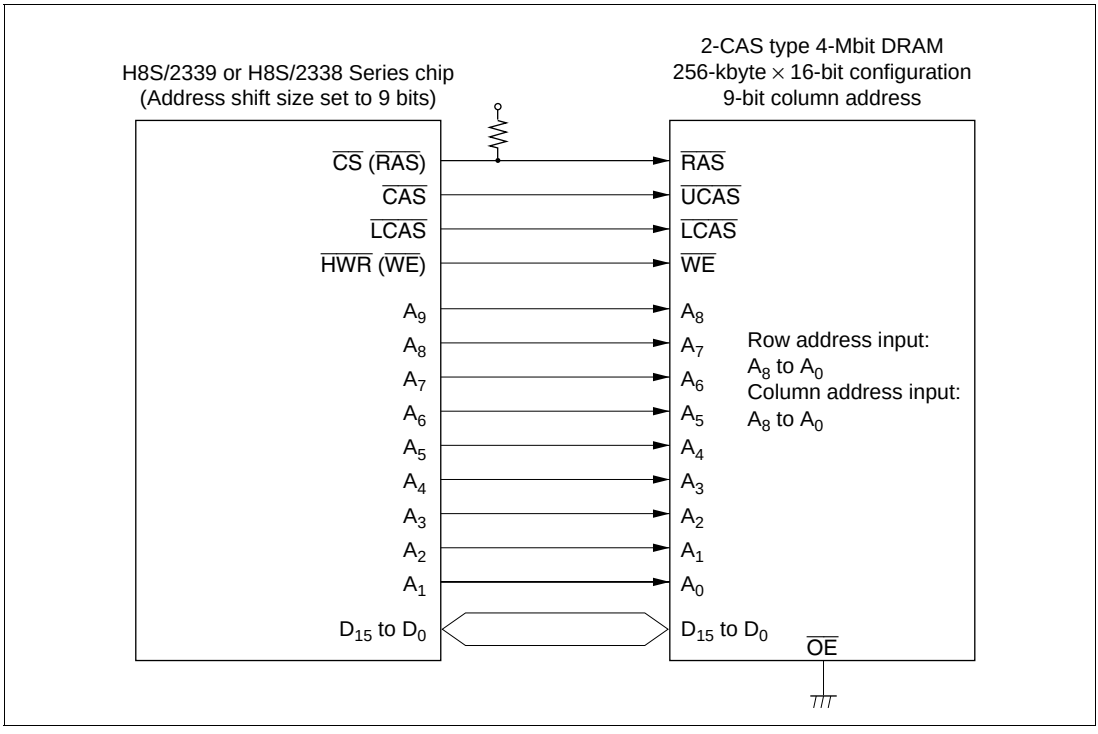


Figure 4.9 Example of 2-CAS DRAM Connection

4.5.10 Burst Operation

With DRAM, in addition to full access (normal access) in which data is accessed by outputting a row address for each access, a fast page mode is also provided which can be used when making a number of consecutive accesses to the same row address. This mode enables fast (burst) access of data by simply changing the column address after the row address has been output. Burst access can be selected by setting the BE bit in MCR to 1.

Burst Access (Fast Page Mode) Operation Timing: Figure 4.10 shows the operation timing for burst access. When there are consecutive access cycles for DRAM space, the $\overline{CAS}$ signal and column address output cycles (two states) continue as long as the row address is the same for consecutive access cycles. The row address used for the comparison is set with bits MXC1 and MXC0 in MCR.

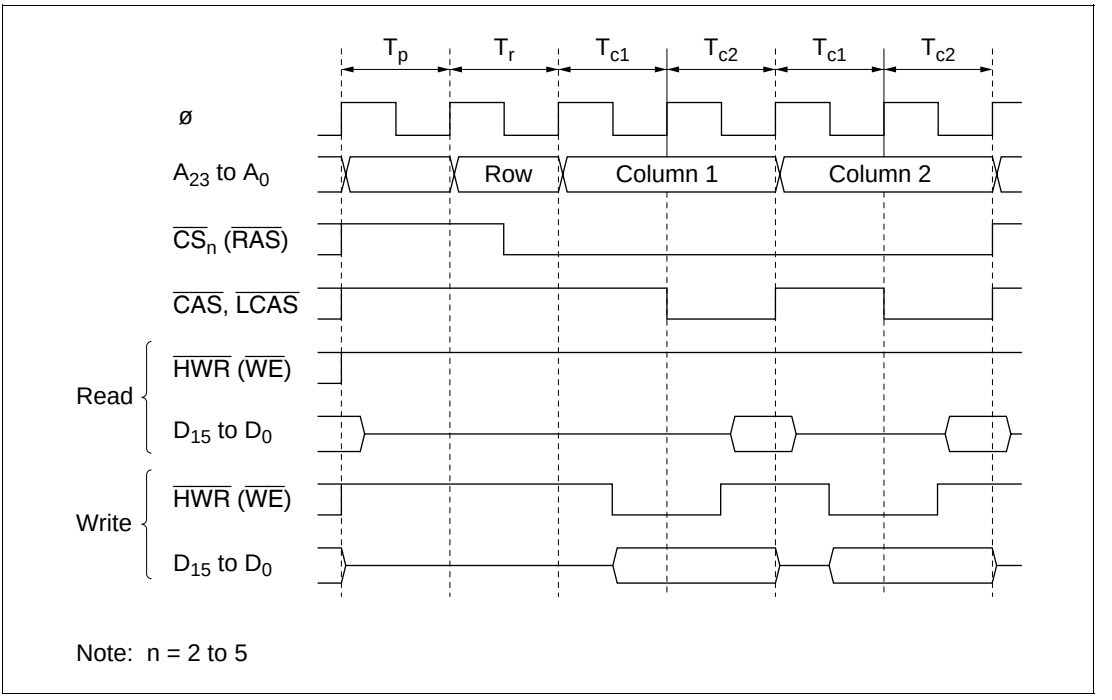


Figure 4.10 Operation Timing in Fast Page Mode

The bus cycle can also be extended in burst access by inserting wait states. The wait state insertion method and timing are the same as for full access. For details, see section 4.5.8, Wait Control.

RAS Down Mode and RAS Up Mode: Even when burst operation is selected, it may happen that access to DRAM space is not continuous, but is interrupted by access to another space. In this case, if the $\overline{RAS}$ signal is held low during the access to the other space, burst operation can be resumed when the same row address in DRAM space is accessed again.

- RAS down mode

  To select RAS down mode, set the RCDM bit in MCR to 1. If access to DRAM space is interrupted and another space is accessed, the $\overline{RAS}$ signal is held low during the access to the other space, and burst access is performed when the row address of the next DRAM space access is the same as the row address of the previous DRAM space access. Figure 4.11 shows an example of the timing in RAS down mode.

  Note, however, that the $\overline{RAS}$ signal will go high if a refresh operation occurs during RAS down mode.

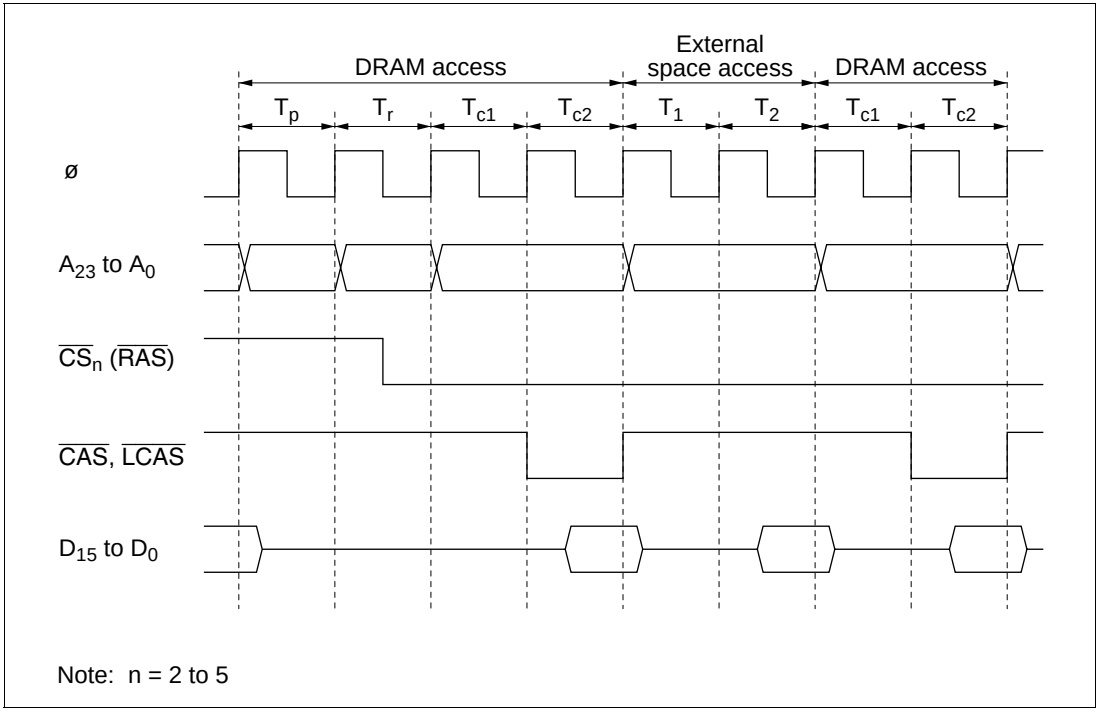


Figure 4.11 Example of Operation Timing in RAS Down Mode

- RAS up mode

  To select RAS up mode, clear the RCDM bit in MCR to 0. Each time access to DRAM space is interrupted and another space is accessed, the $\overline{RAS}$ signal goes high again. Burst operation is only performed if DRAM space is continuous. Figure 4.12 shows an example of the timing in RAS up mode. Note that in burst ROM space access, the $\overline{RAS}$ signal does not return to the high level.

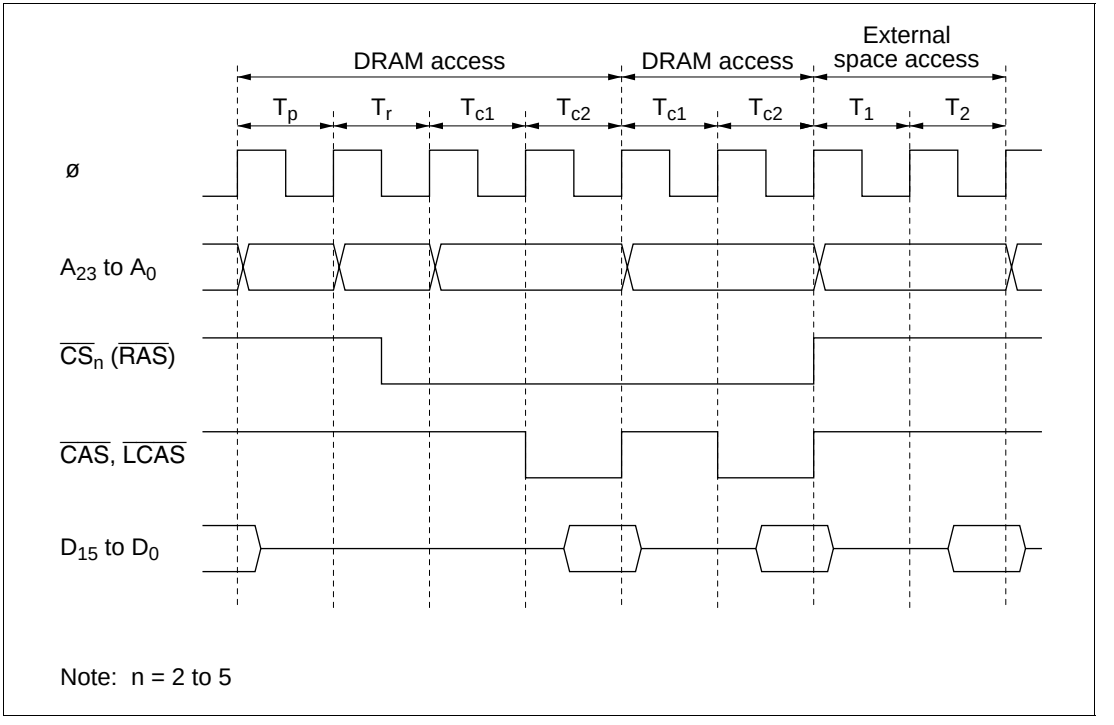


Figure 4.12 Example of Operation Timing in RAS Up Mode

4.5.11 Refresh Control

The H8S/2339 and H8S/2338 Series are provided with a DRAM refresh control function. Either of two refreshing methods can be selected: CAS-before-RAS (CBR) refreshing, or self-refreshing.

CAS-before-RAS (CBR) Refreshing: To select CBR refreshing, set the RFSHE bit in DRAMCR to 1, and clear the RMODE bit to 0.

With CBR refreshing, RTCNT counts up using the input clock selected by bits CKS2 to CKS0 in DRAMCR, and when the count matches the value set in RTCOR (compare match), refresh control is performed. At the same time, RTCNT is reset and starts counting again from H'00. Refreshing is thus repeated at fixed intervals determined by RTCOR and bits CKS2 to CKS0. Set a value in bits CKS2 to CKS0 in RTCOR that will meet the refreshing interval specification for the DRAM used.

When bits CKS2 to CKS0 are set, RTCNT starts counting up. RTCNT and RTCOR settings should therefore be completed before setting bits CKS2 to CKS0.

Do not clear the CMF flag when refresh control is performed (RFSHE = 1).

RTCNT operation is shown in figure 4.13, compare match timing in figure 4.14, and CBR refresh timing in figure 4.15.

Another normal space access can be performed during the CBR refresh interval.

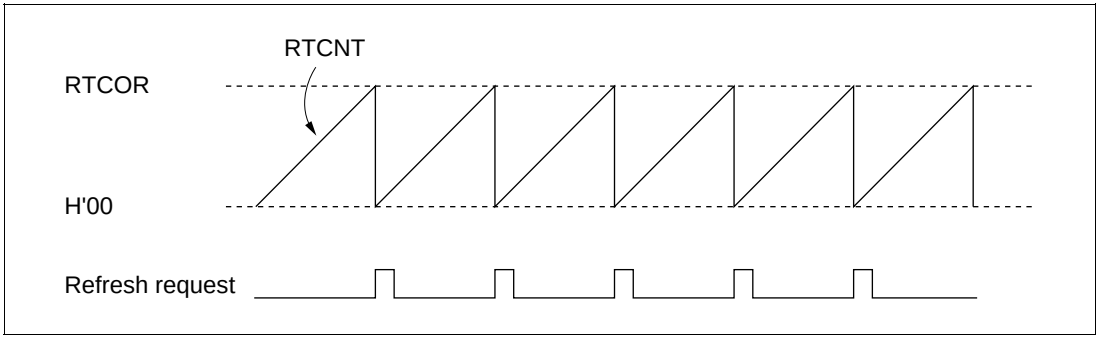


Figure 4.13 RTCNT Operation

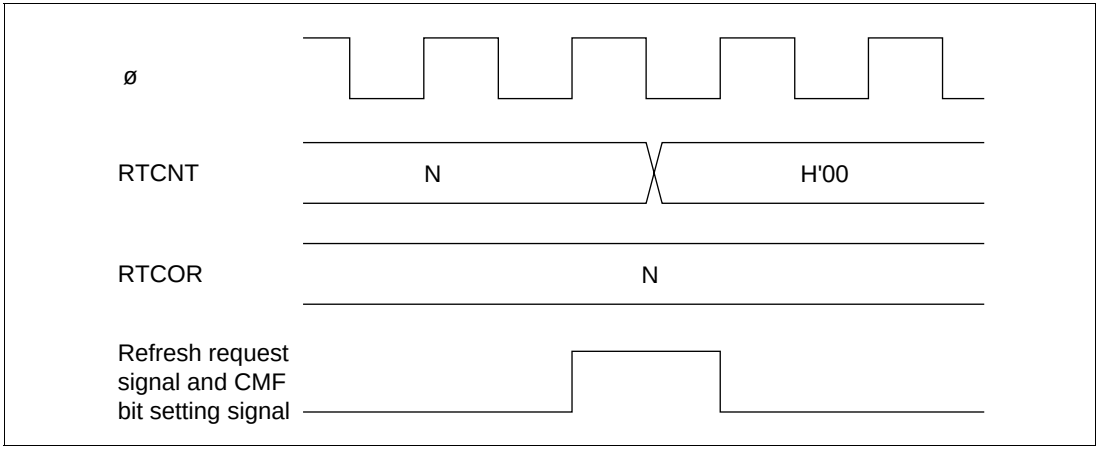


Figure 4.14 Compare Match Timing

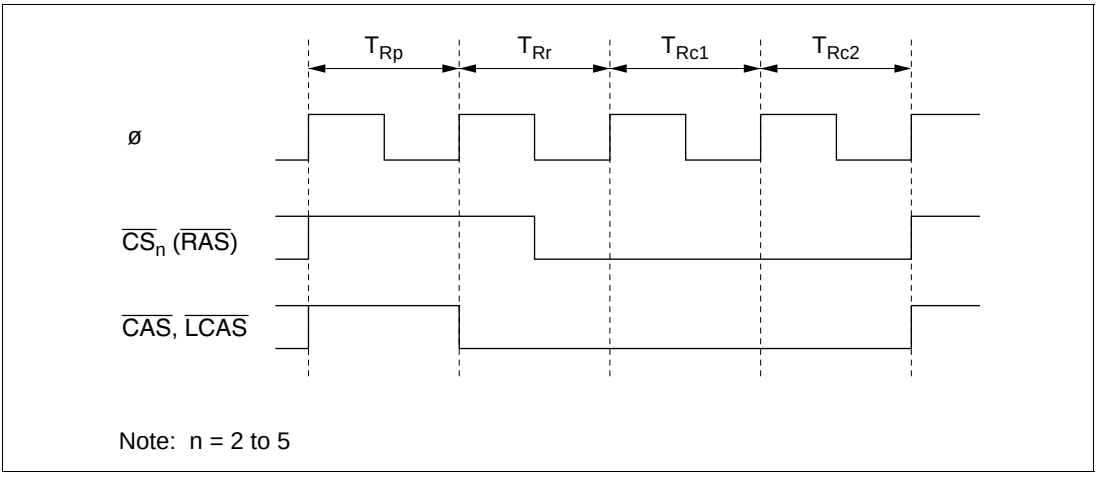


Figure 4.15 CBR Refresh Timing

When the RCW bit is set to 1, $\overline{RAS}$ signal output is delayed by one cycle. Use bits RLW1 and RLW0 to adjust the width of the $\overline{RAS}$ signal. These bits are only enabled in refresh operations.

Figure 4.16 shows the timing when the RCW bit is set to 1.

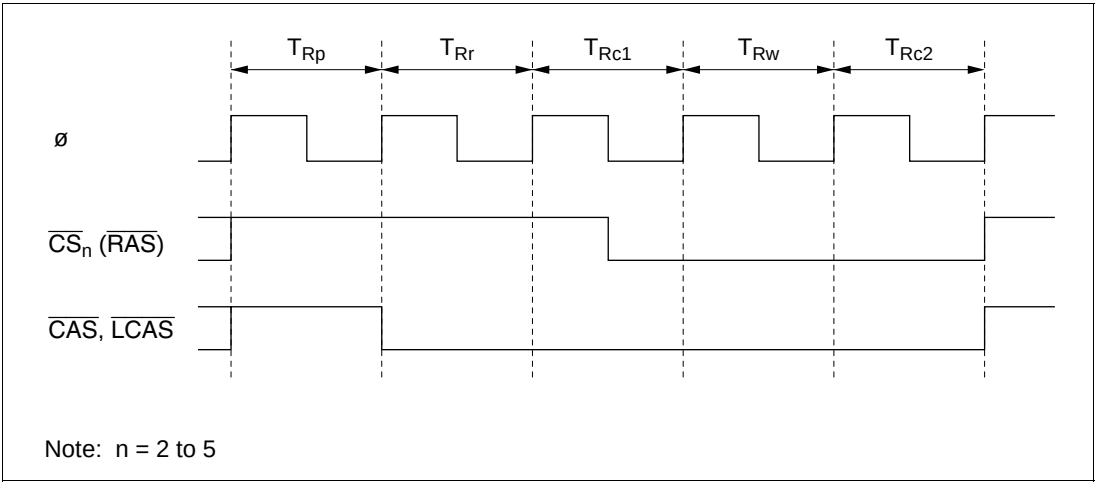


Figure 4.16 CBR Refresh Timing (When RCW = 1, RLW1 = 0, RLW0 = 1)

Self-Refreshing: A self-refresh mode (battery backup mode) is provided for DRAM as a kind of standby mode. In this mode, refresh timing and refresh addresses are generated within the DRAM.

To select self-refreshing, set the RFSHE bit and RMODE bit in DRAMCR to 1. When a SLEEP instruction is executed to enter software standby mode, the $\overline{CAS}$ and $\overline{RAS}$ signals are output and DRAM enters self-refresh mode, as shown in figure 4.17.

When software standby mode is exited, the RMODE bit is cleared to 0 and self-refresh mode is exited.

If a CBR refresh request occurs when making a transition to software standby mode, CBR refreshing is executed, then self-refresh mode is entered.

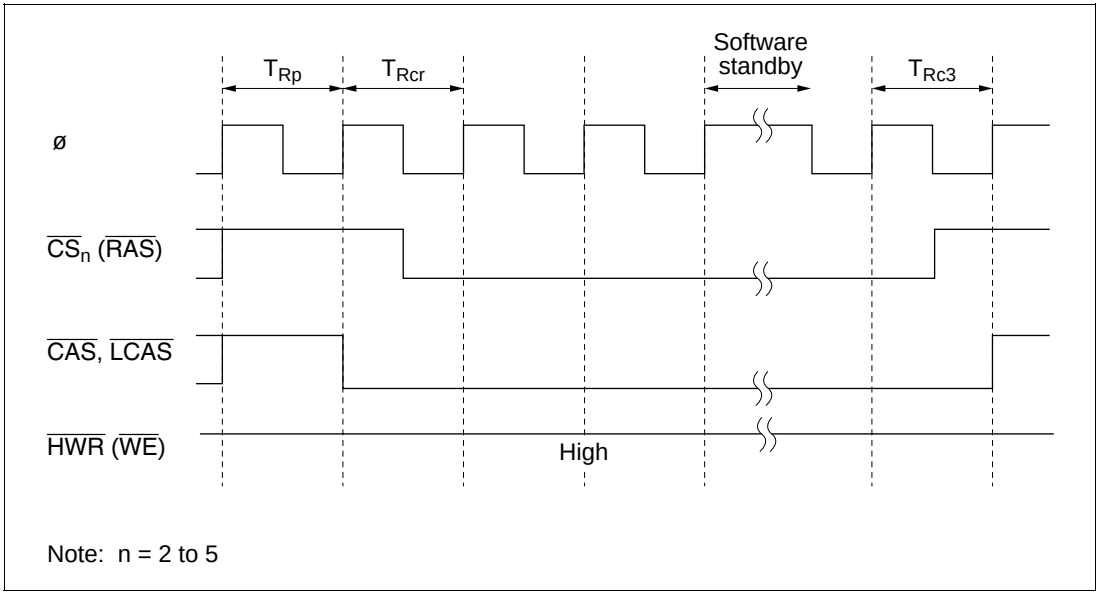


Figure 4.17 Self-Refresh Timing

4.6 DMAC Single Address Mode and DRAM Interface

When burst mode is selected with the DRAM interface, the $\overline{\text{DACK}}$ output timing can be selected with the DDS bit. When DRAM space is accessed in DMAC single address mode at the same time, the DDS bit selects whether or not burst access is to be performed.

4.6.1 When DDS = 1

Burst access is performed by determining the address only, irrespective of the bus master. With the DRAM interface, the $\overline{\text{DACK}}$ output goes low from the T_{c1} state.

Figure 4.18 shows the $\overline{\text{DACK}}$ output timing for the DRAM interface when DDS = 1.

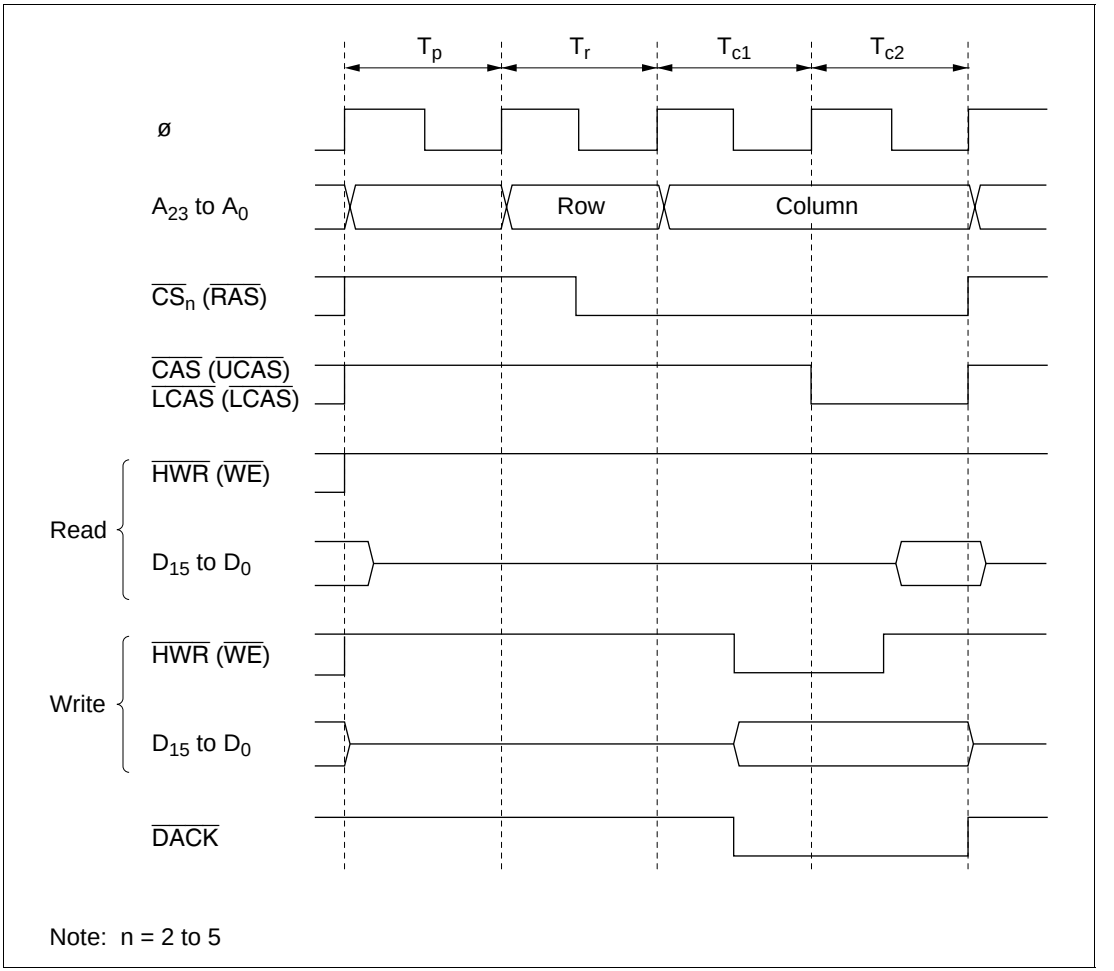


Figure 4.18 $\overline{\text{DACK}}$ Output Timing when DDS = 1 (Example of DRAM Access)

4.6.2 When DDS = 0

When DRAM space is accessed in DMAC single address mode, full access (normal access) is always performed. With the DRAM interface, the $\overline{\text{DACK}}$ output goes low from the T_r state.

In modes other than DMAC single address mode, burst access can be used when accessing DRAM space.

Figure 4.19 shows the $\overline{\text{DACK}}$ output timing for the DRAM interface when DDS = 0.

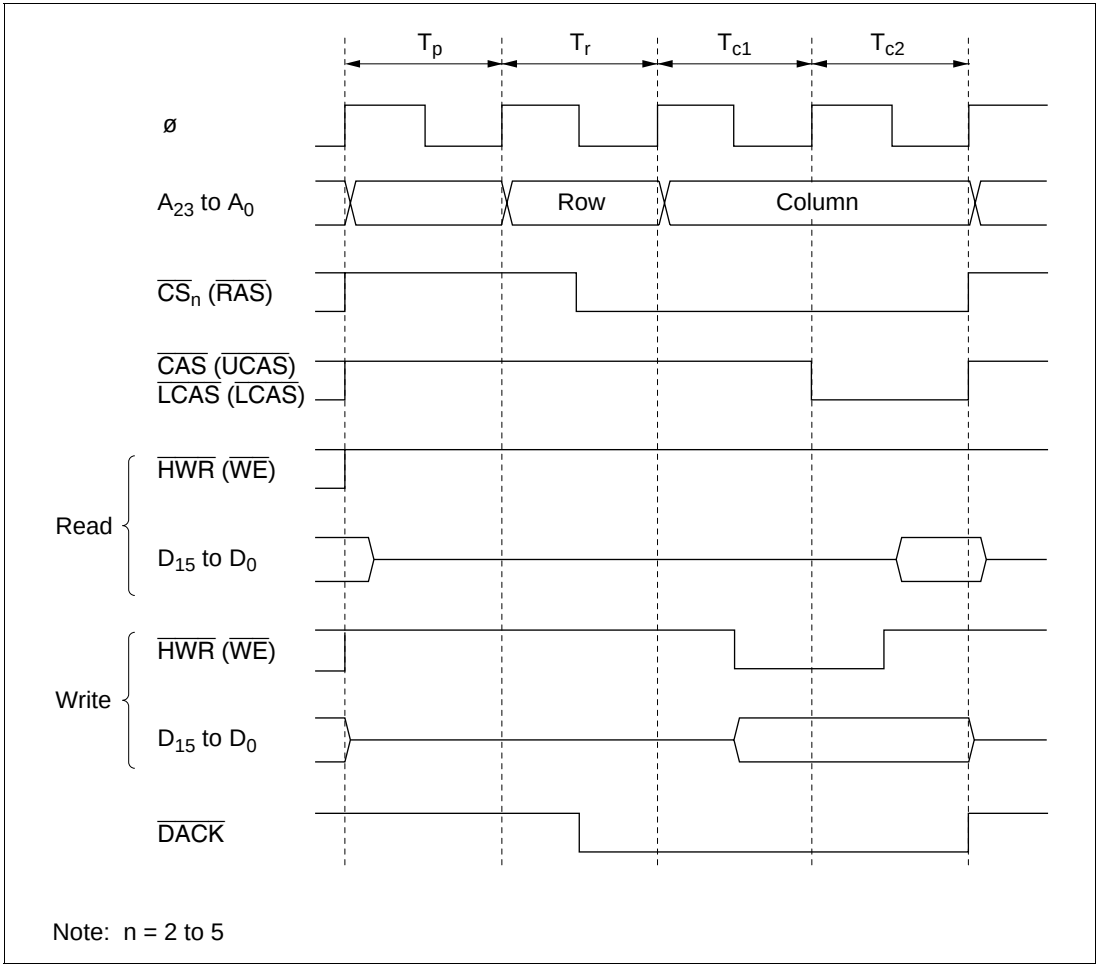


Figure 4.19 $\overline{\text{DACK}}$ Output Timing when DDS = 0 (Example of DRAM Access)

4.7 Burst ROM Interface

4.7.1 Overview

With the H8S/2339 and H8S/2338 Series, external space area 0 can be designated as burst ROM space, and burst ROM interfacing performed. The burst ROM space interface enables 16-bit ROM with burst access capability to be accessed at high speed.

Area 0 can be designated as burst ROM space by means of the BRSTRM bit in BCRH. Consecutive burst accesses of a maximum or 4 words or 8 words can be performed for CPU instruction fetches only. One or two states can be selected for burst access.

4.7.2 Basic Timing

The number of states in the initial cycle (full access) of the burst ROM interface is determined by the setting of the AST0 bit in ASTCR. When the AST0 bit is set to 1, wait state insertion is also possible. One or two states can be selected for the burst cycle, according to the setting of the BRSTS1 bit in BCRH. Wait states cannot be inserted. When area 0 is designated as burst ROM space, it functions as 16-bit access space regardless of the setting of the ABW0 bit in ABWCR.

When the BRSTS0 bit in BCRH is cleared to 0, burst access of up to 4 words is performed; when the BRSTS0 bit is set to 1, burst access of up to 8 words is performed.

The basic access timing for burst ROM space is shown in figures 4.20 (a) and (b). The timing shown in figure 4.20 (a) is for the case where the AST0 and BRSTS1 bits are both set to 1, and that in figure 4.20 (b) is for the case where both these bits are cleared to 0.

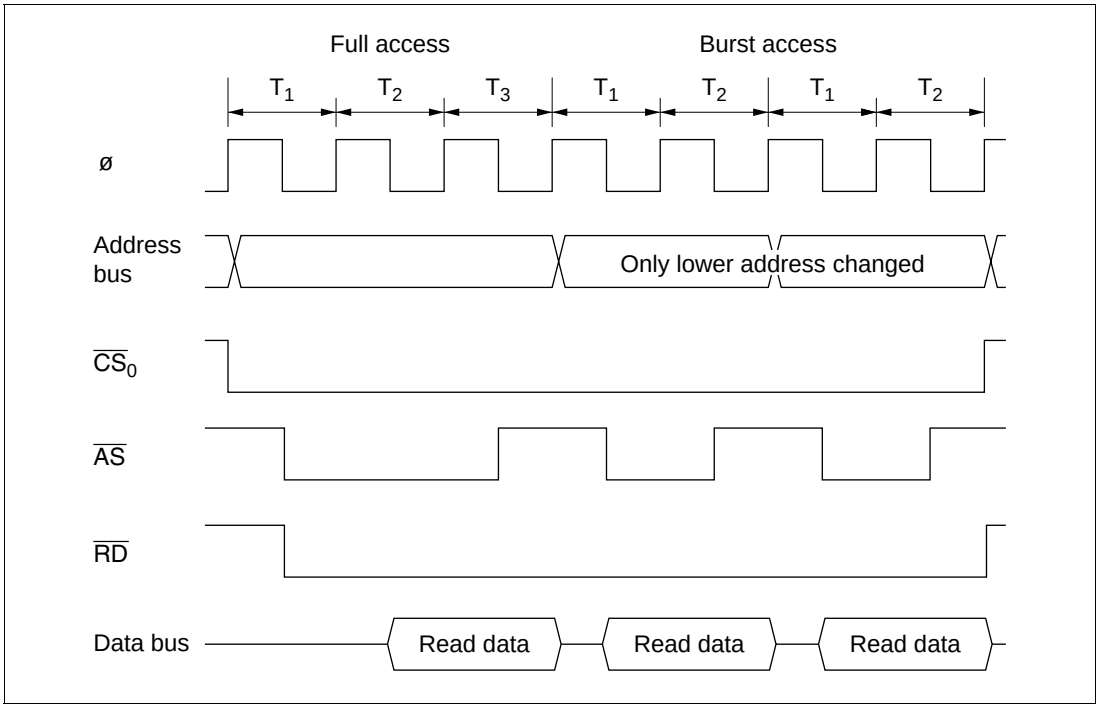


Figure 4.20 (a) Example of Burst ROM Access Timing (When AST0 = BRSTS1= 1)

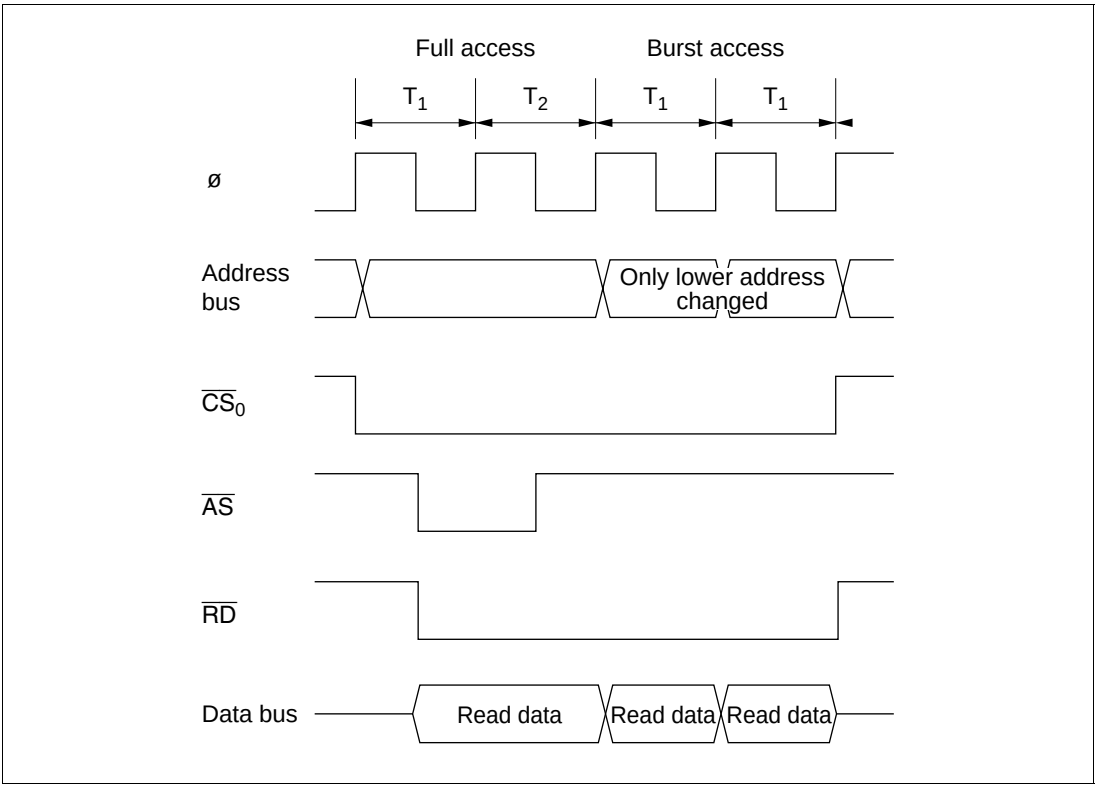


Figure 4.20 (b) Example of Burst ROM Access Timing (When AST0 = BRSTS1 = 0)

4.7.3 Wait Control

As with the basic bus interface, either program wait insertion or pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) on the burst ROM interface. See section 4.4.2, Wait Control.

Wait states cannot be inserted in a burst cycle.

4.8 Idle Cycle

4.8.1 Operation

When the H8S/2339 or H8S/2338 Series chip accesses external space, it can insert a 1-state idle cycle (T_I) between bus cycles in the following two cases: (1) when read accesses in different areas occur consecutively, and (2) when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, etc., with a long output floating time, and high-speed memory, I/O interfaces, and so on.

Consecutive Reads in Different Areas: If consecutive reads in different areas occur while the ICIS1 bit in BCRH is set to 1, an idle cycle is inserted at the start of the second read cycle. This is enabled in advanced mode.

Figure 4.21 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a read cycle for SRAM, each being located in a different area. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and that from SRAM. In (b), an idle cycle is inserted, and a data collision is prevented.

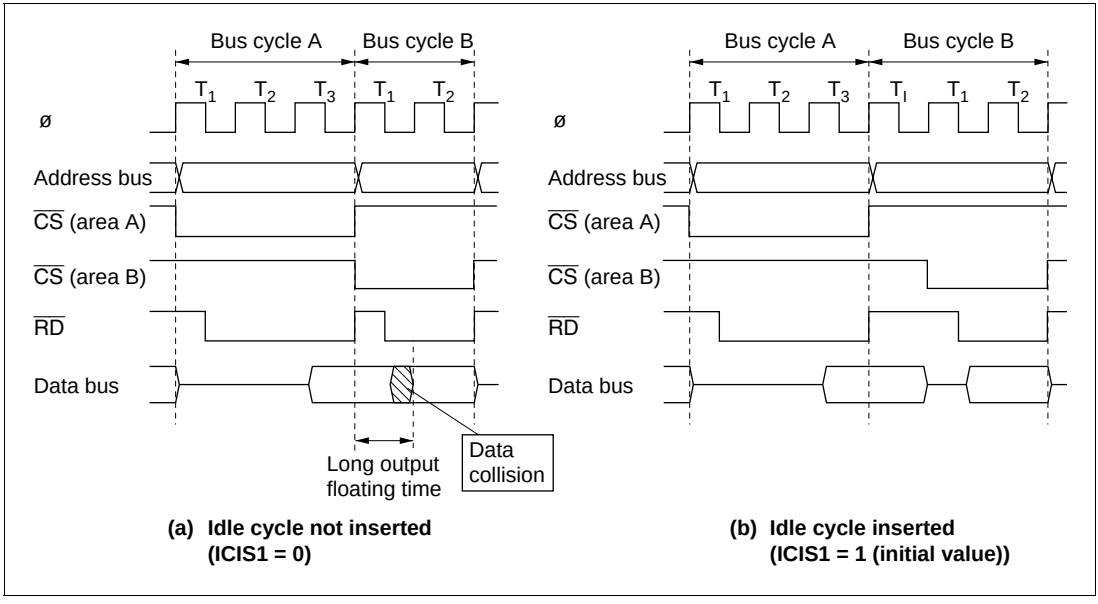


Figure 4.21 Example of Idle Cycle Operation (1)

Write after Read: If an external write occurs after an external read while the ICIS0 bit in BCRH is set to 1, an idle cycle is inserted at the start of the write cycle.

Figure 4.22 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

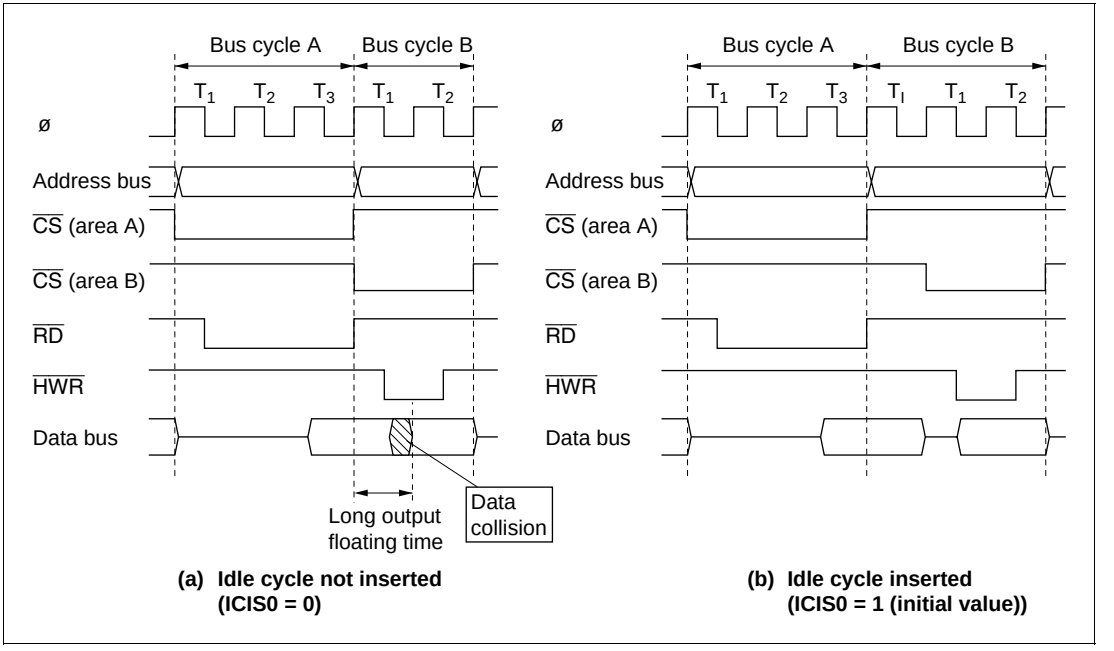


Figure 4.22 Example of Idle Cycle Operation (2)

Relationship between Chip Select ($\overline{CS}$) Signal and Read ($\overline{RD}$) Signal: Depending on the system's load conditions, the $\overline{RD}$ signal may lag behind the $\overline{CS}$ signal. An example is shown in figure 4.23.

In this case, with the setting for no idle cycle insertion (a), there may be a period of overlap between the bus cycle A $\overline{RD}$ signal and the bus cycle B $\overline{CS}$ signal.

Setting idle cycle insertion, as in (b), however, will prevent any overlap between the $\overline{RD}$ and $\overline{CS}$ signals.

In the initial state after reset release, idle cycle insertion (b) is set.

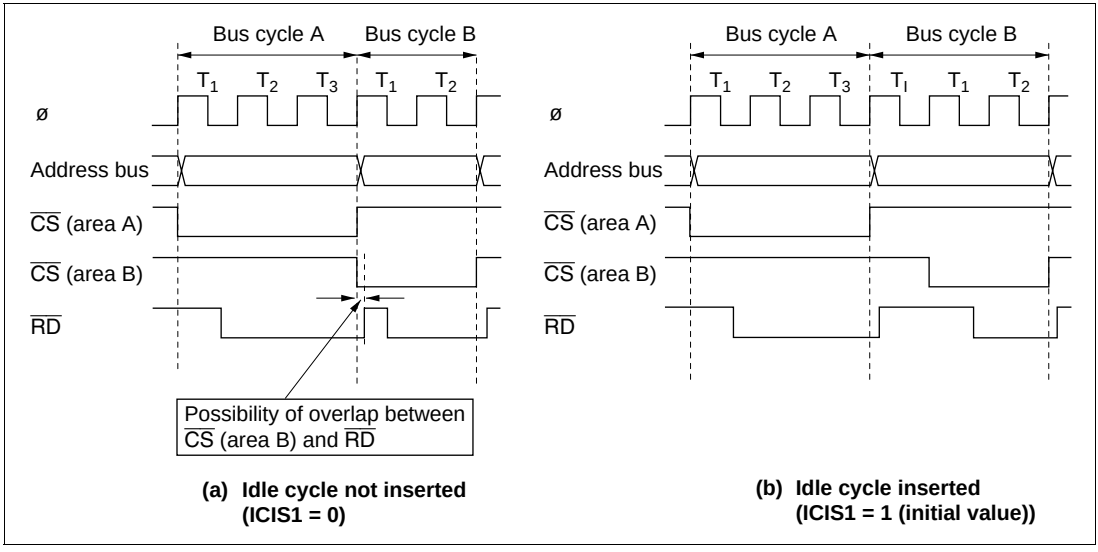


Figure 4.23 Relationship between Chip Select ($\overline{CS}$) and Read ($\overline{RD}$)

Usage Notes: When DRAM space is accessed, the ICIS0 and ICIS1 bit settings are disabled. In the case of consecutive reads in different areas, for example, if the second access is a DRAM access, only a T_p cycle is inserted, and a T_I cycle is not. The timing in this case is shown in figure 4.24. However, in burst access in RAS down mode, the settings of these bits are enabled and an idle cycle is inserted. The timing in this case is shown in figures 4.25 (a) and (b).

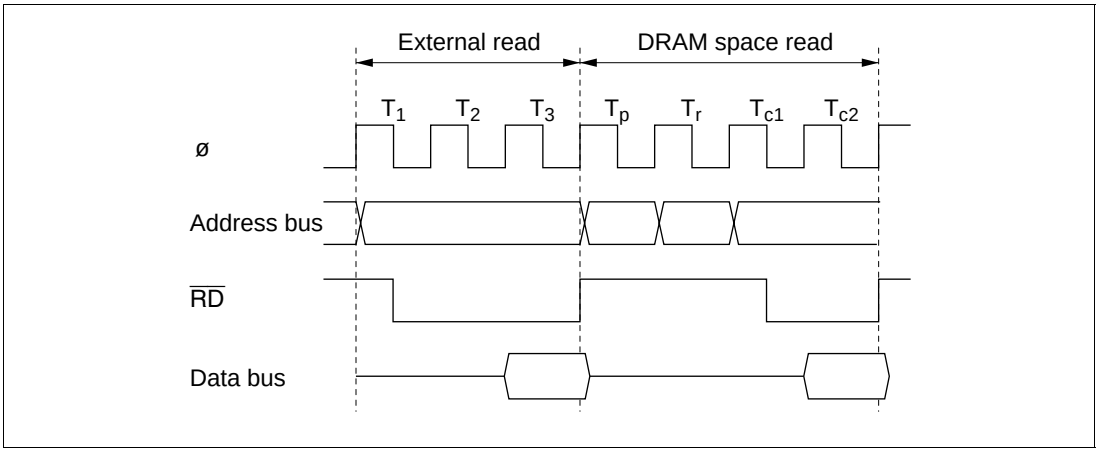


Figure 4.24 Example of DRAM Access after External Read

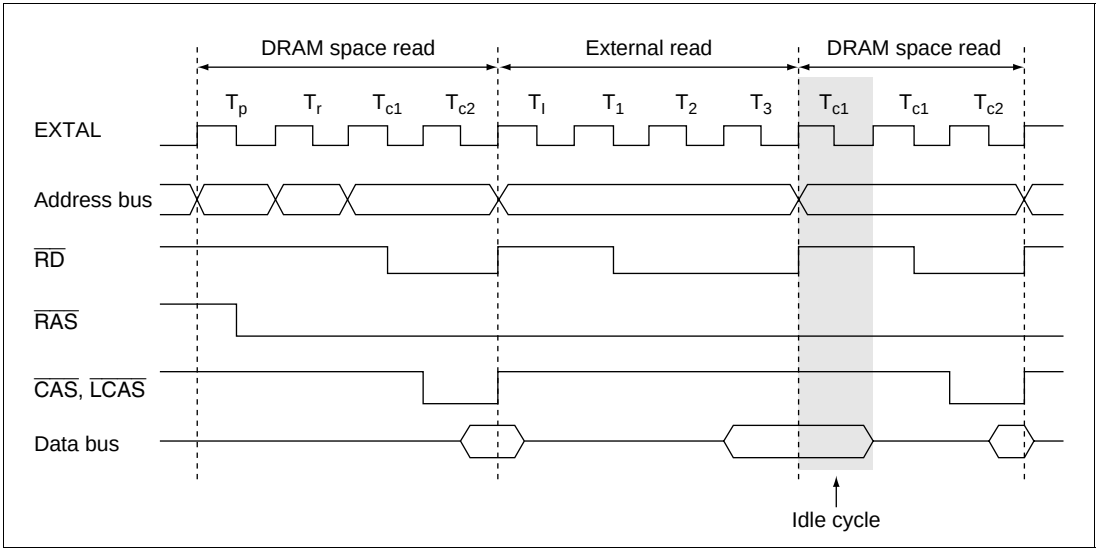


Figure 4.25 (a) Example of Idle Cycle Insertion in RAS Down Mode (ICIS1 = 1)

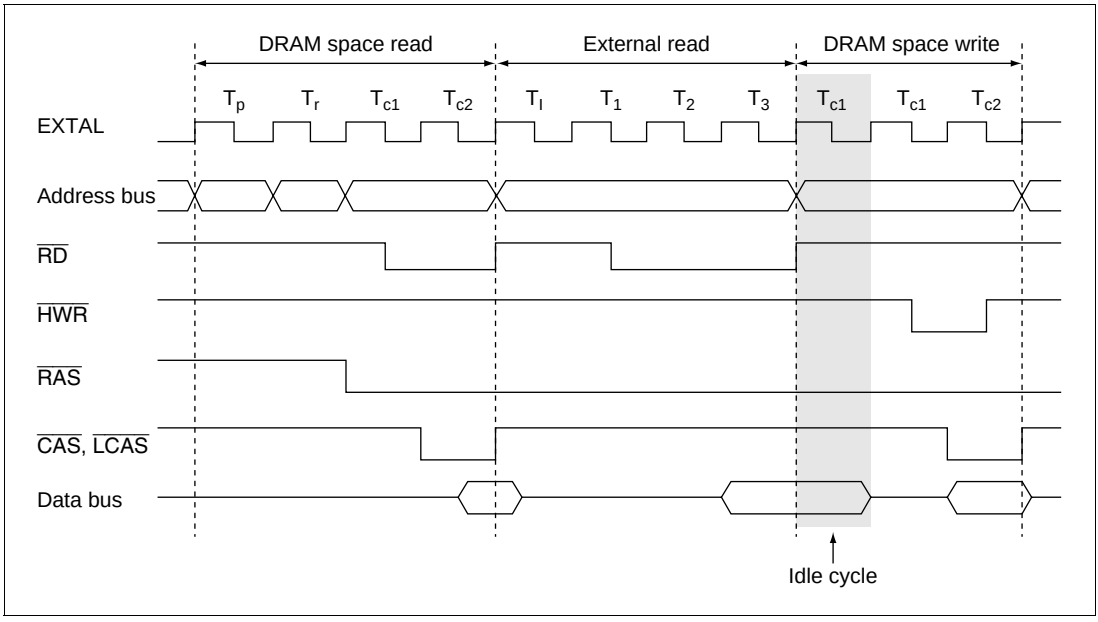


Figure 4.25 (b) Example of Idle Cycle Insertion in RAS Down Mode (ICIS0 = 1)

4.8.2 Pin States in Idle Cycle

Table 4.7 shows the pin states in an idle cycle.

Table 4.7 Pin States in Idle Cycle

Pins	Pin State
A_{23} to A_0	Contents of following bus cycle
D_{15} to D_0	High impedance
$\overline{CS}_n$*2	High*1
$\overline{CAS}$	High
$\overline{AS}$	High
$\overline{RD}$	High
$\overline{HWR}$	High
$\overline{LWR}$	High
$\overline{DACK}_m$*3	High

Notes: 1. Remains low in DRAM space RAS down mode or a refresh cycle.
2. n = 0 to 7
3. m = 0 or 1

4.9 Write Data Buffer Function

The H8S/2339 and H8S/2338 Series have a write data buffer function for the external data bus. Using the write data buffer function enables external writes and DMA single address mode transfers to be executed in parallel with internal accesses. The write data buffer function is made available by setting the WDBE bit in BCRL to 1.

Figure 4.26 shows an example of the timing when the write data buffer function is used. When this function is used, if an external write or DMA single address mode transfer continues for two states or longer, and there is an internal access next, an external write only is executed in the first state, but from the next state onward an internal access (on-chip memory or internal I/O register read/write) is executed in parallel with the external write rather than waiting until it ends.

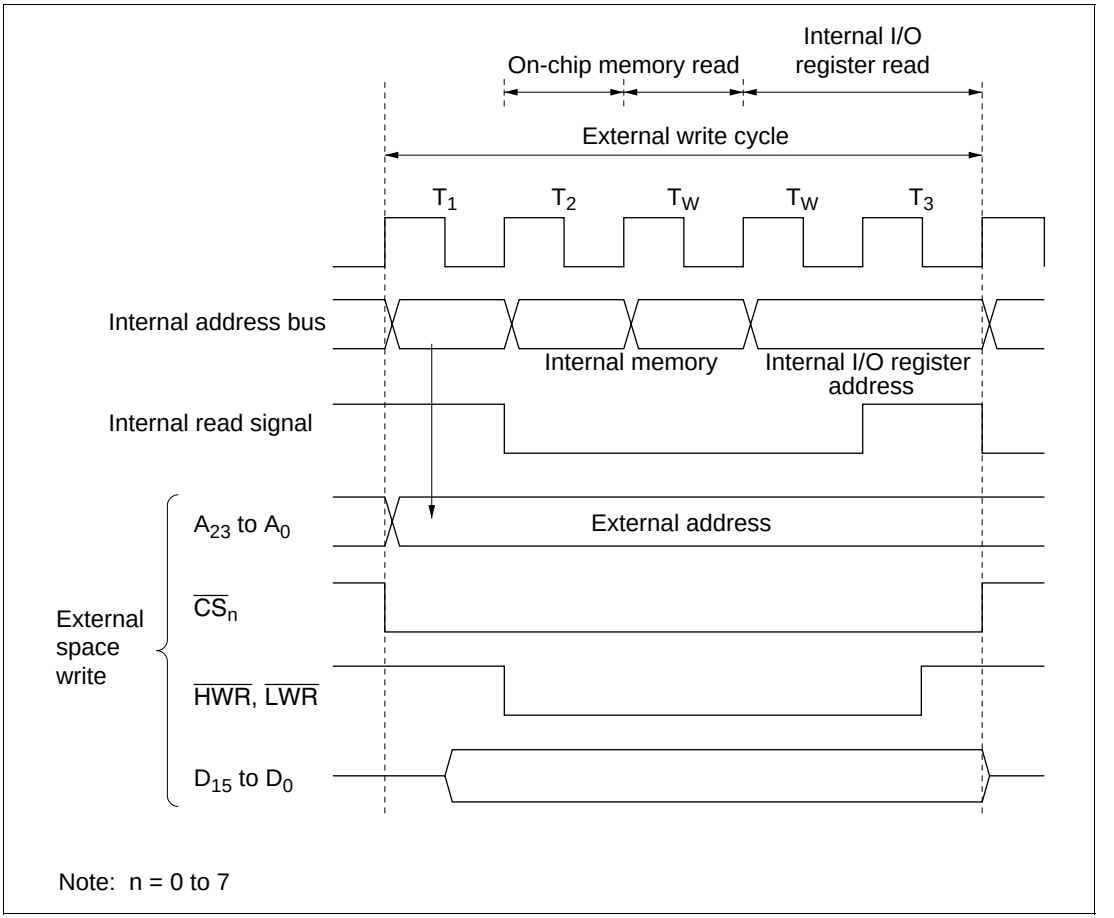


Figure 4.26 Example of Timing when Write Data Buffer Function is Used

4.10 Bus Release

4.10.1 Overview

The H8S/2339 or H8S/2338 Series chip can release the external bus in response to a bus request from an external device. In the external bus-released state, the internal bus master continues to operate as long as there is no external access.

If an internal bus master wants to make an external access in the external bus-released state, or if a refresh request is generated, it can issue a request off-chip for the bus request to be dropped.

The BREQOPS bit can be used to change the $\overline{\text{BREQO}}$ output pin from PF_2 to $P5_3$.

4.10.2 Operation

In external expanded mode, the bus can be released to an external device by setting the BRLE bit in BCRL to 1. Driving the $\overline{\text{BREQ}}$ pin low issues an external bus request to the H8S/2339 or H8S/2338 Series chip. When the $\overline{\text{BREQ}}$ pin is sampled, at the prescribed timing the $\overline{\text{BACK}}$ pin is driven low, and the address bus, data bus, and bus control signals are placed in the high-impedance state, establishing the external bus-released state.

In the external bus-released state, an internal bus master can perform accesses using the internal bus. When an internal bus master wants to make an external access, it temporarily defers activation of the bus cycle, and waits for the bus request from the external bus master to be dropped. If a refresh request is generated in the external bus-released state, refresh control is deferred until the external bus master drops the bus request.

If the BREQOE bit in BCRL is set to 1, when an internal bus master wants to make an external access in the external bus-released state, or when a refresh request is generated, the $\overline{\text{BREQO}}$ pin is driven low and a request can be made off-chip to drop the bus request.

When the $\overline{\text{BREQ}}$ pin goes high, the $\overline{\text{BACK}}$ pin is driven high at the prescribed timing and the external bus-released state is terminated.

If an external bus release request and external access occur simultaneously, the order of priority is as follows:

(High) External bus release > Internal bus master external access (Low)

If a refresh request and external bus release request occur simultaneously, the order of priority is as follows:

(High) Refresh > External bus release (Low)

As a refresh and an external access by an internal bus master can be executed simultaneously, there is no relative order of priority for these two operations.

4.10.3 Pin States in External-Bus-Released State

Table 4.8 shows pin states in the external-bus-released state.

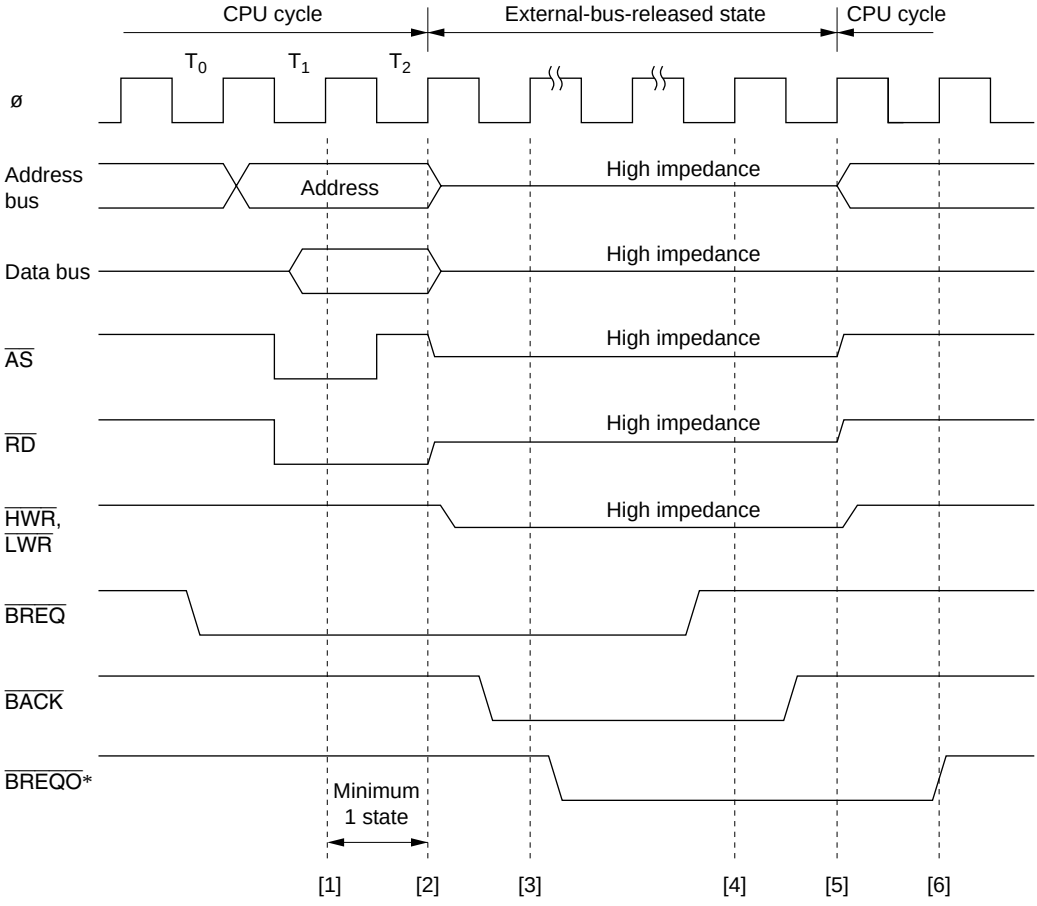
Table 4.8 Pin States in Bus-Released State

Pins	Pin State
A_{23} to A_0	High impedance
D_{15} to D_0	High impedance
$\overline{CS}_n$*1	High impedance
$\overline{CAS}$	High impedance
$\overline{AS}$	High impedance
$\overline{RD}$	High impedance
$\overline{HWR}$	High impedance
$\overline{LWR}$	High impedance
$\overline{DACK}_m$*2	High

Notes: 1. n = 0 to 7
2. m = 0 or 1

4.10.4 Transition Timing

Figure 4.27 shows the timing for transition to the bus-released state.



[1] Low level of $\overline{\text{BREQ}}$ pin is sampled at fall of T_2 state.
[2] $\overline{\text{BACK}}$ pin is driven low at end of CPU read cycle, releasing bus to external bus master.
[3] $\overline{\text{BREQ}}$ pin state is still sampled in external-bus-released state.
[4] High level of $\overline{\text{BREQ}}$ pin is sampled.
[5] $\overline{\text{BACK}}$ pin is driven high, ending bus release cycle.
[6] $\overline{\text{BREQO}}$ signal goes high 1.5 clocks after rise of $\overline{\text{BACK}}$ signal.

Note: * Output only when BREQOE = 1.

Figure 4.27 Bus-Released State Transition Timing

4.10.5 Usage Note

If MSTPCR is set to H'FFFF or H'EFFF and a transition is made to sleep mode, the external bus release function will halt. Therefore, these settings should not be used.

4.11 Bus Arbitration

4.11.1 Overview

The H8S/2339 and H8S/2338 Series have a bus arbiter that arbitrates bus master operations.

There are three bus masters, the CPU, DTC, and DMAC, which perform read/write operations when they have possession of the bus. Each bus master requests the bus by means of a bus request signal. The bus arbiter determines priorities at the prescribed timing, and permits use of the bus by means of a bus request acknowledge signal. The selected bus master then takes possession of the bus and begins its operation.

4.11.2 Operation

The bus arbiter monitors the bus masters' bus request signals, and if the bus is requested, sends a bus request acknowledge signal to the bus master making the request. If there are bus requests from more than one bus master, the bus request acknowledge signal is sent to the one with the highest priority. When a bus master receives the bus request acknowledge signal, it takes possession of the bus until that signal is canceled.

The order of priority of the bus masters is as follows:

(High) DMAC > DTC > CPU (Low)

An external access by an internal bus master, external bus release, and a refresh can be executed in parallel.

If an external bus release request, a refresh request, and an external access by an internal bus master occur simultaneously, the order of priority is as follows:

(High) Refresh > External bus release (Low)

(High) External bus release > Internal bus master external access (Low)

As a refresh and an external access by an internal bus master can be executed simultaneously, there is no relative order of priority for these two operations.

4.11.3 Bus Transfer Timing

Even if a bus request is received from a bus master with a higher priority than that of the bus master that has acquired the bus and is currently operating, the bus is not necessarily transferred immediately. There are specific times at which each bus master can relinquish the bus.

CPU: The CPU is the lowest-priority bus master, and if a bus request is received from the DTC or DMAC, the bus arbiter transfers the bus to the bus master that issued the request. The timing for transfer of the bus is as follows:

- The bus is transferred at a break between bus cycles. However, if a bus cycle is executed in discrete operations, as in the case of a longword-size access, the bus is not transferred between the component operations. For details of times when the bus is not transferred, see appendix A.5, Bus States During Instruction Execution, in the Hardware Manual.
- If the CPU is in sleep mode, it transfers the bus immediately.

DTC: The DTC sends the bus arbiter a request for the bus when an activation request is generated.

The DTC can release the bus after a vector read, a register information read (3 states), a single data transfer, or a register information write (3 states). It does not release the bus during a register information read (3 states), a single data transfer, or a register information write (3 states).

DMAC: The DMAC sends the bus arbiter a request for the bus when an activation request is generated.

In the case of an external request in short address mode or normal mode, and in cycle steal mode, the DMAC releases the bus after a single transfer.

In block transfer mode, it releases the bus after transfer of one block, and in burst mode, after completion of the transfer.

4.11.4 Note on Use of External Bus Release

External bus release can be performed on completion of an external bus cycle. The $\overline{RD}$ signal and the DRAM interface $\overline{RAS}$ and $\overline{CAS}$ signals remain low until the end of the external bus cycle. Therefore, when external bus release is performed, the $\overline{RD}$, $\overline{RAS}$, and $\overline{CAS}$ signals may change from the low level to the high-impedance state.

4.12 Bus Controller Operation in a Reset

In a reset, the chip, including the bus controller, enters the reset state immediately, and any executing bus cycle is aborted.

Section 5 I/O Ports

5.1 Overview

The H8S/2339 and H8S/2338 Series have 15 I/O ports (ports 1 to 3, $P5_0$ to $P5_3$, 6 to 9, and A to G), and two input-only ports (port 4 and $P5_4$ to $P5_7$).

Table 5.1 summarizes the port functions. The pins of each port also have other functions.

Each port includes a data direction register (DDR) that controls input/output (not provided for the input-only ports), a data register (DR) that stores output data, and a port register (PORT) used to read the pin states.

Ports A to E have a built-in MOS pull-up function, and in addition to DR and DDR, have a MOS input pull-up control register (PCR) to control the on/off state of MOS input pull-up.

Port 3 and port A include an open drain control register (ODR) that controls the on/off state of the output buffer PMOS.

Ports 1 and A to F can drive a single TTL load and 50 pF capacitive load, and ports 2, 3, 5 to 9, and G can drive a single TTL load and 30 pF capacitive load.

Ports 1, 2, 7, and 9, and pins 5_0 to 5_3 (only when used as IRQ inputs), 6_4 to 6_7, and A_4 to A_7, are Schmitt-triggered inputs.

Table 5.1 Port Functions

Port	Description	Pins	Mode 4*[1]	Mode 5*[1]	Mode 6	Mode 7
Port 1	• 8-bit I/O port • Schmitt-triggered input	$P1_7/PO_{15}/TIOCB_2/TCLKD$ $P1_6/PO_{14}/TIOCA_2$ $P1_5/PO_{13}/TIOCB_1/TCLKC$ $P14/PO12/TIOCA_1$ $P1_3/PO_{11}/TIOCD_0/TCLKB$ $P1_2/PO_{10}/TIOCC_0/TCLKA$ $P1_1/PO_9/TIOCB_0$ $P1_0/PO_8/TIOCA_0$	8-bit I/O port also functioning as TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, $TIOCA_0$, $TIOCB_0$, $TIOCC_0$, $TIOCD_0$, $TIOCA_1$, $TIOCB_1$, $TIOCA_2$, $TIOCB_2$) and PPG output pins (PO_{15} to PO_8)			
Port 2	• 8-bit I/O port • Schmitt-triggered input	$P2_7/PO_7/TIOCB_5$ $P2_6/PO_6/TIOCA_5$ $P2_5/PO_5/TIOCB_4$ $P2_4/PO_4/TIOCA_4$ $P2_3/PO_3/TIOCD_3$ $P2_2/PO_2/TIOCC_3$ $P2_1/PO_1/TIOCB_3$ $P2_0/PO_0/TIOCA_3$	8-bit I/O port also functioning as TPU I/O pins ($TIOCA_3$, $TIOCB_3$, $TIOCC_3$, $TIOCD_3$, $TIOCA_4$, $TIOCB_4$, $TIOCA_5$, $TIOCB_5$) and PPG output pins (PO_7 to PO_0)			
Port 3	• 6-bit I/O port • Open-drain output capability	$P3_5/SCK_1$ $P3_4/SCK_0$ $P3_3/RxD_1$ $P3_2/RxD_0$ $P3_1/TxD_1$ $P3_0/TxD_0$	6-bit I/O port also functioning as SCI (channel 0 and 1) I/O pins (TxD_0, RxD_0, SCK_0, TxD_1, RxD_1, SCK_1)			
Port 4	• 8-bit input port	$P4_7/AN_7/DA_1$ $P4_6/AN_6/DA_0$ $P4_5/AN_5$ $P4_4/AN_4$ $P4_3/AN_3$ $P4_2/AN_2$ $P4_1/AN_1$ $P4_0/AN_0$	8-bit input port also functioning as A/D converter analog inputs (AN_7 to AN_0) and D/A converter analog outputs (DA_1 and DA_0)			

Port	Description	Pins	Mode 4*[1]	Mode 5*[1]	Mode 6	Mode 7
Port 5	• 4-bit I/O port • 4-bit input port	$P5_7/AN_{15}/DA_3$ $P5_6/AN_{14}/DA_2$ $P5_5/AN_{13}$ $P5_4/AN_{12}$	4-bit input port also functioning as A/D converter analog inputs (AN_{15} to AN_{12}) and D/A converter analog outputs (DA_3 and DA_2)			
	• Schmitt-triggered input ($\overline{IRQ}$ input only)	$P5_3/\overline{ADTRG}/\overline{IRQ_7}/\overline{WAIT}/\overline{BREQO}$	I/O port also functioning as A/D converter input pin ($\overline{ADTRG}$), and as interrupt input pin ($\overline{IRQ_7}$) when IRQPAS = 1, $\overline{WAIT}$ input pin when WAITE =1, BREQOE =0, WAITPS = 1, DDR =0, and $\overline{BREQO}$ output pin when WAITE =0, BREQOE = 1,BREQOPS = 1			I/O port also functioning as A/D converter input pin ($\overline{ADTRG}$), and as interrupt input pin ($\overline{IRQ_7}$) when IRQPAS = 1
		$P5_2/SCK_2/\overline{IRQ_6}$ $P5_1/RxD_2/\overline{IRQ_5}$ $P5_0/TxD_2/\overline{IRQ_4}$	I/O port also functioning as SCI (channel 2) I/O pins (TxD_2, RxD_2, SCK_2), and as interrupt input pins ($\overline{IRQ_4}$ to $\overline{IRQ_6}$) when IRQPAS = 1			
Port 6	• 8-bit I/O port • Schmitt-triggered input ($P6_4$ to $P6_7$)	$P6_7/\overline{CS_7}$ $P6_6/\overline{CS_6}$ $P6_5/\overline{IRQ_1}$ $P6_4/\overline{IRQ_0}$ $P6_3$ $P6_2$ $P6_1/\overline{CS_5}$ $P6_0/\overline{CS_4}$	8-bit I/O port also functioning as bus control output pins ($\overline{CS_4}$ to $\overline{CS_7}$), and interrupt input pins ($\overline{IRQ_0}$ and $\overline{IRQ_1}$)			8-bit I/O port also functioning as interrupt input pins ($\overline{IRQ_0}$ and $\overline{IRQ_1}$)
Port 7	• 6-bit I/O port • Schmitt-triggered input	$P7_5/TMO_1$ $P7_4/TMO_0$ $P7_3/TMCI_1$ $P7_2/TMCI_0$ $P7_1/TMRI_1$ $P7_0/TMRI_0$	6-bit I/O port also functioning as 8-bit timer (channels 0 and 1) I/O pins ($TMRI_0$, $TMCI_0$, TMO_0, $TMRI_1$, $TMCI_1$, TMO_1)			
Port 8	• 7-bit I/O port	$P8_6/\overline{WAIT}$ $P8_5/\overline{DACK_1}$ $P8_4/\overline{DACK_0}$ $P8_3/\overline{TEND_1}$ $P8_2/\overline{TEND_0}$ $P8_1/\overline{DREQ_1}$ $P8_0/\overline{DREQ_0}$	7-bit I/O port also functioning as DMA controller I/O pins ($\overline{DREQ_0}$, $\overline{TEND_0}$, $\overline{DACK_0}$, $\overline{DREQ_1}$, $\overline{TEND_1}$, $\overline{DACK_1}$) and $\overline{WAIT}$ input when WAITPS = 0, DDR =0			

Port	Description	Pins	Mode 4*[1]	Mode 5*[1]	Mode 6	Mode 7
Port 9	• 6-bit I/O port • Schmitt-triggered input	$P9_7/\overline{IRQ_7}$ $P9_6/\overline{IRQ_6}$ $P9_5/\overline{IRQ_5}$ $P9_4/\overline{IRQ_4}$ $P9_3/\overline{IRQ_3}$ $P9_2/\overline{IRQ_2}$	6-bit I/O port also functioning as interrupt input pins ($\overline{IRQ_7}$ to $\overline{IRQ_2}$)			
Port A	• 8-bit I/O port • Built-in MOS input pull-up • Open-drain output capability • Schmitt-triggered input (PA_4 to PA_7)	PA_7/A_{23} PA_6/A_{22} PA_5/A_{21}	When DDR = 0 (after reset): input port When DDR = 1 and A23E to A21E = 1: address output When DDR = 1 and A23E to A21E = 0: DR value output		When DDR = 0 (after reset): input port When DDR = 1 and A23E to A20E = 1: address output	I/O ports
		PA_4/A_{20}	Address output also functioning as DR value output		When DDR = 1 and A23E to A20E = 0: DR value output	
		PA_3/A_{19} to PA_0/A_{16}	Address output		When DDR = 0 (after reset): input ports When DDR = 1: address output	I/O ports
Port B	• 8-bit I/O port • Built-in MOS input pull-up	PB_7/A_{15} to PB_0/A_8	Address output		When DDR = 0 (after reset): input port When DDR = 1: address output	I/O port
Port C	• 8-bit I/O port • Built-in MOS input pull-up	PC_7/A_7 to PC_0/A_0	Address output		When DDR = 0 (after reset): input port When DDR = 1: address output	I/O port
Port D	• 8-bit I/O port • Built-in MOS input pull-up	PD_7/D_{15} to PD_0/D_8	Data bus input/output			I/O port

Port	Description	Pins	Mode 4*[1]	Mode 5*[1]	Mode 6	Mode 7
Port E	• 8-bit I/O port • Built-in MOS input pull-up	PE_7/D_7 to PE_0/D_0	In 8-bit bus mode: I/O port In 16-bit bus mode: data bus input/output			I/O port
Port F	• 8-bit I/O port	$PF_7/ø$	When DDR = 0: input port When DDR = 1 (after reset): ø output			When DDR = 0 (after reset): input port When DDR = 1: ø output
		$PF_6/\overline{AS}$	When ASOD = 1: I/O port When ASOD = 0: $\overline{AS}$ output			I/O port
		$PF_5/\overline{RD}$ $PF_4/\overline{HWR}$	$\overline{RD}$, $\overline{HWR}$ output			
		$PF_3/\overline{LWR}$	When LWROD = 1: I/O port When LWROD = 0: $\overline{LWR}$ output			
		$PF_2/\overline{LCAS}/\overline{BREQO}$	When BREQOE = 0 (after reset): I/O port When BREQOE = 1 and BREQOPS = 0: $\overline{BREQO}$ output When RMTS2 to RMTS0= B'001 to B'011, and 16-bit access space is set: $\overline{LCAS}$ output			
		$PF_1/\overline{BACK}$ $PF_0/\overline{BREQ}$	When BRLE = 0 (after reset): I/O port When BRLE = 1: $\overline{BREQ}$ input, $\overline{BACK}$ output			
Port G	• 5-bit I/O port	$PG_4/\overline{CS_0}$	When DDR = 0*[2]: input port When DDR = 1*[3]: $\overline{CS_0}$ output			I/O port
		$PG_3/\overline{CS_1}$	When DDR = 0 (after reset): input port When CS167E = 0 and DDR = 1: output port When CS167E = 1 and DDR = 1: $\overline{CS_1}$ output			
		$PG_2/\overline{CS_2}$	When DDR = 0 (after reset): input port When CS25E = 0 and DDR = 1: output port When CS25E = 1 and DDR = 1: $\overline{CS_2}$ output			
		$PG_1/\overline{CS_3}$	When DDR = 0 (after reset): input port When CS25E = 0 and DDR = 1: output port When CS25E = 1 and DDR = 1: $\overline{CS_3}$ output			
		$PG_0/\overline{CAS}$	DRAM space set: $\overline{CAS}$ output Otherwise (after reset): I/O port			

Notes: 1. Only modes 4 and 5 are provided in the ROMless version.
2. After a reset in mode 6
3. After a reset in mode 4 or 5

5.2 Port 1

5.2.1 Overview

Port 1 is an 8-bit I/O port. Port 1 pins also function as PPG output pins (PO_{15} to PO_8) and TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, $TIOCA_0$, $TIOCB_0$, $TIOCC_0$, $TIOCD_0$, $TIOCA_1$, $TIOCB_1$, $TIOCA_2$, and $TIOCB_2$) Port 1 pin functions are the same in all operating modes. Port 1 uses Schmitt-triggered input.

Figure 5.1 shows the port 1 pin configuration.

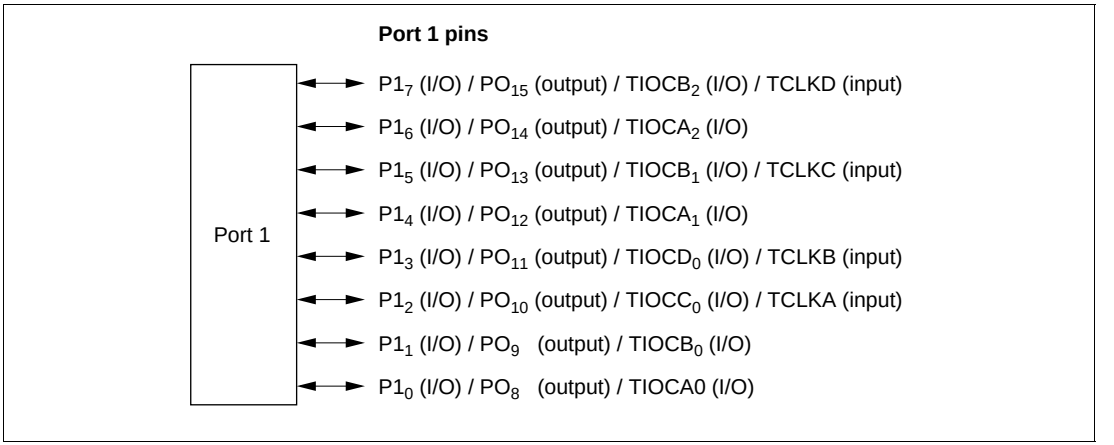


Figure 5.1 Port 1 Pin Functions

5.2.2 Register Configuration

Table 5.2 shows the port 1 register configuration.

Table 5.2 Port 1 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 1 data direction register	P1DDR	W	H'00	H'FEB0
Port 1 data register	P1DR	R/W	H'00	H'FF60
Port 1 register	PORT1	R	Undefined	H'FF50

Note: * Lower 16 bits of the address.

Port 1 Data Direction Register (P1DDR)

Bit	:	7	6	5	4	3	2	1	0
		P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

P1DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 1. P1DDR cannot be read; if it is, an undefined value will be read.

Setting a P1DDR bit to 1 makes the corresponding port 1 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P1DDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 1 Data Register (P1DR)

Bit	:	7	6	5	4	3	2	1	0
		P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1DR is an 8-bit readable/writable register that stores output data for the port 1 pins (P17 to P10).

P1DR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 1 Register (PORT1)

Bit	:	7	6	5	4	3	2	1	0
		P17	P16	P15	P14	P13	P12	P11	P10
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins $P1_7$ to $P1_0$.

PORT1 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 1 pins ($P1_7$ to $P1_0$) must always be performed on P1DR.

If a port 1 read is performed while P1DDR bits are set to 1, the P1DR values are read. If a port 1 read is performed while P1DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT1 contents are determined by the pin states, as P1DDR and P1DR are initialized. PORT1 retains its prior state in software standby mode.

5.2.3 Pin Functions

Port 1 pins also function as PPG output pins (PO_{15} to PO_8) and TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, $TIOCA_0$, $TIOCB_0$, $TIOCC_0$, $TIOCD_0$, $TIOCA_1$, $TIOCB_1$, $TIOCA_2$, and $TIOCB_2$) Port 1 pin functions are shown in table 5.3.

Table 5.3 Port 1 Pin Functions

Pin | **Selection Method and Pin Functions**

$P1_7/PO_{15}/TIOCB_2/TCLKD$

The pin function is switched as shown below according to the combination of the TPU channel 2 setting (by bits MD3 to MD0 in TMDR2, bits IOB3 to IOB0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), bits TPSC2 to TPSC0 in TCR0 and TCR5, bit NDER15 in NDERH, and bit P17DDR.

TPU Channel 2 Setting	Table Below (1)	Table Below (2)		
P17DDR	—	0	1	1
NDER15	—	—	0	1
Pin function	$TIOCB_2$ output	$P1_7$ input	$P1_7$ output	PO_{15} output
		$TIOCB_2$ input *1		
	TCLKD input *2			

Notes: 1. $TIOCB_2$ input when MD3 to MD0 = B'0000 or B'01xx, and IOB3 = 1.
2. TCLKD input when the setting for either TCR0 or TCR5 is: TPSC2 to TPSC0 = B'111.
TCLKD input when channels 2 and 4 are set to phase counting mode.

TPU Channel 2 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
$P1_6/PO_{14}/TIOCA_2$	The pin function is switched as shown below according to the combination of the TPU channel 2 setting (by bits MD3 to MD0 in TMDR2, bits IOA3 to IOA0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), bit NDER14 in NDERH, and bit P16DDR.

TPU Channel 2 Setting	Table Below (1)	Table Below (2)		
P16DDR	—	0	1	1
NDER14	—	—	0	1
Pin function	$TIOCA_2$ output	$P1_6$ input	$P1_6$ output	PO_{14} output
		$TIOCA_2$ input *1		

TPU Channel 2 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0011	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output *2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_2$ input when MD3 to MD0 = B'0000 or B'01xx, and IOA3 = 1.
2. $TIOCB_2$ output is disabled.

Pin	Selection Method and Pin Functions
$P1_5/PO_{13}/TIOCB_1/TCLKC$	The pin function is switched as shown below according to the combination of the TPU channel 1 setting (by bits MD3 to MD0 in TMDR1, bits IOB3 to IOB0 in TIOR1, and bits CCLR1 and CCLR0 in TCR1), bits TPSC2 to TPSC0 in TCR0, TCR2, TCR4, and TCR5, bit NDER13 in NDERH, and bit P15DDR.

TPU Channel 1 Setting	Table Below (1)	Table Below (2)		
P15DDR	—	0	1	1
NDER13	—	—	0	1
Pin function	$TIOCB_1$ output	$P1_5$ input	$P1_5$ output	PO_{13} output
		$TIOCB_1$ input *1		
	TCLKC input *2			

Notes: 1. $TIOCB_1$ input when MD3 to MD0 = B'0000 or B'01xx, and IOB3 to IOB0 = B'10xx.

2. TCLKC input when the setting for either TCR0 or TCR2 is: TPSC2 to TPSC0 = B'110; or when the setting for either TCR4 or TCR5 is TPSC2 to TPSC0 = B'101.
   TCLKC input when channels 2 and 4 are set to phase counting mode.

TPU Channel 1 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
$P1_4/PO_{12}/TIOCA_1$	The pin function is switched as shown below according to the combination of the TPU channel 1 setting (by bits MD3 to MD0 in TMDR1, bits IOA3 to IOA0 in TIOR1, and bits CCLR1 and CCLR0 in TCR1), bit NDER12 in NDERH, and bit P14DDR.

TPU Channel 1 Setting	Table Below (1)	Table Below (2)		
P14DDR	—	0	1	1
NDER12	—	—	0	1
Pin function	$TIOCA_1$ output	$P1_4$ input	$P1_4$ output	PO_{12} output
		$TIOCA_1$ input *1		

TPU Channel 1 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_1$ input when MD3 to MD0 = B'0000 or B'01xx, and IOA3 to IOA0 = B'10xx.

2. $TIOCB_1$ output is disabled.

Pin	Selection Method and Pin Functions

$P1_3/PO_{11}/TIOCD_0/TCLKB$

The pin function is switched as shown below according to the combination of the TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOD3 to IOD0 in TIOR0L, and bits CCLR2 to CCLR0 in TCR0), bits TPSC2 to TPSC0 in TCR0 to TCR2, bit NDER11 in NDERH, and bit P13DDR.

TPU Channel 0 Setting	Table Below (1)	Table Below (2)		
P13DDR	—	0	1	1
NDER11	—	—	0	1
Pin function	$TIOCD_0$ output	$P1_3$ input	$P1_3$ output	PO_{11} output
		$TIOCD_0$ input *1		
	TCLKB input *2			

Notes: 1. $TIOCD_0$ input when MD3 to MD0 = B'0000, and IOD3 to IOD0 = B'10xx.

2. TCLKB input when the setting for TCR0 to TCR2 is: TPSC2 to TPSC0 = B'101.
   TCLKB input when channels 1 and 5 are set to phase counting mode.

TPU Channel 0 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions

$P1_2/PO_{10}/TIOCC_0/TCLKA$

The pin function is switched as shown below according to the combination of the TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOC3 to IOC0 in TIOR0L, and bits CCLR2 to CCLR0 in TCR0), bits TPSC2 to TPSC0 in TCR0 to TCR5, bit NDER10 in NDERH, and bit P12DDR.

TPU Channel 0 Setting	Table Below (1)	Table Below (2)		
P12DDR	—	0	1	1
NDER10	—	—	0	1
Pin function	$TIOCC_0$ output	$P1_2$ input	$P1_2$ output	PO_{10} output
		$TIOCC_0$ input *1		
	TCLKA input *2			

TPU Channel 0 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOC3 to IOC0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'101	B'101
Output function	—	Output compare output	—	PWM mode 1 output*3	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCC_0$ input when MD3 to MD0 = B'0000, and IOC3 to IOC0 = B'10xx.

2. TCLKA input when the setting for TCR0 to TCR5 is: TPSC2 to TPSC0 = B'100.
   TCLKA input when channels 1 and 5 are set to phase counting mode.

3. $TIOCD_0$ output is disabled.
   When BFA = 1 or BFB = 1 in TMDR0, output is disabled and setting (2) applies.

Pin	Selection Method and Pin Functions
$P1_1/PO_9/TIOCB_0$	The pin function is switched as shown below according to the combination of the TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOB3 to IOB0 in TIOR0H, and bits CCLR2 to CCLR0 in TCR0), bit NDER9 in NDERH, and bit P11DDR.

TPU Channel 0 Setting	Table Below (1)	Table Below (2)		
P11DDR	—	0	1	1
NDER9	—	—	0	1
Pin function	$TIOCB_0$ output	$P1_1$ input	$P1_1$ output	PO_9 output
		$TIOCB_0$ input *		

Note: * $TIOCB_0$ input when MD3 to MD0 = B'0000, and IOB3 to IOB0 = B'10xx.

TPU Channel 0 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions

$P1_0/PO_8/TIOCA_0$

The pin function is switched as shown below according to the combination of the TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOA3 to IOA0 in TIOR0H, and bits CCLR2 to CCLR0 in TCR0), bit NDER8 in NDERH, and bit P10DDR.

TPU Channel 0 Setting	Table Below (1)	Table Below (2)		
P10DDR	—	0	1	1
NDER8	—	—	0	1
Pin function	$TIOCA_0$ output	$P1_0$ input	$P1_0$ output	PO_8 output
		$TIOCA_0$ input *1		

TPU Channel 0 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_0$ input when MD3 to MD0 = B'0000, and IOA3 to IOA0 = B'10xx.

2. $TIOCB_0$ output is disabled.

5.3 Port 2

5.3.1 Overview

Port 2 is an 8-bit I/O port. Port 2 pins also function as PPG output pins (PO_7 to PO_0) and TPU I/O pins ($TIOCA_3$, $TIOCB_3$, $TIOCC_3$, $TIOCD_3$, $TIOCA_4$, $TIOCB_4$, $TIOCA_5$, and $TIOCB_5$). Port 2 pin functions are the same in all operating modes. Port 2 uses Schmitt-triggered input.

Figure 5.2 shows the port 2 pin configuration.

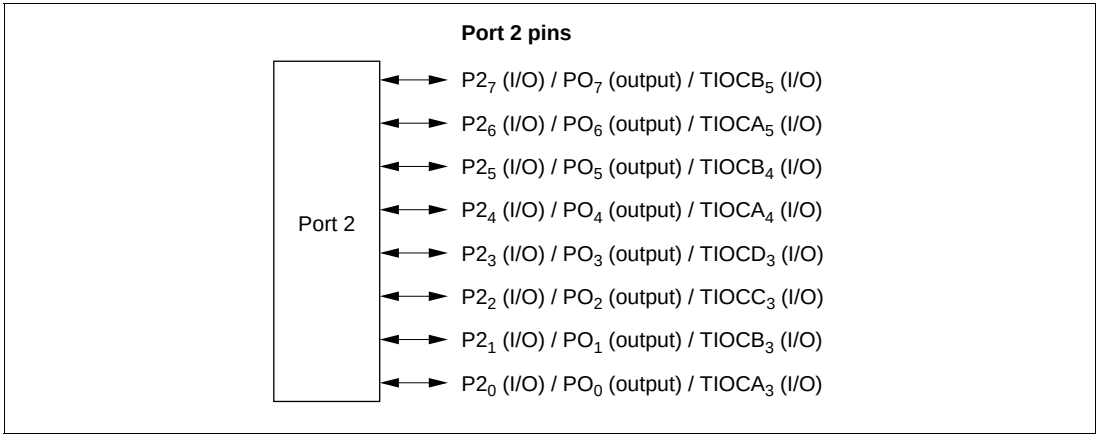


Figure 5.2 Port 2 Pin Functions

5.3.2 Register Configuration

Table 5.4 shows the port 2 register configuration.

Table 5.4 Port 2 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 2 data direction register	P2DDR	W	H'00	H'FEB1
Port 2 data register	P2DR	R/W	H'00	H'FF61
Port 2 register	PORT2	R	Undefined	H'FF51

Note: * Lower 16 bits of the address.

Port 2 Data Direction Register (P2DDR)

Bit	:	7	6	5	4	3	2	1	0
		P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

P2DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 2. P2DDR cannot be read; if it is, an undefined value will be read.

Setting a P2DDR bit to 1 makes the corresponding port 2 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P2DDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 2 Data Register (P2DR)

Bit	:	7	6	5	4	3	2	1	0
		P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2DR is an 8-bit readable/writable register that stores output data for the port 2 pins (P27 to P20).

P2DR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 2 Register (PORT2)

Bit	:	7	6	5	4	3	2	1	0
		P27	P26	P25	P24	P23	P22	P21	P20
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins $P2_7$ to $P2_0$.

PORT2 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 2 pins ($P2_7$ to $P2_0$) must always be performed on P2DR.

If a port 2 read is performed while P2DDR bits are set to 1, the P2DR values are read. If a port 2 read is performed while P2DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT2 contents are determined by the pin states, as P2DDR and P2DR are initialized. PORT2 retains its prior state in software standby mode.

5.3.3 Pin Functions

Port 2 pins also function as PPG output pins (PO_7 to PO_0) and TPU I/O pins ($TIOCA_3$, $TIOCB_3$, $TIOCC_3$, $TIOCD_3$, $TIOCA_4$, $TIOCB_4$, $TIOCA_5$, and $TIOCB_5$). Port 2 pin functions are shown in table 5.5.

Table 5.5 Port 2 Pin Functions

Pin | **Selection Method and Pin Functions**

$P2_7/PO_7/TIOCB_5$

The pin function is switched as shown below according to the combination of the TPU channel 5 setting (by bits MD3 to MD0 in TMDR5, bits IOB3 to IOB0 in TIOR5, and bits CCLR1 and CCLR0 in TCR5), bit NDER7 in NDERL, and bit P27DDR.

TPU Channel 5 Setting	Table Below (1)	Table Below (2)		
P27DDR	—	0	1	1
NDER7	—	—	0	1
Pin function	$TIOCB_5$ output	$P2_7$ input	$P2_7$ output	PO_7 output
		$TIOCB_5$ input *		

Note: * $TIOCB_5$ input when MD3 to MD0 = B'0000 or B'01xx, and IOB3 = 1.

TPU Channel 5 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
$P2_6/PO_6/TIOCA_5$	The pin function is switched as shown below according to the combination of the TPU channel 5 setting (by bits MD3 to MD0 in TMDR5, bits IOA3 to IOA0 in TIOR5, and bits CCLR1 and CCLR0 in TCR5), bit NDER6 in NDERL, and bit P26DDR.

TPU Channel 5 Setting	Table Below (1)	Table Below (2)		
P26DDR	—	0	1	1
NDER6	—	—	0	1
Pin function	$TIOCA_5$ output	$P2_6$ input	$P2_6$ output	PO_6 output
		$TIOCA_5$ input *1		

TPU Channel 5 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_5$ input when MD3 to MD0 = B'0000 or B'01xx, and IOA3 = 1.
2. $TIOCB_5$ output is disabled.

Pin	Selection Method and Pin Functions

$P2_5/PO_5/TIOCB_4$

The pin function is switched as shown below according to the combination of the TPU channel 4 setting (by bits MD3 to MD0 in TMDR4, bits IOB3 to IOB0 in TIOR4, and bits CCLR1 and CCLR0 in TCR4), bit NDER5 in NDERL, and bit P25DDR.

TPU Channel 4 Setting	Table Below (1)	Table Below (2)		
P25DDR	—	0	1	1
NDER5	—	—	0	1
Pin function	$TIOCB_4$ output	$P2_5$ input	$P2_5$ output	PO_5 output
		$TIOCB_4$ input *		

Note: * $TIOCB_4$ input when MD3 to MD0 = B'0000 or B'01xx, and IOB3 to IOB0 = B'10xx.

TPU Channel 4 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
$P2_4/PO_4/TIOCA_4$	The pin function is switched as shown below according to the combination of the TPU channel 4 setting (by bits MD3 to MD0 in TMDR4, bits IOA3 to IOA0 in TIOR4, and bits CCLR1 and CCLR0 in TCR4), bit NDER4 in NDERL, and bit P24DDR.

TPU Channel 4 Setting	Table Below (1)	Table Below (2)		
P24DDR	—	0	1	1
NDER4	—	—	0	1
Pin function	$TIOCA_4$ output	$P2_4$ input	$P2_4$ output	PO_4 output
		$TIOCA_4$ input *1		

TPU Channel 4 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_4$ input when MD3 to MD0 = B'0000 or B'01xx, and IOA3 to IOA0 = B'10xx.

2. $TIOCB_4$ output is disabled.

Pin	Selection Method and Pin Functions

$P2_3/PO_3/TIOCD_3$

The pin function is switched as shown below according to the combination of the TPU channel 3 setting (by bits MD3 to MD0 in TMDR3, bits IOD3 to IOD0 in TIOR3L, and bits CCLR2 to CCLR0 in TCR3), bit NDER3 in NDERL, and bit P23DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)		
P23DDR	—	0	1	1
NDER3	—	—	0	1
Pin function	$TIOCD_3$ output	$P2_3$ input	$P2_3$ output	PO_3 output
		$TIOCD_3$ input *		

Note: * $TIOCD_3$ input when MD3 to MD0 = B'0000, and IOD3 to IOD0 = B'10xx.

TPU Channel 3 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions

$P2_2/PO_2/TIOCC_3$

The pin function is switched as shown below according to the combination of the TPU channel 3 setting (by bits MD3 to MD0 in TMDR3, bits IOC3 to IOC0 in TIOR3L, and bits CCLR2 to CCLR0 in TCR3), bit NDER2 in NDERL, and bit P22DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)		
P22DDR	—	0	1	1
NDER2	—	—	0	1
Pin function	$TIOCC_3$ output	$P2_2$ input	$P2_2$ output	PO_2 output
		$TIOCC_3$ input *1		

TPU Channel 3 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOC3 to IOC0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'101	B'101
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCC_3$ input when MD3 to MD0 = B'0000, and IOC3 to IOC0 = B'10xx.

2. $TIOCD_3$ output is disabled.
When BFA = 1 or BFB = 1 in TMDR3, output is disabled and setting (2) applies.

Pin	Selection Method and Pin Functions

$P2_1/PO_1/TIOCB_3$

The pin function is switched as shown below according to the combination of the TPU channel 3 setting (by bits MD3 to MD0 in TMDR3, bits IOB3 to IOB0 in TIOR3H, and bits CCLR2 to CCLR0 in TCR3), bit NDER1 in NDERL, and bit P21DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)		
P21DDR	—	0	1	1
NDER1	—	—	0	1
Pin function	$TIOCB_3$ output	$P2_1$ input	$P2_1$ output	PO_1 output
		$TIOCB_3$ input *		

Note: * $TIOCB_3$ input when MD3 to MD0 = B'0000, and IOB3 to IOB0 = B'10xx.

TPU Channel 3 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions

$P2_0/PO_0/TIOCA_3$

The pin function is switched as shown below according to the combination of the TPU channel 3 setting (by bits MD3 to MD0 in TMDR3, bits IOA3 to IOA0 in TIOR3H, and bits CCLR2 to CCLR0 in TCR3), bit NDER0 in NDERL, and bit P20DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)		
P20DDR	—	0	1	1
NDER0	—	—	0	1
Pin function	$TIOCA_3$ output	$P2_0$ input	$P2_0$ output	PO_0 output
		$TIOCA_3$ input *1		

TPU Channel 3 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_3$ input when MD3 to MD0 = B'0000, and IOA3 to IOA0 = B'10xx.

2. $TIOCB_3$ output is disabled.

5.4 Port 3

5.4.1 Overview

Port 3 is a 6-bit I/O port. Port 3 pins also function as SCI I/O pins (TxD_0, RxD_0, SCK_0, TxD_1, RxD_1, and SCK_1). Port 3 pin functions are the same in all operating modes.

Figure 5.3 shows the port 3 pin configuration.

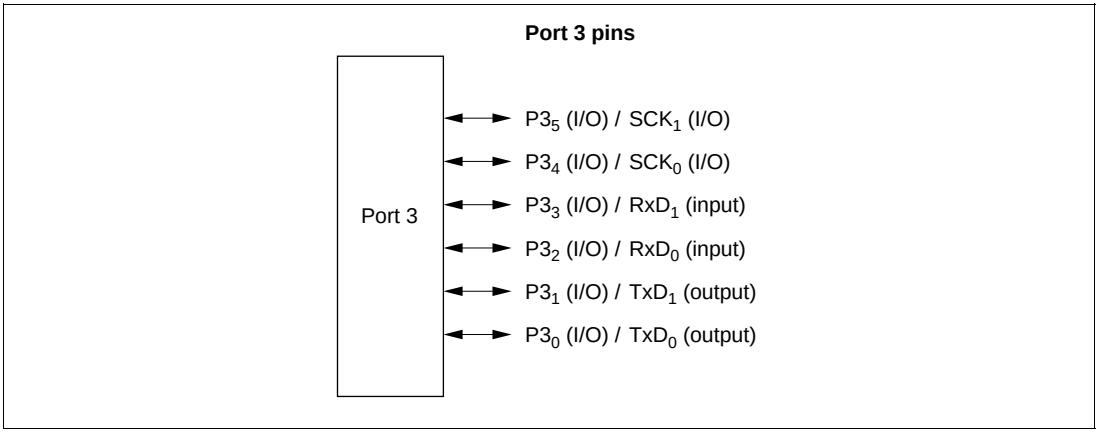


Figure 5.3 Port 3 Pin Functions

5.4.2 Register Configuration

Table 5.6 shows the port 3 register configuration.

Table 5.6 Port 3 Registers

Name	Abbreviation	R/W	Initial Value*2	Address*1
Port 3 data direction register	P3DDR	W	H'00	H'FEB2
Port 3 data register	P3DR	R/W	H'00	H'FF62
Port 3 register	PORT3	R	Undefined	H'FF52
Port 3 open drain control register	P3ODR	R/W	H'00	H'FF76

Notes: 1. Lower 16 bits of the address.
2. Value of bits 5 to 0.

Port 3 Data Direction Register (P3DDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	W	W	W	W	W	W

P3DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 3. Bits 7 and 6 are reserved. P3DDR cannot be read; if it is, an undefined value will be read.

Setting a P3DDR bit to 1 makes the corresponding port 3 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P3DDR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode. As the SCI is initialized, the pin states are determined by the P3DDR and P3DR specifications.

Port 3 Data Register (P3DR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P3DR is an 8-bit readable/writable register that stores output data for the port 3 pins ($P3_5$ to $P3_0$).

Bits 7 and 6 are reserved; they return an undefined value if read, and cannot be modified.

P3DR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 3 Register (PORT3)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35	P34	P33	P32	P31	P30
Initial value	:	Undefined	Undefined	—*	—*	—*	—*	—*	—*
R/W	:	—	—	R	R	R	R	R	R

Note: * Determined by state of pins $P3_5$ to $P3_0$.

PORT3 is an 8-bit read-only register that shows the pin states. Writing of output data for the port 3 pins ($P3_5$ to $P3_0$) must always be performed on P3DR.

Bits 7 and 6 are reserved; they return an undefined value if read, and cannot be modified.

If a port 3 read is performed while P3DDR bits are set to 1, the P3DR values are read. If a port 3 read is performed while P3DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT3 contents are determined by the pin states, as P3DDR and P3DR are initialized. PORT3 retains its prior state in software standby mode.

Port 3 Open Drain Control Register (P3ODR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P3ODR is an 8-bit readable/writable register that controls the PMOS on/off status for each port 3 pin ($P3_5$ to $P3_0$).

Bits 7 and 6 are reserved; they return an undefined value if read, and cannot be modified.

Setting a P3ODR bit to 1 makes the corresponding port 3 pin an NMOS open-drain output pin, while clearing the bit to 0 makes the pin a CMOS output pin.

P3ODR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.4.3 Pin Functions

Port 3 pins also function as SCI I/O pins (TxD_0, RxD_0, SCK_0, TxD_1, RxD_1, and SCK_1). Port 3 pin functions are shown in table 5.7.

Table 5.7 Port 3 Pin Functions

Pin	Selection Method and Pin Functions
$P3_5/SCK_1$	The pin function is switched as shown below according to the combination of bit C/$\overline{A}$ in the SCI1 SMR, bits CKE0 and CKE1 in SCR, and bit P35DDR.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P35DDR	0	1	—	—	—
Pin function	$P3_5$ input pin	$P3_5$ output pin*	SCK_1 output pin*	SCK_1 output pin*	SCK_1 input pin

Note: * When P35ODR = 1, the pin becomes an NMOS open-drain output.

$P3_4/SCK_0$	The pin function is switched as shown below according to the combination of bit C/$\overline{A}$ in the SCI0 SMR, bits CKE0 and CKE1 in SCR, and bit P34DDR.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P34DDR	0	1	—	—	—
Pin function	$P3_4$ input pin	$P3_4$ output pin*	SCK_0 output pin*	SCK_0 output pin*	SCK_0 input pin

Note: * When P34ODR = 1, the pin becomes an NMOS open-drain output.

Pin	Selection Method and Pin Functions
$P3_3/RxD_1$	The pin function is switched as shown below according to the combination of bit RE in the SCI1 SCR, and bit P33DDR.

RE	0		1
P33DDR	0	1	—
Pin function	$P3_3$ input pin	$P3_3$ output pin*	RxD_1 input pin

Note: * When P33ODR = 1, the pin becomes an NMOS open-drain output.

$P3_2/RxD_0$ The pin function is switched as shown below according to the combination of bit RE in the SCI0 SCR, and bit P32DDR.

RE	0		1
P32DDR	0	1	—
Pin function	$P3_2$ input pin	$P3_2$ output pin*	RxD_0 input pin

Note: * When P32ODR = 1, the pin becomes an NMOS open-drain output.

$P3_1/TxD_1$ The pin function is switched as shown below according to the combination of bit TE in the SCI1 SCR, and bit P31DDR.

TE	0		1
P31DDR	0	1	—
Pin function	$P3_1$ input pin	$P3_1$ output pin*	TxD_1 output pin

Note: * When P31ODR = 1, the pin becomes an NMOS open-drain output.

$P3_0/TxD_0$ The pin function is switched as shown below according to the combination of bit TE in the SCI0 SCR, and bit P30DDR.

TE	0		1
P30DDR	0	1	—
Pin function	$P3_0$ input pin	$P3_0$ output pin*	TxD_0 output pin

Note: * When P30ODR = 1, the pin becomes an NMOS open-drain output.

5.5 Port 4

5.5.1 Overview

Port 4 is an 8-bit input-only port. Port 4 pins also function as A/D converter analog input pins (AN_0 to AN_7) and D/A converter analog output pins (DA_0 and DA_1). Port 4 pin functions are the same in all operating modes. Figure 5.4 shows the port 4 pin configuration.

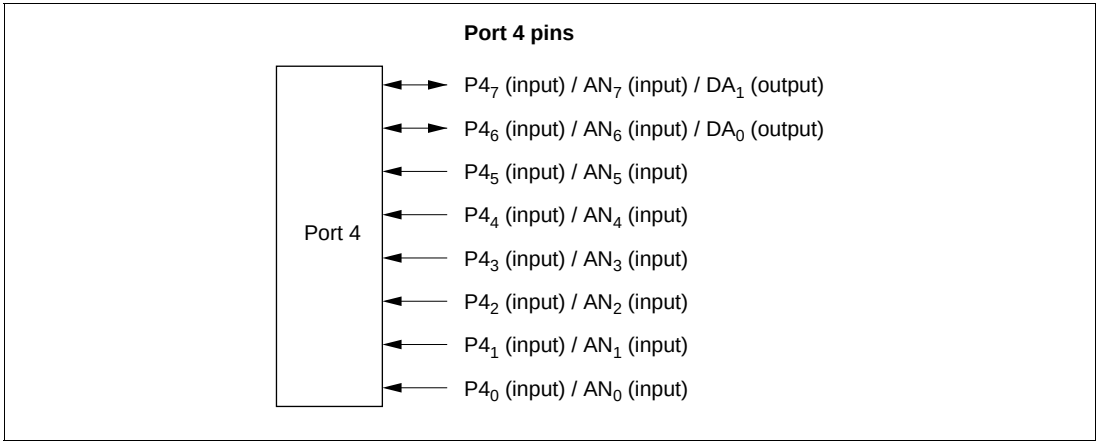


Figure 5.4 Port 4 Pin Functions

5.5.2 Register Configuration

Table 5.8 shows the port 4 register configuration. Port 4 is an input-only port, and does not have a data direction register or data register.

Table 5.8 Port 4 Register

Name	Abbreviation	R/W	Initial Value	Address*
Port 4 register	PORT4	R	Undefined	H'FF53

Note: * Lower 16 bits of the address.

Port 4 Register (PORT4): The pin states are always read when a port 4 read is performed.

Bit	:	7	6	5	4	3	2	1	0
		P47	P46	P45	P44	P43	P42	P41	P40
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins P4$_7$ to P4$_0$.

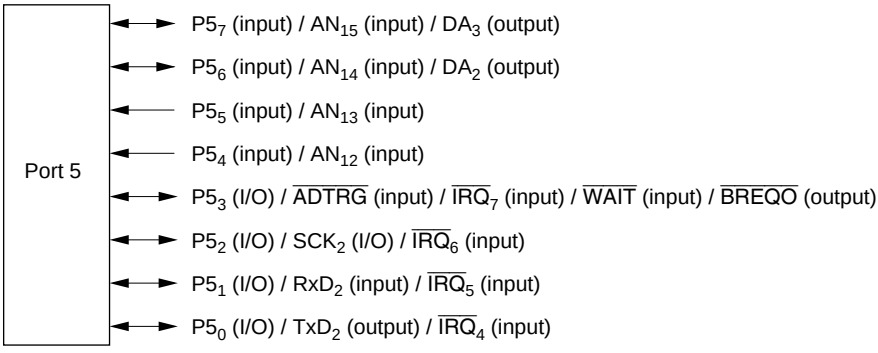
5.5.3 Pin Functions

Port 4 pins also function as A/D converter analog input pins (AN_0 to AN_7) and D/A converter analog output pins (DA_0 and DA_1).

5.6 Port 5

5.6.1 Overview

Port 5 comprises a 4-bit I/O port and a 4-bit input port. Port 5 pins also function as SCI I/O pins (TxD_2, RxD_2, and SCK_2), the A/D converter input pin ($\overline{ADTRG}$), A/D converter analog input pins (AN_{12} to AN_{15}), D/A converter analog output pins (DA_2 and DA_3),interrupt input pins ($\overline{IRQ_4}$ to $\overline{IRQ_7}$), and bus control signal I/O pins ($\overline{WAIT}$ and $\overline{BREQO}$). The pin functions can be switched by means of settings in PFCR2 and SYSCR. $\overline{IRQ_4}$ to $\overline{IRQ_7}$ are Schmitt-triggered inputs. Figure 5.5 shows the port 5 pin configuration.



Pin functions in modes 4 to 6

P5$_7$ (input) / AN$_{15}$ (input) / DA$_3$ (output)

P5$_6$ (input) / AN$_{14}$ (input) / DA$_2$ (output)

P5$_5$ (input) / AN$_{13}$ (input)

P5$_4$ (input) / AN$_{12}$ (input)

P5$_3$ (I/O) / $\overline{\text{ADTRG}}$ (input) / $\overline{\text{IRQ}}_7$ (input) / $\overline{\text{WAIT}}$ (input) / $\overline{\text{BREQO}}$ (output)

P5$_2$ (I/O) / SCK$_2$ (I/O) / $\overline{\text{IRQ}}_6$ (input)

P5$_1$ (I/O) / RxD$_2$ (input) / $\overline{\text{IRQ}}_6$ (input)

P5$_0$ (I/O) / TxD$_2$ (output) / $\overline{\text{IRQ}}_4$ (input)

Pin functions in mode 7

P5$_7$ (input) / AN$_{15}$ (input) / DA$_3$ (output)

P5$_6$ (input) / AN$_{14}$ (input) / DA$_2$ (output)

P5$_5$ (input) / AN$_{13}$ (input)

P5$_4$ (input) / AN$_{12}$ (input)

P5$_3$ (I/O) / $\overline{\text{ADTRG}}$ (intput) / $\overline{\text{IRQ}}_7$ (intput)

P5$_2$ (I/O) / SCK$_2$ (I/O) / $\overline{\text{IRQ}}_6$ (input)

P5$_1$ (I/O) / RxD$_2$ (input) / $\overline{\text{IRQ}}_5$ (input)

P5$_0$ (I/O) / TxD$_2$ (output) / $\overline{\text{IRQ}}_4$ (input)

Figure 5.5 Port 5 Pin Functions

5.6.2 Register Configuration

Table 5.9 shows the port 5 register configuration.
Bits 7 to 4 of port 5 are input ports, and have no data direction register or data register.

Table 5.9 Port 5 Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port 5 data direction register	P5DDR	W	H'0*[2]	H'FEB4
Port 5 data register	P5DR	R/W	H'0*[2]	H'FF64
Port 5 register	PORT5	R	Undefined	H'FF54
Port function control register 2	PFCR2	R/W	H'30	H'FFAC
System control register	SYSCR	R/W	H'01	H'FF39

Notes: 1. Lower 16 bits of the address.
2. Value of bits 3 to 0.

Port 5 Data Direction Register (P5DDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR
Initial value	:	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	:	—	—	—	—	W	W	W	W

P5DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 5. Bits 7 to 4 are reserved. P5DDR cannot be read; if it is, an undefined value will be read.

Setting a P5DDR bit to 1 makes the corresponding port 5 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P5DDR is initialized to H'0 (bits 3 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode. As the SCI is initialized, the pin states are determined by the P5DDR and P5DR specifications.

Port 5 Data Register (P5DR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	P53DR	P52DR	P51DR	P50DR
Initial value	:	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

P5DR is an 8-bit readable/writable register that stores output data for the port 5 pins ($P5_3$ to $P5_0$).

Bits 7 to 4 are reserved; they return an undefined value if read, and cannot be modified.

P5DR is initialized to H'0 (bits 3 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 5 Register (PORT5)

Bit	:	7	6	5	4	3	2	1	0
		P57	P56	P55	P54	P53	P52	P51	P50
Initial value	:	Undefined	Undefined	Undefined	Undefined	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins $P5_7$ to $P5_0$.

PORT5 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 5 pins ($P5_3$ to $P5_0$) must always be performed on P5DR.

Bits 7 to 4 always return the pin states when a port 5 read is performed, without regard to P5DDR.

If a port 5 read is performed while P5DDR bits are set to 1, the P5DR values are read. If a port 5 read is performed while P5DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT5 contents are determined by the pin states, as P5DDR and P5DR are initialized. PORT5 retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. Set the WAITPS bit before setting the DDR bit clear to 0 and the WAITE bit in BCRL to 1.

Bit 7 WAITPS	Description	
0	$\overline{\text{WAIT}}$ input is $P8_6$ pin	(Initial value)
1	$\overline{\text{WAIT}}$ input is $P5_3$ pin	

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. Set the BREQOPS bit before setting the BREQOE bit in BCRL to 1.

Bit 6 BREQOPS	Description	
0	$\overline{\text{BREQO}}$ output is PF_2 pin	(Initial value)
1	$\overline{\text{BREQO}}$ output is $P5_3$ pin	

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output. For details, see section 5.7, Port 6 and section 5.17, Port G.

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output. For details, see section 5.7, Port 6 and section 5.17, Port G.

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 5.16, Port F.

System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

SYSCR is an 8-bit readable/writable register that selects the interrupt control mode, controls the $\overline{\text{LWR}}$ pin, switches the $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input pins, and selects the detected edge for NMI. SYSCR is initialized to H'01 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select either of two interrupt control modes for the interrupt controller. For details, see section 3, Interrupt Controller, in the Hardware Manual.

Bit 3—NMI Edge Select (NMIEG): Selects the input edge for the NMI pin. For details, see section 3, Interrupt Controller, in the Hardware Manual.

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{\text{LWR}}$ output. For details, see section 5.16, Port F.

Bit 1—IRQ Port Switching Select (IRQPAS): Selects switching of input pins for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$. $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input is always performed from one of the ports.

Bit 1 IRQPAS	Description	
0	$P9_4$ to $P9_7$ used for $\overline{\text{RQ}}_4$ to $\overline{\text{IRQ}}_7$ input	(Initial value)
1	$P5_3$ to $P5_0$ used for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input	

Bit 0—RAM Enable (RAME): Enables or disables on-chip RAM. For details, see section 16, RAM, in the Hardware Manual.

5.6.3 Pin Functions

Port 5 pins also function as SCI I/O pins (TxD_2, RxD_2, and SCK_2), the A/D converter input pin ($\overline{ADTRG}$), interrupt input pins ($\overline{IRQ_4}$ to $\overline{IRQ_7}$), and bus control signal I/O pins ($\overline{WAIT}$ and $\overline{BREQO}$). Port 5 pins $P5_7$ to $P5_4$ also function as A/D converter analog input pins (AN_{12} to AN_{15}) and D/A converter analog output pins (DA_2 and DA_3).Port 5 pin functions are shown in table 5.10.

Table 5.10 Port 5 Pin Functions

<table>
<tr><th>Pin</th><th>Selection Method and Pin Functions</th></tr>
<tr><td>$P5_7/AN_{15}/DA_3$
$P5_6/AN_{14}/DA_2$
$P5_5/AN_{13}$
$P5_4/AN_{12}$</td><td>These pins also function as A/D converter analog input pins (AN_{12} to AN_{15}) and D/A converter analog output pins (DA_2 and DA_3). $P5_7$ to $P5_4$ have no data direction register.</td></tr>
<tr><td>$P5_3/\overline{ADTRG}/\overline{IRQ_7}/\overline{WAIT}/\overline{BREQO}$</td><td>The pin function is switched as shown below according to the combination of the operating mode, bits TRGS1 and TRGS0 in the A/D control register (ADCR), and bits IRQPAS, WAITE, WAITPS, BREQOE, BREQOPS, and P53DDR.
<table>
<tr><td>Operating mode</td><td colspan="6">Modes 4 to 6</td><td colspan="2">Mode 7</td></tr>
<tr><td>[BREQOE · BREQOPS]</td><td colspan="4">0</td><td colspan="2">1</td><td colspan="2">—</td></tr>
<tr><td>[WAITE · WAITPS]</td><td colspan="2">0</td><td colspan="2">1</td><td>0</td><td>1</td><td colspan="2">—</td></tr>
<tr><td>P53DDR</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Pin function</td><td>$P5_3$ input pin</td><td>$P5_3$ output pin</td><td>$\overline{WAIT}$ input pin</td><td>Setting pro-hibited</td><td>$\overline{BREQ_0}$ output pin</td><td>Setting pro-hibited</td><td>$P5_3$ input pin</td><td>$P5_3$ output pin</td></tr>
<tr><td></td><td colspan="8">$\overline{ADTRG}$ input pin*1</td></tr>
<tr><td></td><td colspan="8">$\overline{IRQ_7}$ interrupt input pin*2</td></tr>
</table>
Notes: 1. $\overline{ADTRG}$ input when TRGS0 = TRGS1 = 0.
2. $\overline{IRQ_7}$ input when IRQPAS = 1.</td></tr>
</table>

Pin	Selection Method and Pin Functions

$P5_2/SCK_2/\overline{IRQ}_6$

The pin function is switched as shown below according to the combination of bit C/$\overline{A}$ in the SCI2 SMR, bits CKE0 and CKE1 in SCR, and bits IRQPAS and P52DDR.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P52DDR	0	1	—	—	—
Pin function	$P5_2$ input pin	$P5_2$ output pin	SCK_2 output pin	SCK_2 output pin	SCK_2 input pin
	$\overline{IRQ}_6$ interrupt input pin*				

Note: * $\overline{IRQ}_6$ input when IRQPAS = 1.

$P5_1/RxD_2/\overline{IRQ}_5$

The pin function is switched as shown below according to the combination of bit RE in the SCI2 SCR, and bits IRQPAS and P51DDR.

RE	0		1
P51DDR	0	1	—
Pin function	$P5_1$ input pin	$P5_1$ output pin	RxD_2 input pin
	$\overline{IRQ}_5$ interrupt input pin*		

Note: * $\overline{IRQ}_5$ input when IRQPAS = 1.

$P5_0/TxD_2/\overline{IRQ}_4$

The pin function is switched as shown below according to the combination of bit TE in the SCI2 SCR, and bits IRQPAS and P50DDR.

TE	0		1
P50DDR	0	1	—
Pin function	$P5_0$ input pin	$P5_0$ output pin	TxD_2 output pin
	$\overline{IRQ}_4$ interrupt input pin*		

Note: * $\overline{IRQ}_4$ input when IRQPAS = 1.

5.7 Port 6

5.7.1 Overview

Port 6 is an 8-bit I/O port. Port 6 pins also function as interrupt input pins ($\overline{IRQ_0}$ and $\overline{IRQ_1}$) and bus control output pins ($\overline{CS_4}$ to $\overline{CS_7}$). The functions of pins $P6_5$ to $P6_2$ are the same in all operating modes, while the functions of pins $P6_7$, $P6_6$, $P6_1$, and $P6_0$ change according to the operating mode. Switching of $\overline{CS_4}$ to $\overline{CS_7}$ output can be performed by setting PFCR2. Pins $P6_7$ to $P6_4$ are Schmitt-triggered inputs. Figure 5.6 shows the port 6 pin configuration.

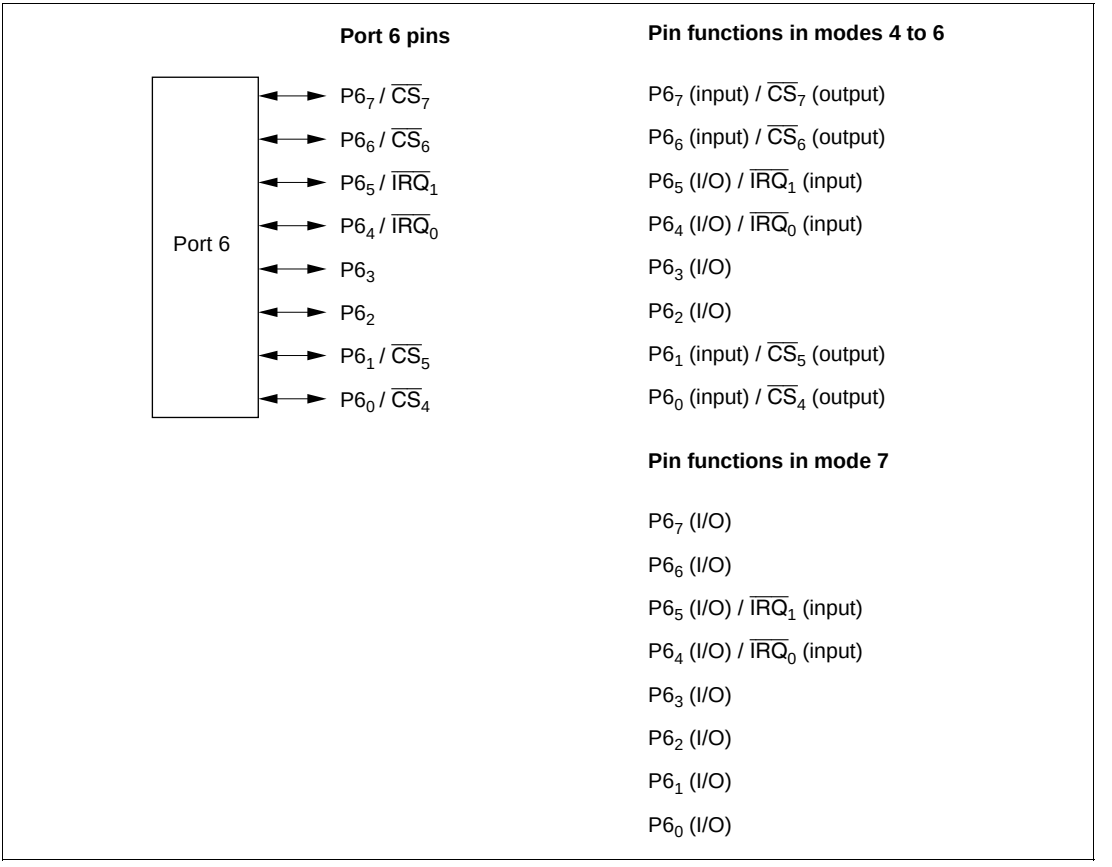


Figure 5.6 Port 6 Pin Functions

5.7.2 Register Configuration

Table 5.11 shows the port 6 register configuration.

Table 5.11 Port 6 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 6 data direction register	P6DDR	W	H'00	H'FEB5
Port 6 data register	P6DR	R/W	H'00	H'FF65
Port 6 register	PORT6	R	Undefined	H'FF55
Port function control register 2	PFCR2	R/W	H'30	H'FFAC

Note: * Lower 16 bits of the address.

Port 6 Data Direction Register (P6DDR)

Bit	:	7	6	5	4	3	2	1	0
		P67DDR	P66DDR	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

P6DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 6. P6DDR cannot be read; if it is, an undefined value will be read.

Setting a P6DDR bit to 1 makes the corresponding port 6 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P6DDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 6 Data Register (P6DR)

Bit	:	7	6	5	4	3	2	1	0
		P67DR	P66DR	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P6DR is an 8-bit readable/writable register that stores output data for the port 6 pins ($P6_7$ to $P6_0$).

P6DR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 6 Register (PORT6)

Bit	:	7	6	5	4	3	2	1	0
		P67	P66	P65	P64	P63	P62	P61	P60
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins $P6_7$ to $P6_0$.

PORT6 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 6 pins ($P6_7$ to $P6_0$) must always be performed on P6DR.

If a port 6 read is performed while P6DDR bits are set to 1, the P6DR values are read. If a port 6 read is performed while P6DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT6 contents are determined by the pin states, as P6DDR and P6DR are initialized. PORT6 retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. For details, see section 5.6, Port 5.

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. For details, see section 5.6, Port 5.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output. Only change the CS167E bit setting when the DDR bits are cleared to 0.

Bit 5 CS167E	Description	
0	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output enabled	(Initial value)

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output. Only change the CS25E bit setting when the DDR bits are cleared to 0.

Bit 4 CS25E	Description	
0	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output enabled	(Initial value)

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 5.16, Port F.

Bits 2 to 0—Reserved

5.7.3 Pin Functions

Port 6 pins also function as interrupt input pins ($\overline{IRQ_0}$ and $\overline{IRQ_1}$) and bus control output pins ($\overline{CS_4}$ to $\overline{CS_7}$). Port 6 pin functions are shown in table 5.12.

Table 5.12 Port 6 Pin Functions

Pin | **Selection Method and Pin Functions**

$P6_7/\overline{CS_7}$

The pin function is switched as shown below according to the combination of bits P67DDR and CS167E.

Mode	Modes 4 to 6				Mode 7	
CS167E	0		1		0	1
P67DDR	0	1	0	1	—	—
Pin function	$P6_7$ input pin	$P6_7$ output pin	$P6_7$ input pin	$\overline{CS_7}$ output pin	$P6_7$ input pin	$P6_7$ output pin

$P6_6/\overline{CS_6}$

The pin function is switched as shown below according to the combination of bits P66DDR and CS167E.

Mode	Modes 4 to 6				Mode 7	
CS167E	0		1		0	1
P66DDR	0	1	0	1	—	—
Pin function	$P6_6$ input pin	$P6_6$ output pin	$P6_6$ input pin	$\overline{CS_6}$ output pin	$P6_6$ input pin	$P6_6$ output pin

$P6_5/\overline{IRQ_1}$

The pin function is switched as shown below according to bit P65DDR.

P65DDR	0	1
Pin function	$P6_5$ input pin	$P6_5$ output pin
	$\overline{IRQ_1}$ interrupt input pin	

$P6_4/\overline{IRQ_0}$

The pin function is switched as shown below according to bit P64DDR.

P64DDR	0	1
Pin function	$P6_4$ input pin	$P6_4$ output pin
	$\overline{IRQ_0}$ interrupt input pin	

Pin	Selection Method and Pin Functions

$P6_3$

The pin function is switched as shown below according to bit P63DDR.

P63DDR	0	1
Pin function	$P6_3$ input pin	$P6_3$ output pin

$P6_2$

The pin function is switched as shown below according to bit P62DDR.

P62DDR	0	1
Pin function	$P6_2$ input pin	$P6_2$ output pin

$P6_1/\overline{CS}_5$

The pin function is switched as shown below according to the combination of bits P61DDR and CS25E.

Mode	Modes 4 to 6				Mode 7	
CS25E	0		1		0	1
P61DDR	0	1	0	1	—	—
Pin function	$P6_1$ input pin	$P6_1$ output pin	$P6_1$ input pin	$\overline{CS}_5$ output pin	$P6_1$ input pin	$P6_1$ output pin

$P6_0/\overline{CS}_4$

The pin function is switched as shown below according to the combination of bits P60DDR and CS25E.

Mode	Modes 4 to 6				Mode 7	
CS25E	0		1		0	1
P60DDR	0	1	0	1	—	—
Pin function	$P6_0$ input pin	$P6_0$ output pin	$P6_0$ input pin	$\overline{CS}_4$ output pin	$P6_0$ input pin	$P6_0$ output pin

5.8 Port 7

5.8.1 Overview

Port 7 is a 6-bit I/O port. Port 7 pins also function as 8-bit timer I/O pins ($TMRI_0$, $TMCI_0$, TMO_0, $TMRI_1$, $TMCI_1$, TMO_1). Port 7 pin functions are the same in all operating modes. Port 7 uses Schmitt-triggered input.

Figure 5.7 shows the port 7 pin configuration.

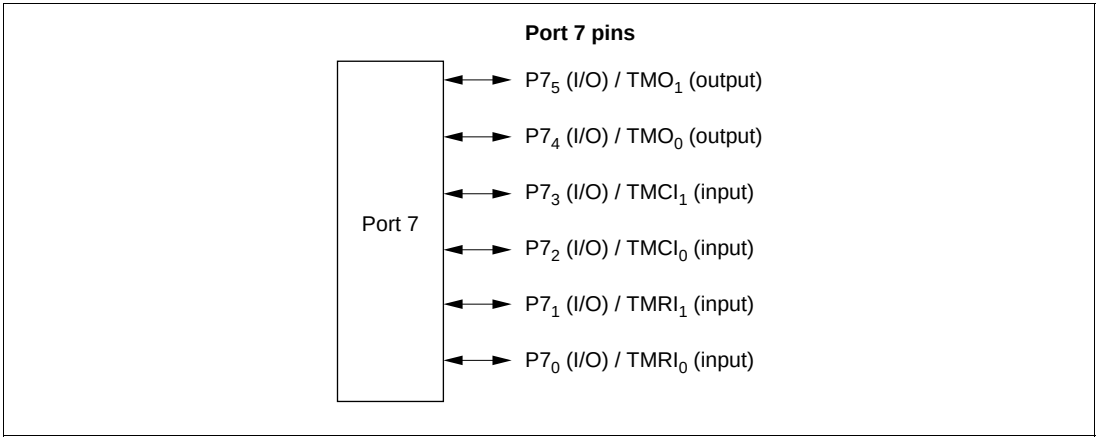


Figure 5.7 Port 7 Pin Functions

5.8.2 Register Configuration

Table 5.13 shows the port 7 register configuration.

Table 5.13 Port 7 Registers

Name	Abbreviation	R/W	Initial Value*[2]	Address*[1]
Port 7 data direction register	P7DDR	W	H'00	H'FEB6
Port 7 data register	P7DR	R/W	H'00	H'FF66
Port 7 register	PORT7	R	Undefined	H'FF56

Notes: 1. Lower 16 bits of the address.
2. Value of bits 5 to 0.

Port 7 Data Direction Register (P7DDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	W	W	W	W	W	W

P7DDR is a 6-bit write-only register, the individual bits of which specify input or output for the pins of port 7. P2DDR cannot be read; if it is, an undefined value will be read. Bits 7 and 6 are reserved.

Setting a P7DDR bit to 1 makes the corresponding port 7 pin an output pin, while clearing the bit to 0 makes the pin an input port.

P7DDR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 7 Data Register (P7DR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P7DR is a 6-bit readable/writable register that stores output data for the port 7 pins ($P7_5$ to $P7_0$). Bits 7 and 6 are reserved; they return an undefined value if read, and cannot be modified.

P7DR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 7 Register (PORT7)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P75	P74	P73	P72	P71	P70
Initial value	:	Undefined	Undefined	—*	—*	—*	—*	—*	—*
R/W	:	—	—	R	R	R	R	R	R

Note: * Determined by state of pins $P7_5$ to $P7_0$.

PORT7 is a 6-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 7 pins ($P7_5$ to $P7_0$) must always be performed on P7DR.

If a port 7 read is performed while P7DDR bits are set to 1, the P7DR values are read. If a port 7 read is performed while P7DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT7 contents are determined by the pin states, as P7DDR and P7DR are initialized. PORT7 retains its prior state in software standby mode.

5.8.3 Pin Functions

Port 7 pins also function as 8-bit timer I/O pins ($TMRI_0$, $TMCI_0$, TMO_0, $TMRI_1$, $TMCI_1$, and TMO_1). Port 7 pin functions are shown in table 5.14.

Table 5.14 Port 7 Pin Functions

<table>
<tr><th>Pin</th><th>Selection Method and Pin Functions</th></tr>
<tr><td>$P7_5/TMO_1$</td><td>The pin function is switched as shown below according to the combination of bits OS3 to OS0 in 8-bit timer TCSR1 and bit P75DDR.
<table>
<tr><td>OS3 to OS0</td><td colspan="2">All 0</td><td>Not all 0</td></tr>
<tr><td>P75DDR</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>Pin function</td><td>$P7_5$ input pin</td><td>$P7_5$ output pin</td><td>TMO_1 output pin</td></tr>
</table></td></tr>
<tr><td>$P7_4/TMO_0$</td><td>The pin function is switched as shown below according to the combination of bits OS3 to OS0 in 8-bit timer TCSR0 and bit P74DDR.
<table>
<tr><td>OS3 to OS0</td><td colspan="2">All 0</td><td>Not all 0</td></tr>
<tr><td>P74DDR</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>Pin function</td><td>$P7_4$ input pin</td><td>$P7_4$ output pin</td><td>TMO_0 output pin</td></tr>
</table></td></tr>
<tr><td>$P7_3/TMCI_1$</td><td>The pin function is switched as shown below according to bit P73DDR.
When this pin is used as an 8-bit timer external clock input pin, the external clock is selected with bits CKS2 to CKS0 in TCR1.
<table>
<tr><td>P73DDR</td><td>0</td><td>1</td></tr>
<tr><td rowspan="2">Pin function</td><td>$P7_3$ input pin</td><td>$P7_3$ output pin</td></tr>
<tr><td colspan="2">$TMCI_1$ input pin</td></tr>
</table></td></tr>
</table>

Pin	Selection Method and Pin Functions
$P7_2/TMCI_0$	The pin function is switched as shown below according to bit P72DDR. When this pin is used as an 8-bit timer external clock input pin, the external clock is selected with bits CKS2 to CKS0 in TCR0.

P72DDR	0	1
Pin function	$P7_2$ input pin	$P7_2$ output pin
	$TMCI_0$ input pin	

$P7_1/TMRI_1$	The pin function is switched as shown below according to bit P71DDR. When this pin is used as an 8-bit timer counter reset pin, bits CCLR1 and CCLR0 in TCR1 are both set to 1.

P71DDR	0	1
Pin function	$P7_1$ input pin	$P7_1$ output pin
	$TMRI_1$ input pin	

$P7_0/TMRI_0$	The pin function is switched as shown below according to bit P70DDR. When this pin is used as an 8-bit timer counter reset pin, bits CCLR1 and CCLR0 in TCR0 are both set to 1.

P70DDR	0	1
Pin function	$P7_0$ input pin	$P7_0$ output pin
	$TMRI_0$ input pin	

5.9 Port 8

5.9.1 Overview

Port 8 is a 7-bit I/O port. Port 8 pins also function as DMAC I/O pins ($\overline{DREQ_0}$, $\overline{TEND_0}$, $\overline{DACK_0}$, $\overline{DREQ_1}$, $\overline{TEND_1}$, and $\overline{DACK_1}$) and a bus control signal input pin ($\overline{WAIT}$). Figure 5.8 shows the port 8 pin configuration.

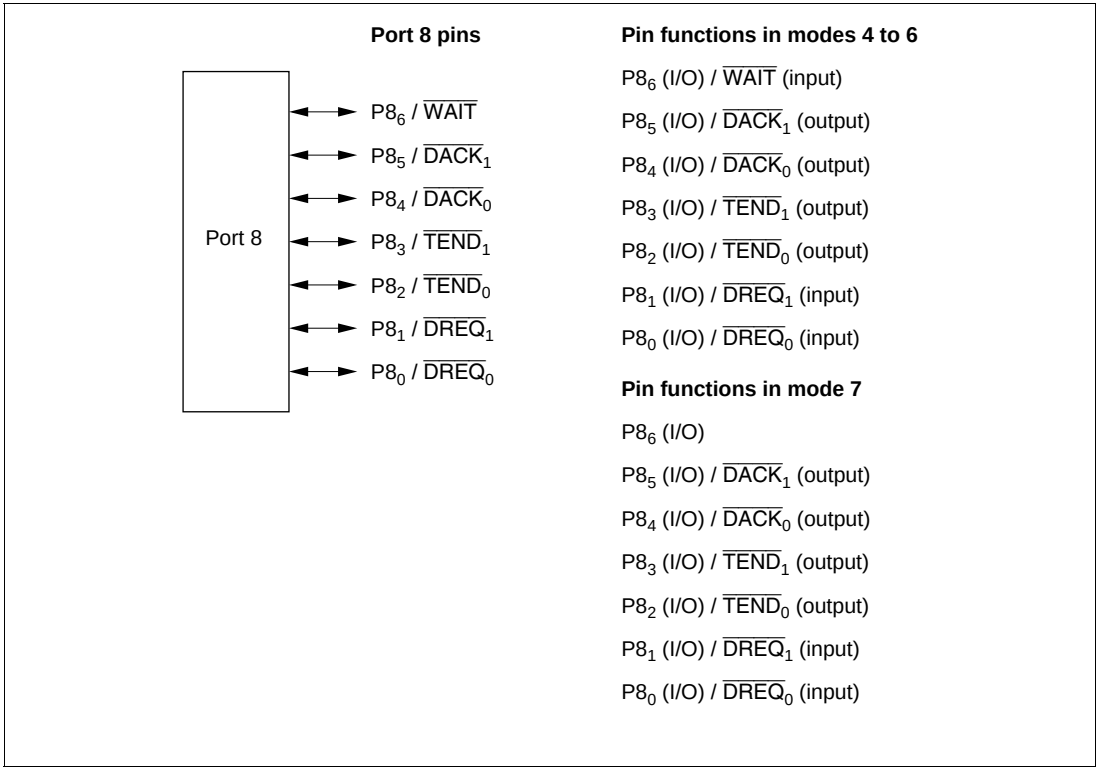


Figure 5.8 Port 8 Pin Functions

5.9.2 Register Configuration

Table 5.15 shows the port 8 register configuration.

Table 5.15 Port 8 Registers

Name	Abbreviation	R/W	Initial Value*[2]	Address*[1]
Port 8 data direction register	P8DDR	W	H'00	H'FEB7
Port 8 data register	P8DR	R/W	H'00	H'FF67
Port 8 register	PORT8	R	Undefined	H'FF57
Port function control register2	PFCR2	R/W	H'30	H'FFAC

Notes: 1. Lower 16 bits of the address.
2. Value of bits 6 to 0.

Port 8 Data Direction Register (P8DDR)

Bit	:	7	6	5	4	3	2	1	0
		—	P86DDR	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR
Initial value	:	Undefined	0	0	0	0	0	0	0
R/W	:	—	W	W	W	W	W	W	W

P8DDR is a 7-bit write-only register, the individual bits of which specify input or output for the pins of port 8. P2DDR cannot be read; if it is, an undefined value will be read. Bit 7 is reserved.

Setting a P8DDR bit to 1 makes the corresponding port 8 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P8DDR is initialized to H'00 (bits 6 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 8 Data Register (P8DR)

Bit	:	7	6	5	4	3	2	1	0
		—	P86DR	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR
Initial value	:	Undefined	0	0	0	0	0	0	0
R/W	:	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P8DR is a 7-bit readable/writable register that stores output data for the port 8 pins ($P8_6$ to $P8_0$).

Bit 7 is reserved; it returns an undefined value if read, and cannot be modified.

P8DR is initialized to H'00 (bits 6 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 8 Register (PORT8)

Bit	:	7	6	5	4	3	2	1	0
		—	P86	P85	P84	P83	P82	P81	P80
Initial value	:	Undefined	—*	—*	—*	—*	—*	—*	—*
R/W	:	—	R	R	R	R	R	R	R

Note: * Determined by state of pins $P8_6$ to $P8_0$.

PORT8 is a 7-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 8 pins ($P8_6$ to $P8_0$) must always be performed on P8DR.

Bit 7 is reserved; it returns an undefined value if read, and cannot be modified.

If a port 8 read is performed while P8DDR bits are set to 1, the P8DR values are read. If a port 8 read is performed while P8DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT8 contents are determined by the pin states, as P8DDR and P8DR are initialized. PORT8 retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ output pin. Set the WAITPS bit before setting the DDR bit clear to 0 and the WAITE bit in BCRL to 1.

Bit 7 WAITPS	Description	
0	$\overline{\text{WAIT}}$ output is pin $P8_6$	(Initial value)
1	$\overline{\text{WAIT}}$ output is pin $P5_3$	

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. For details, see section 5.6, Port 5 and section 5.16, Port F.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{CS}_1$, $\overline{CS}_6$, and $\overline{CS}_7$ output. For details, see section 5.7, Port 6 and section 5.17, Port G.

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$, and $\overline{CS}_5$ output. For details, see section 5.7, Port 6 and section 5.17, Port G.

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 5.16, Port F.

Bits 2 to 0—Reserved

5.9.3 Pin Functions

Port 8 pins also function as DMAC I/O pins ($\overline{DREQ_0}$, $\overline{TEND_0}$, $\overline{DACK_0}$, $\overline{DREQ_1}$, $\overline{TEND_1}$, and $\overline{DACK_1}$) and a bus control signal input pin ($\overline{WAIT}$). Port 8 pin functions are shown in table 5.16.

Table 5.16 Port 8 Pin Functions

Pin | **Selection Method and Pin Functions**

$P8_6/\overline{WAIT}$

The pin function is switched as shown below according to the combination of the operating mode and bits WAITE, WAITPS, and P86DDR.

Operating mode	Modes 4 to 6				Mode 7	
[WAITE · $\overline{WAITPS}$]	0		1		—	
P86DDR	0	1	0	1	0	1
Pin function	$P8_6$ input pin	$P8_6$ output pin	$\overline{WAIT}$ input pin	Setting pro-hibited	$P8_6$ input pin	$P8_6$ output pin

$P8_5/\overline{DACK_1}$

The pin function is switched as shown below according to the combination of bit SAE1 in DMABCRH and bit P85DDR.

SAE1	0		1
P85DDR	0	1	—
Pin function	$P8_5$ input pin	$P8_5$ output pin	$\overline{DACK_1}$ output pin

$P8_4/\overline{DACK_0}$

The pin function is switched as shown below according to the combination of bit SAE0 in DMABCRH and bit P84DDR.

SAE0	0		1
P84DDR	0	1	—
Pin function	$P8_4$ input pin	$P8_4$ output pin	$\overline{DACK_0}$ output pin

Pin	Selection Method and Pin Functions

$P8_3/\overline{TEND}_1$

The pin function is switched as shown below according to the combination of bit TEE1 in the DMAC's DMATCR and bit P83DDR.

TEE1	0		1
P83DDR	0	1	—
Pin function	$P8_3$ input pin	$P8_3$ output pin	$\overline{TEND}_1$ output pin

$P8_2/\overline{TEND}_0$

The pin function is switched as shown below according to the combination of bit TEE0 in the DMAC's DMATCR and bit P82DDR.

TEE0	0		1
P82DDR	0	1	—
Pin function	$P8_2$ input pin	$P8_2$ output pin	$\overline{TEND}_0$ output pin

$P8_1/\overline{DREQ}_1$

The pin function is switched as shown below according to bit P81DDR.

P81DDR	0	1
Pin function	$P8_1$ input pin	$P8_1$ output pin
	$\overline{DREQ}_1$ input pin	

$P8_0/\overline{DREQ}_0$

The pin function is switched as shown below according to bit P80DDR.

P80DDR	0	1
Pin function	$P8_0$ input pin	$P8_0$ output pin
	$\overline{DREQ}_0$ input pin	

5.10 Port 9

5.10.1 Overview

Port 9 is a 6-bit I/O port. Port 9 pins also function as interrupt input pins ($\overline{IRQ_2}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$, $\overline{IRQ_6}$, and $\overline{IRQ_7}$). When the IRQPAS bit is set to 1, inputs $\overline{IRQ_4}$ to $\overline{IRQ_7}$ are switched to $P5_0$ to $P5_3$. Port 9 pin functions are the same in all operating modes. Port 9 uses Schmitt-triggered input. Figure 5.9 shows the port 9 pin configuration.

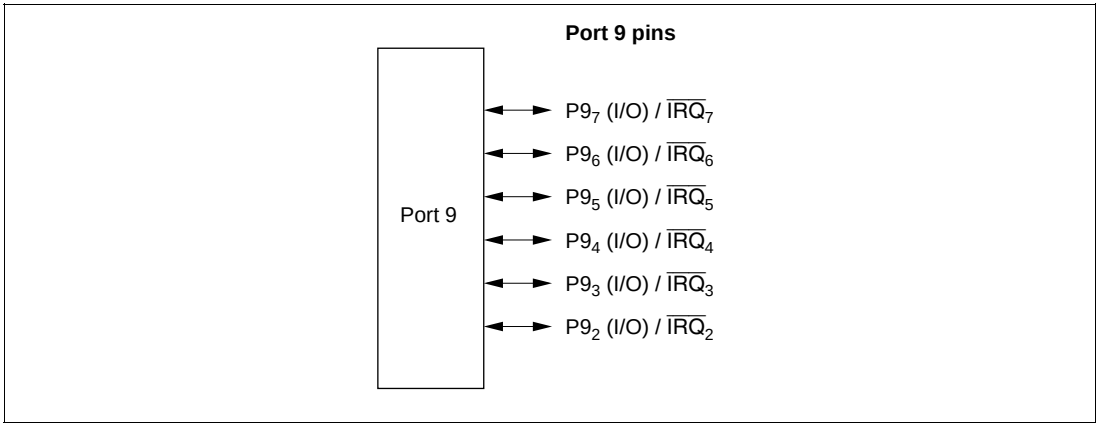


Figure 5.9 Port 9 Pin Functions

5.10.2 Register Configuration

Table 5.17 shows the port 9 register configuration.

Table 5.17 Port 9 Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port 9 data direction register	P9DDR	W	H'00*[2]	H'FEB8
Port 9 data register	P9DR	R/W	H'00*[2]	H'FF68
Port 9 register	PORT9	R	Undefined	H'FF58
System control register	SYSCR	R/W	H'01	H'FF39

Notes: 1. Lower 16 bits of the address.
2. Value of bits 7 to 2.

Port 9 Data Direction Register (P9DDR)

Bit	:	7	6	5	4	3	2	1	0
		P97DDR	P96DDR	P95DDR	P94DDR	P93DDR	P92DDR	—	—
Initial value	:	0	0	0	0	0	0	Undefined	Undefined
R/W	:	W	W	W	W	W	W	—	—

P9DDR is a 6-bit write-only register, the individual bits of which specify input or output for the pins of port 9. P2DDR cannot be read; if it is, an undefined value will be read. Bits 1 and 0 are reserved.

Setting a P9DDR bit to 1 makes the corresponding port 9 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P9DDR is initialized to H'00 (bits 7 to 2) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 9 Data Register (P9DR)

Bit	:	7	6	5	4	3	2	1	0
		P97DR	P96DR	P95DR	P94DR	P93DR	P92DR	—	—
Initial value	:	0	0	0	0	0	0	Undefined	Undefined
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	—	—

P9DR is a 6-bit readable/writable register that stores output data for the port 9 pins ($P9_7$ to $P9_2$). Bits 1 and 0 are reserved; they return an undefined value if read, and cannot be modified.
P9DR is initialized to H'00 (bits 7 to 2) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port 9 Register (PORT9)

Bit	:	7	6	5	4	3	2	1	0
		P97	P96	P95	P94	P93	P92	—	—
Initial value	:	—*	—*	—*	—*	—*	—*	Undefined	Undefined
R/W	:	R	R	R	R	R	R	—	—

Note: * Determined by state of pins $P9_7$ to $P9_2$.

PORT9 is a 6-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 9 pins ($P9_7$ to $P9_2$) must always be performed on P9DR.

Bits 1 and 0 are reserved; they return an undefined value if read, and cannot be modified.

If a port 9 read is performed while P9DDR bits are set to 1, the P9DR values are read. If a port 9 read is performed while P9DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT9 contents are determined by the pin states, as P9DDR and P9DR are initialized. PORT9 retains its prior state in software standby mode.

System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

SYSCR is an 8-bit readable/writable register that selects the interrupt control mode, controls the $\overline{\text{LWR}}$ pin, switches the $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input pins, and selects the detected edge for NMI. SYSCR is initialized to H'01 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select either of two interrupt control modes for the interrupt controller. For details, see section 3, Interrupt Controller, in the Hardware Manual.

Bit 3—NMI Edge Select (NMIEG): Selects the input edge for the NMI pin. For details, see section 3, Interrupt Controller, in the Hardware Manual.

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{\text{LWR}}$ output. For details, see section 5.16, Port F.

Bit 1—IRQ Port Switching Select (IRQPAS): Selects switching of input pins $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$. $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input is always performed from one of the ports.

Bit 1 IRQPAS	Description	
0	$P9_4$ to $P9_7$ used for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input	(Initial value)
1	$P5_0$ to $P5_3$ used for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input	

Bit 0—RAM Enable (RAME): Enables or disables on-chip RAM. For details, see section 16, RAM, in the Hardware Manual.

5.10.3 Pin Functions

Port 9 pins also function as interrupt input pins ($\overline{IRQ_2}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, $\overline{IRQ_5}$, $\overline{IRQ_6}$, and $\overline{IRQ_7}$). Port 9 pin functions are shown in table 5.18.

Table 5.18 Port 9 Pin Functions

Pin	Selection Method and Pin Functions
$P9_7/\overline{IRQ_7}$	The pin function is switched as shown below according to the combination of bits P97DDR and IRQPAS.

P97DDR	0	1
Pin function	$P9_7$ input pin	$P9_7$ output pin
	$\overline{IRQ_7}$ interrupt input pin*	

Note: * $\overline{IRQ_7}$ input when IRQPAS = 0.

$P9_6/\overline{IRQ_6}$	The pin function is switched as shown below according to the combination of bits P96DDR and IRQPAS.

P96DDR	0	1
Pin function	$P9_6$ input pin	$P9_6$ output pin
	$\overline{IRQ_6}$ interrupt input pin*	

Note: * $\overline{IRQ_6}$ input when IRQPAS = 0.

$P9_5/\overline{IRQ_5}$	The pin function is switched as shown below according to the combination of bits P95DDR and IRQPAS.

P95DDR	0	1
Pin function	$P9_5$ input pin	$P9_5$ output pin
	$\overline{IRQ_5}$ interrupt input pin*	

Note: * $\overline{IRQ_5}$ input when IRQPAS = 0.

$P9_4/\overline{IRQ_4}$	The pin function is switched as shown below according to the combination of bits P94DDR and IRQPAS.

P94DDR	0	1
Pin function	$P9_4$ input pin	$P9_4$ output pin
	$\overline{IRQ_4}$ interrupt input pin*	

Note: * $\overline{IRQ_4}$ input when IRQPAS = 0.

Pin	Selection Method and Pin Functions
$P9_3/\overline{IRQ}_3$	The pin function is switched as shown below according to the combination of bits P93DDR and IRQPAS.

P93DDR	0	1
Pin function	$P9_3$ input pin	$P9_3$ output pin
	$\overline{IRQ}_3$ interrupt input pin*	

Note: * $\overline{IRQ}_3$ input when IRQPAS = 0.

$P9_2/\overline{IRQ}_2$ The pin function is switched as shown below according to the combination of bits P92DDR and IRQPAS.

P92DDR	0	1
Pin function	$P9_2$ input pin	$P9_2$ output pin
	$\overline{IRQ}_2$ interrupt input pin*	

Note: * $\overline{IRQ}_2$ input when IRQPAS = 0.

5.11 Port A

5.11.1 Overview

Port A is an 8-bit I/O port. Port A pins also function as address bus outputs. The pin functions change according to the operating mode. The address output or port output function can be selected by means of bits A23E to A20E in PFCR1.

Port A has a built-in MOS input pull-up function that can be controlled by software. Pins PA_7 to PA_4 are Schmitt-triggered inputs.

Figure 5.10 shows the port A pin configuration.

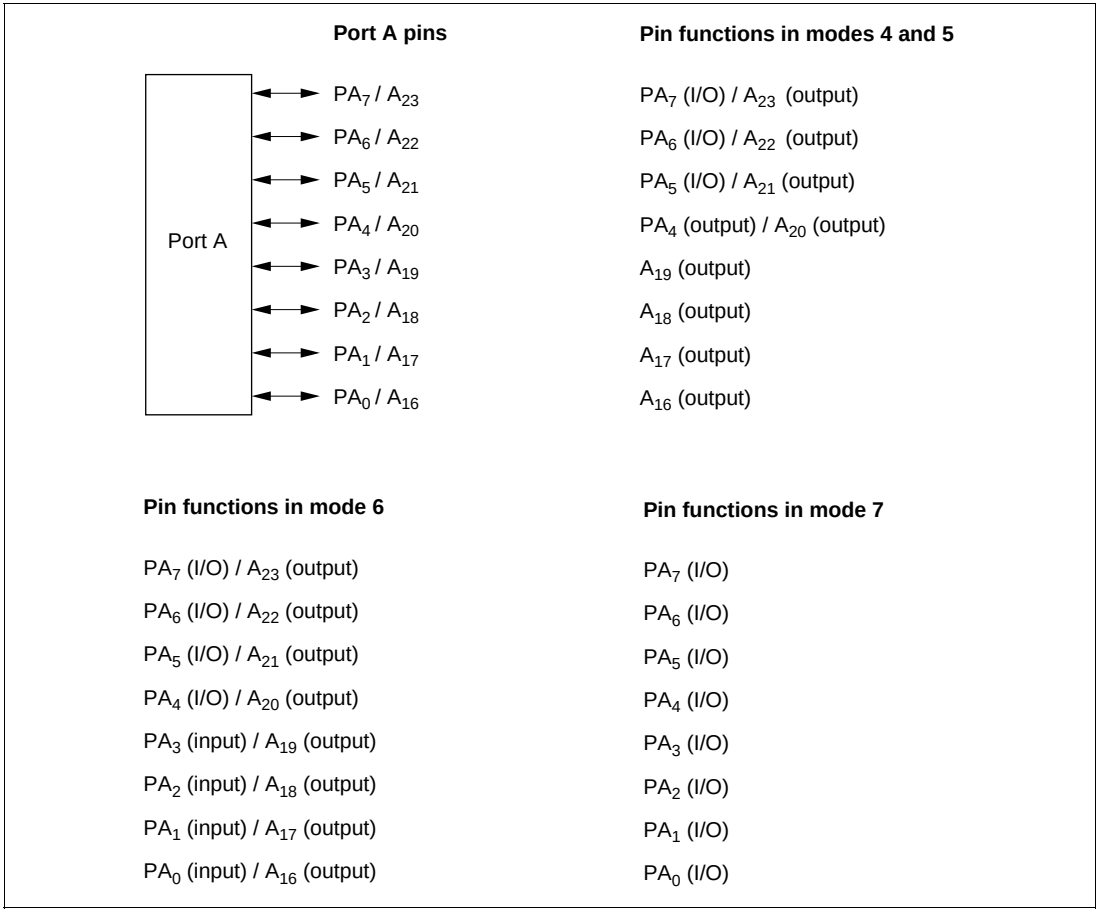


Figure 5.10 Port A Pin Functions

5.11.2 Register Configuration

Table 5.19 shows the port A register configuration.

Table 5.19 Port A Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port A data direction register	PADDR	W	H'00	H'FEB9
Port A data register	PADR	R/W	H'00	H'FF69
Port A register	PORTA	R	Undefined	H'FF59
Port A MOS pull-up control register	PAPCR	R/W	H'00	H'FF70
Port A open drain control register	PAODR	R/W	H'00	H'FF77
Port function control register 1	PFCR1	R/W	H'0F	H'FF45

Note: * Lower 16 bits of the address.

Port A Data Direction Register (PADDR)

Bit	:	7	6	5	4	3	2	1	0
		PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PADDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port A. PADDR cannot be read; if it is, an undefined value will be read.

PADDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

Port A Data Register (PADR)

Bit	:	7	6	5	4	3	2	1	0
		PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PADR is an 8-bit readable/writable register that stores output data for the port A pins (PA_7 to PA_0).

PADR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port A Register (PORTA)

Bit	:	7	6	5	4	3	2	1	0
		PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PA_7 to PA_0.

PORTA is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port A pins (PA_7 to PA_0) must always be performed on PADR.

If a port A read is performed while PADDR bits are set to 1, the PADR values are read. If a port A read is performed while PADDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTA contents are determined by the pin states, as PADDR and PADR are initialized. PORTA retains its prior state in software standby mode.

Port A MOS Pull-Up Control Register (PAPCR)

Bit	:	7	6	5	4	3	2	1	0
		PA7PCR	PA6PCR	PA5PCR	PA4PCR	PA3PCR	PA2PCR	PA1PCR	PA0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PAPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port A on an individual bit basis.

All the bits are valid in modes 6 and 7, and bits 7 to 5 are valid in modes 4 and 5. When a PADDR bit is cleared to 0 (input port setting), setting the corresponding PAPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PAPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port A Open Drain Control Register (PAODR)

Bit	:	7	6	5	4	3	2	1	0
		PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PAODR is an 8-bit readable/writable register that controls whether PMOS is on or off for each port A pin (PA_7 to PA_0).

PAODR is valid only in mode 7. Do not PAODR bits to 1 in modes 4 to 6.

Setting a PAODR bit to 1 makes the corresponding port A pin an NMOS open-drain output, while clearing the bit to 0 makes the pin a CMOS output.

PAODR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port Function Control Register 1 (PFCR1)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	A23E	A22E	A21E	A20E
Initial value	:	0	0	0	0	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR1 is an 8-bit readable/writable register that performs I/O port control. PFCR1 is initialized to H'0F by a reset, and in hardware standby mode.

Bits 7 to 4—Reserved: Only 0 should be written to these bits.

Bit 3—Address 23 Enable (A23E): Enables or disables address output 23 (A_{23}). This bit is valid in modes 4 to 6.

Bit 3 A23E	Description	
0	DR is output when PA7DDR = 1	
1	A_{23} is output when PA7DDR = 1	(Initial value)

Bit 2—Address 22 Enable (A22E): Enables or disables address output 22 (A_{22}). This bit is valid in modes 4 to 6.

Bit 2 A22E	Description	
0	DR is output when PA6DDR = 1	
1	A_{22} is output when PA6DDR = 1	(Initial value)

Bit 1—Address 21 Enable (A21E): Enables or disables address output 21 (A_{21}). This bit is valid in modes 4 to 6.

Bit 1 A21E	Description	
0	DR is output when PA5DDR = 1	
1	A_{21} is output when PA5DDR = 1	(Initial value)

Bit 0—Address 20 Enable (A20E): Enables or disables address output 20 (A_{20}). This bit is valid in modes 4 to 6.

Bit 0 A20E	Description	
0	DR is output when PA4DDR = 1	
1	A_{20} is output when PA4DDR = 1	(Initial value)

5.11.3 Pin Functions

Port A pins function as address outputs and I/O ports. Port A pin functions are shown in table 5.20.

Table 5.20 Port A Pin Functions

Pin	Selection Method and Pin Functions
PA_7/A_{23}	The pin function is switched as shown below according to the combination of the operating mode and bits A23E and PA7DDR.

Operating mode	Modes 4 to 6				Mode 7	
A23E	0		1		—	
PA7DDR	0	1	0	1	0	1
Pin function	PA_7 input pin	PA_7 output pin	PA_7 input pin	A_{23} output pin	PA_7 input pin	PA_7 output pin

PA_6/A_{22}	The pin function is switched as shown below according to the combination of the operating mode and bits A22E and PA6DDR.

Operating mode	Modes 4 to 6				Mode 7	
A22E	0		1		—	
PA6DDR	0	1	0	1	0	1
Pin function	PA_6 input pin	PA_6 output pin	PA_6 input pin	A_{22} output pin	PA_6 input pin	PA_6 output pin

PA_5/A_{21}	The pin function is switched as shown below according to the combination of the operating mode and bits A21E and PA5DDR.

Operating mode	Modes 4 to 6				Mode 7	
A21E	0		1		—	
PA5DDR	0	1	0	1	0	1
Pin function	PA_5 input pin	PA_5 output pin	PA_5 input pin	A_{21} output pin	PA_5 input pin	PA_5 output pin

Pin	Selection Method and Pin Functions
PA_4/A_{20}	The pin function is switched as shown below according to the combination of the operating mode and bits A20E and PA4DDR.

Operating mode	Modes 4 and 5			Mode 6				Mode 7	
A20E	0		1	0		1		—	
PA4DDR	0	1	—	0	1	0	1	0	1
Pin function	Setting pro-hibited	PA_4 output pin	A_{20} output pin	PA_4 input pin	PA_4 output pin	PA_4 input pin	A_{20} output pin	PA_4 input pin	PA_4 output pin

PA_3/A_{19}
PA_2/A_{18}
PA_1/A_{17}
PA_0/A_{16}

The pin function is switched as shown below according to the combination of the operating mode and bit PAnDDR.

Operating mode	Modes 4 and 5	Mode 6		Mode 7	
PAnDDR	—	0	1	0	1
Pin function	Address output pin	PA_n input pin	A_m output pin	PA_n input pin	PA_n output pin

(n = 0 to 3)
(m = 16 to 19)

5.11.4 MOS Input Pull-Up Function

Port A has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used by pins PA_7 to PA_5 in modes 4 and 5, and by all pins in modes 6 and 7. MOS input pull-up can be specified as on or off on an individual bit basis.

When a PADDR bit is cleared to 0, setting the corresponding PAPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.21 summarizes the MOS input pull-up states.

Table 5.21 MOS Input Pull-Up States (Port A)

Modes		Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
6, 7	PA_7 to PA_0	Off	Off	On/off	On/off
4, 5	PA_7 to PA_5			On/off	On/off
	PA_4 to PA_0			Off	Off

Legend

Off: MOS input pull-up is always off.

On/off: On when PADDR = 0 and PAPCR = 1; otherwise off.

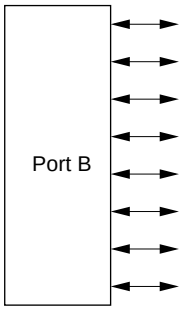
5.12 Port B

5.12.1 Overview

Port B is an 8-bit I/O port. Port B has an address bus output function, and the pin functions change according to the operating mode.

Port B has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.11 shows the port B pin configuration.



Port B pins	Pin functions in modes 4 and 5	Pin functions in mode 6	Pin functions in mode 7
PB_7 / A_{15}	A_{15} (output)	PB_7 (input) / A_{15} (output)	PB_7 (I/O)
PB_6 / A_{14}	A_{14} (output)	PB_6 (input) / A_{14} (output)	PB_6 (I/O)
PB_5 / A_{13}	A_{13} (output)	PB_5 (input) / A_{13} (output)	PB_5 (I/O)
PB_4 / A_{12}	A_{12} (output)	PB_4 (input) / A_{12} (output)	PB_4 (I/O)
PB_3 / A_{11}	A_{11} (output)	PB_3 (input) / A_{11} (output)	PB_3 (I/O)
PB_2 / A_{10}	A_{10} (output)	PB_2 (input) / A_{10} (output)	PB_2 (I/O)
PB_1 / A_9	A_9 (output)	PB_1 (input) / A_9 (output)	PB_1 (I/O)
PB_0 / A_8	A_8 (output)	PB_0 (input) / A_8 (output)	PB_0 (I/O)

Figure 5.11 Port B Pin Functions

5.12.2 Register Configuration

Table 5.22 shows the port B register configuration.

Table 5.22 Port B Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port B data direction register	PBDDR	W	H'00	H'FEBA
Port B data register	PBDR	R/W	H'00	H'FF6A
Port B register	PORTB	R	Undefined	H'FF5A
Port B MOS pull-up control register	PBPCR	R/W	H'00	H'FF71

Note: * Lower 16 bits of the address.

Port B Data Direction Register (PBDDR)

Bit	:	7	6	5	4	3	2	1	0
		PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PBDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port B. PBDDR cannot be read; if it is, an undefined value will be read.

PBDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 4 and 5

  The corresponding port B pins are address outputs irrespective of the value of the PBDDR bits.

- Mode 6

  Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port.

- Mode 7

  Setting a PBDDR bit to 1 makes the corresponding port B pin an output port, while clearing the bit to 0 makes the pin an input port.

Port B Data Register (PBDR)

Bit	:	7	6	5	4	3	2	1	0
		PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PBDR is an 8-bit readable/writable register that stores output data for the port B pins (PB_7 to PB_0). PBDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port B Register (PORTB)

Bit	:	7	6	5	4	3	2	1	0
		PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PB_7 to PB_0.

PORTB is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port B pins (PB_7 to PB_0) must always be performed on PBDR.

If a port B read is performed while PBDDR bits are set to 1, the PBDR values are read. If a port B read is performed while PBDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTB contents are determined by the pin states, as PBDDR and PBDR are initialized. PORTB retains its prior state in software standby mode.

Port B MOS Pull-Up Control Register (PBPCR)

Bit	:	7	6	5	4	3	2	1	0
		PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PBPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port B on an individual bit basis.

When a PBDDR bit is cleared to 0 (input port setting) in mode 6 or 7, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PBPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.12.3 Pin Functions

Modes 4 and 5: In modes 4 and 5, port B pins are automatically designated as address outputs.

Port B pin functions in modes 4 and 5 are shown in figure 5.12.

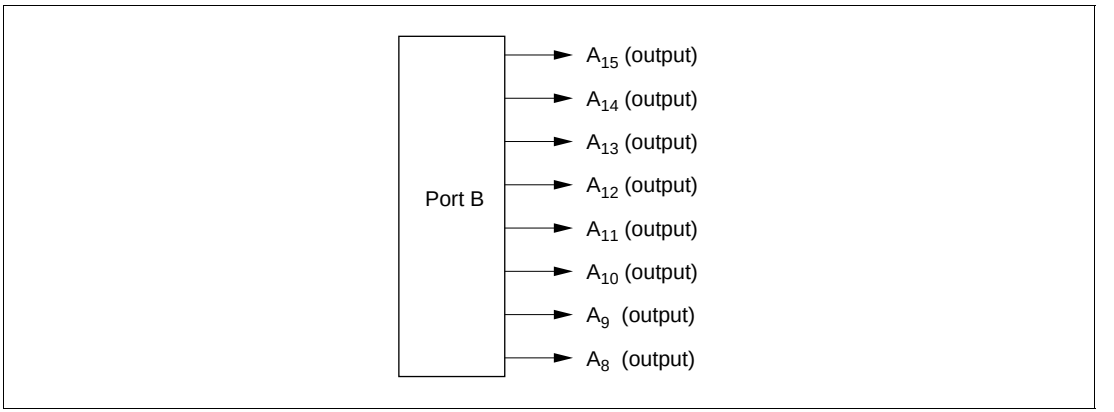


Figure 5.12 Port B Pin Functions (Modes 4 and 5)

Mode 6: In mode 6, port B pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port.

Port B pin functions in mode 6 are shown in figure 5.13

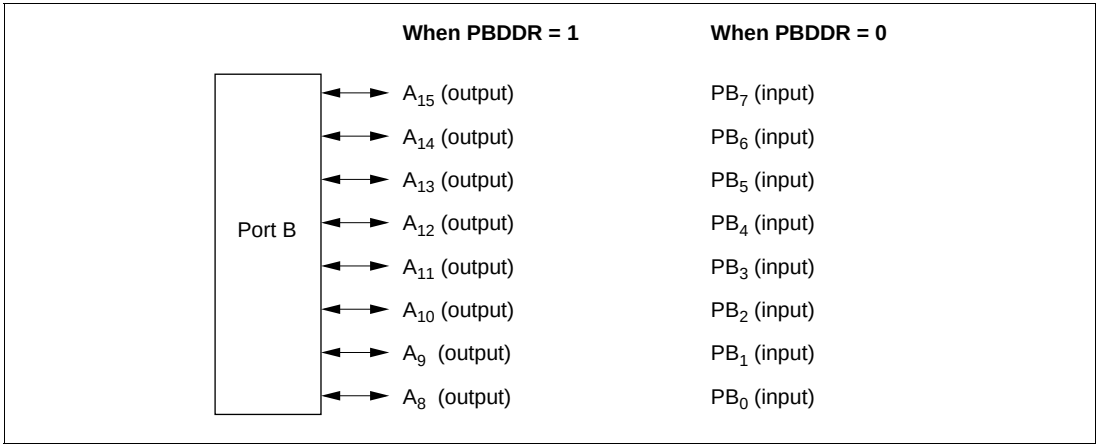


Figure 5.13 Port B Pin Functions (Mode 6)

Mode 7: In mode 7, port B pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PBDDR bit to 1 makes the corresponding port B pin an output port, while clearing the bit to 0 makes the pin an input port.

Port B pin functions in mode 7 are shown in figure 5.14.

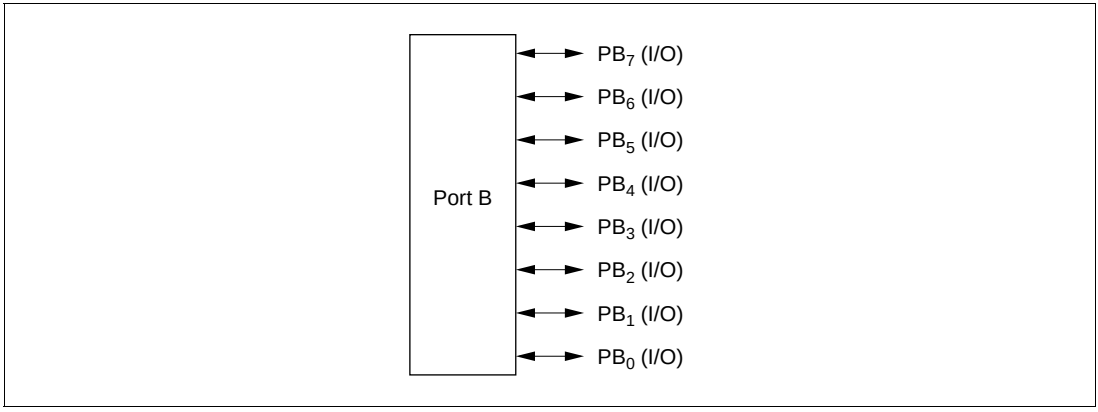


Figure 5.14 Port B Pin Functions (Mode 7)

5.12.4 MOS Input Pull-Up Function

Port B has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 6 and 7, and can be specified as on or off on an individual bit basis.

When a PBDDR bit is cleared to 0 in mode 6 or 7, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.23 summarizes the MOS input pull-up states.

Table 5.23 MOS Input Pull-Up States (Port B)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4, 5	Off	Off	Off	Off
6, 7			On/off	On/off

Legend

Off: MOS input pull-up is always off.

On/off: On when PBDDR = 0 and PBPCR = 1; otherwise off.

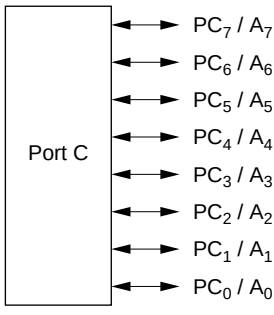
5.13 Port C

5.13.1 Overview

Port C is an 8-bit I/O port. Port C has an address bus output function, and the pin functions change according to the operating mode.

Port C has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.15 shows the port C pin configuration.



Pin functions in modes 4 and 5	Pin functions in mode 6	Pin functions in mode 7
A_7 (output)	PC_7 (input) / A_7 (output)	PC_7 (I/O)
A_6 (output)	PC_6 (input) / A_6 (output)	PC_6 (I/O)
A_5 (output)	PC_5 (input) / A_5 (output)	PC_5 (I/O)
A_4 (output)	PC_4 (input) / A_4 (output)	PC_4 (I/O)
A_3 (output)	PC_3 (input) / A_3 (output)	PC_3 (I/O)
A_2 (output)	PC_2 (input) / A_2 (output)	PC_2 (I/O)
A_1 (output)	PC_1 (input) / A_1 (output)	PC_1 (I/O)
A_0 (output)	PC_0 (input) / A_0 (output)	PC_0 (I/O)

Figure 5.15 Port C Pin Functions

5.13.2 Register Configuration

Table 5.24 shows the port C register configuration.

Table 5.24 Port C Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port C data direction register	PCDDR	W	H'00	H'FEBB
Port C data register	PCDR	R/W	H'00	H'FF6B
Port C register	PORTC	R	Undefined	H'FF5B
Port C MOS pull-up control register	PCPCR	R/W	H'00	H'FF72

Note: * Lower 16 bits of the address.

Port C Data Direction Register (PCDDR)

Bit	:	7	6	5	4	3	2	1	0
		PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PCDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port C. PCDDR cannot be read; if it is, an undefined value will be read.

PCDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 4 and 5

  The corresponding port C pins are address outputs irrespective of the value of the PCDDR bits.

- Mode 6

  Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.

- Mode 7

  Setting a PCDDR bit to 1 makes the corresponding port C pin an output port, while clearing the bit to 0 makes the pin an input port.

Port C Data Register (PCDR)

Bit	:	7	6	5	4	3	2	1	0
		PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCDR is an 8-bit readable/writable register that stores output data for the port C pins (PC_7 to PC_0).

PCDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port C Register (PORTC)

Bit	:	7	6	5	4	3	2	1	0
		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PC_7 to PC_0.

PORTC is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port C pins (PC_7 to PC_0) must always be performed on PCDR.

If a port C read is performed while PCDDR bits are set to 1, the PCDR values are read. If a port C read is performed while PCDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTC contents are determined by the pin states, as PCDDR and PCDR are initialized. PORTC retains its prior state in software standby mode.

Port C MOS Pull-Up Control Register (PCPCR)

Bit	:	7	6	5	4	3	2	1	0
		PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port C on an individual bit basis.

When a PCDDR bit is cleared to 0 (input port setting) in mode 6 or 7, setting the corresponding PCPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PCPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.13.3 Pin Functions

Modes 4 and 5: In modes 4 and 5, port C pins are automatically designated as address outputs.

Port C pin functions in modes 4 and 5 are shown in figure 5.16.

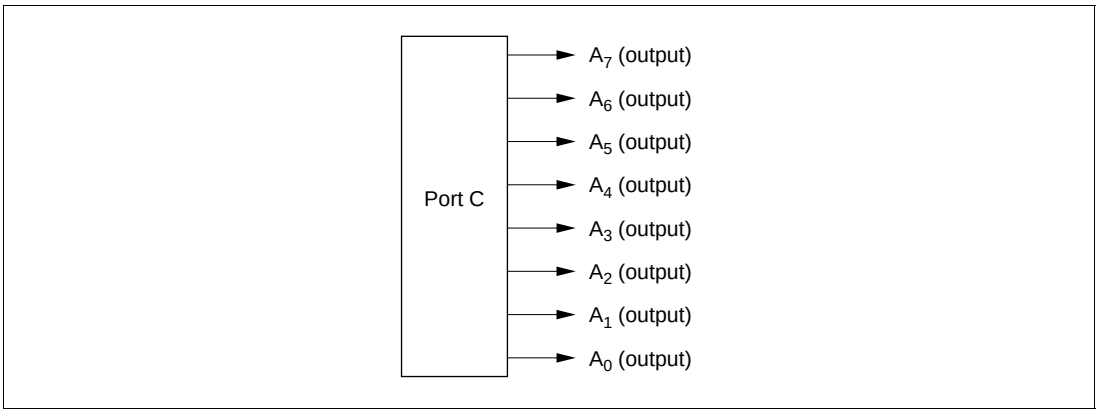


Figure 5.16 Port C Pin Functions (Modes 4 and 5)

Mode 6: In mode 6, port C pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.

Port C pin functions in mode 6 are shown in figure 5.17.

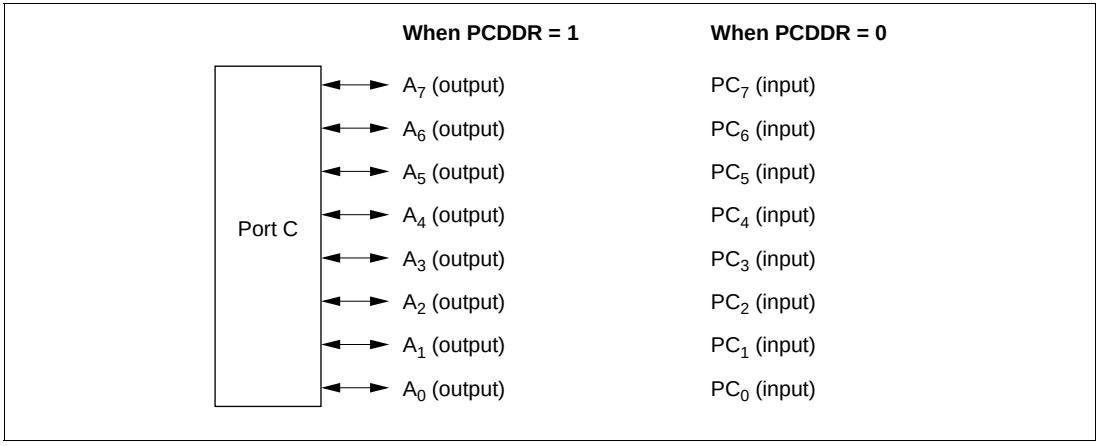


Figure 5.17 Port C Pin Functions (Mode 6)

Mode 7: In mode 7, port C pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PCDDR bit to 1 makes the corresponding port C pin an output port, while clearing the bit to 0 makes the pin an input port.

Port C pin functions in mode 7 are shown in figure 5.18.

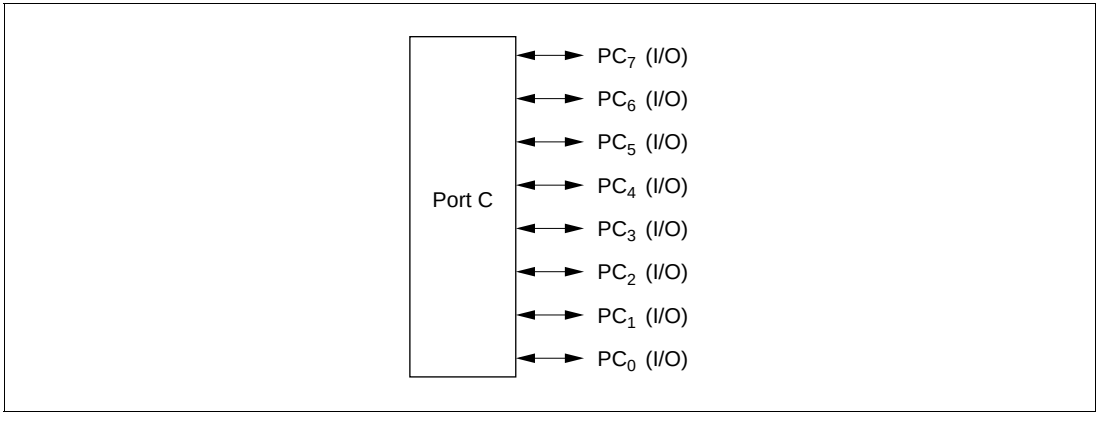


Figure 5.18 Port C Pin Functions (Mode 7)

5.13.4 MOS Input Pull-Up Function

Port C has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 6 and 7, and can be specified as on or off on an individual bit basis.

When a PCDDR bit is cleared to 0 in mode 6 or 7, setting the corresponding PCPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.25 summarizes the MOS input pull-up states.

Table 5.25 MOS Input Pull-Up States (Port C)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4, 5	Off	Off	Off	Off
6, 7			On/off	On/off

Legend

Off: MOS input pull-up is always off.

On/off: On when PCDDR = 0 and PCPCR = 1; otherwise off.

5.14 Port D

5.14.1 Overview

Port D is an 8-bit I/O port. Port D has a data bus I/O function, and the pin functions change according to the operating mode.

Port D has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.19 shows the port D pin configuration.

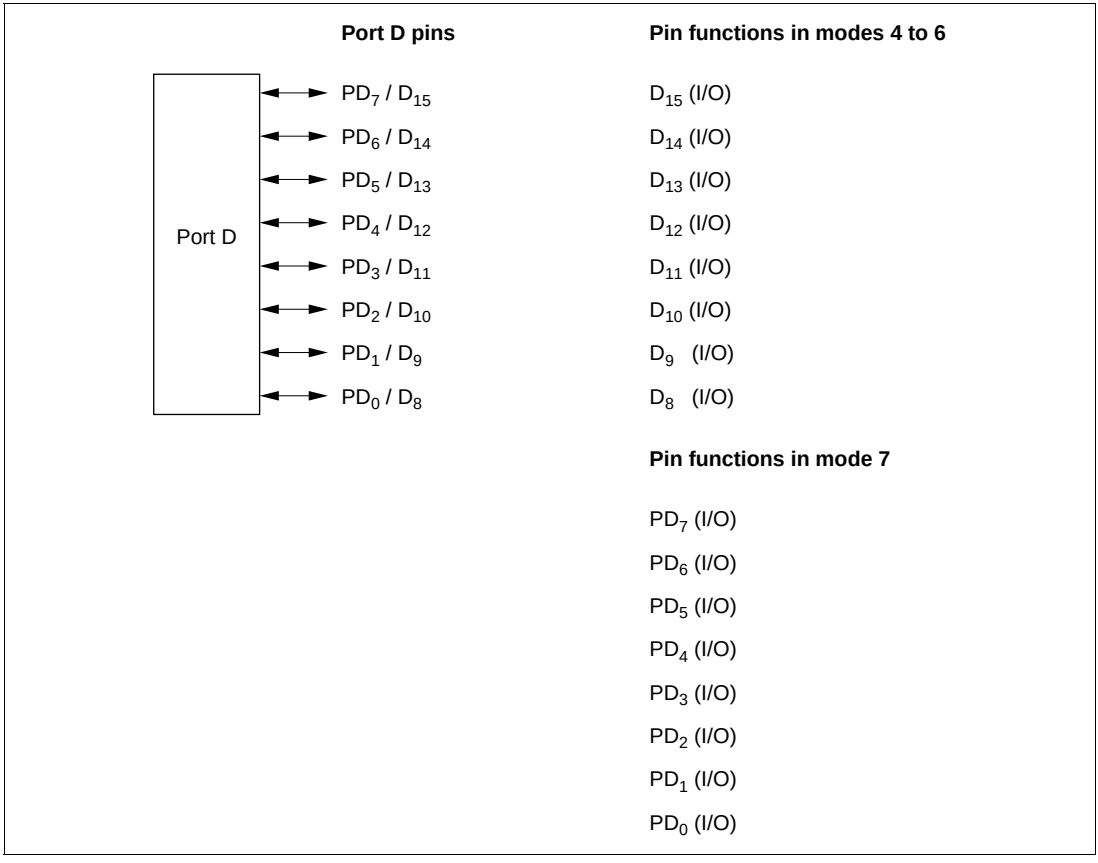


Figure 5.19 Port D Pin Functions

5.14.2 Register Configuration

Table 5.26 shows the port D register configuration.

Table 5.26 Port D Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port D data direction register	PDDDR	W	H'00	H'FEBC
Port D data register	PDDR	R/W	H'00	H'FF6C
Port D register	PORTD	R	Undefined	H'FF5C
Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FF73

Note: * Lower 16 bits of the address.

Port D Data Direction Register (PDDDR)

Bit	:	7	6	5	4	3	2	1	0
		PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PDDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port D. PDDDR cannot be read; if it is, an undefined value will be read.

PDDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 4 to 6

  The input/output direction specification by PDDDR is ignored, and port D is automatically designated for data I/O.

- Mode 7

  Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

Port D Data Register (PDDR)

Bit	:	7	6	5	4	3	2	1	0
		PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDDR is an 8-bit readable/writable register that stores output data for the port D pins (PD_7 to PD_0).

PDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port D Register (PORTD)

Bit	:	7	6	5	4	3	2	1	0
		PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PD_7 to PD_0.

PORTD is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port D pins (PD_7 to PD_0) must always be performed on PDDR.

If a port D read is performed while PDDDR bits are set to 1, the PDDR values are read. If a port D read is performed while PDDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTD contents are determined by the pin states, as PDDDR and PDDR are initialized. PORTD retains its prior state in software standby mode.

Port D MOS Pull-Up Control Register (PDPCR)

Bit	:	7	6	5	4	3	2	1	0
		PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port D on an individual bit basis.

When a PDDDR bit is cleared to 0 (input port setting) in mode 7, setting the corresponding PDPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PDPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.14.3 Pin Functions

Modes 4 to 6: In modes 4 to 6, port D pins are automatically designated as data I/O pins.

Port D pin functions in modes 4 to 6 are shown in figure 5.20.

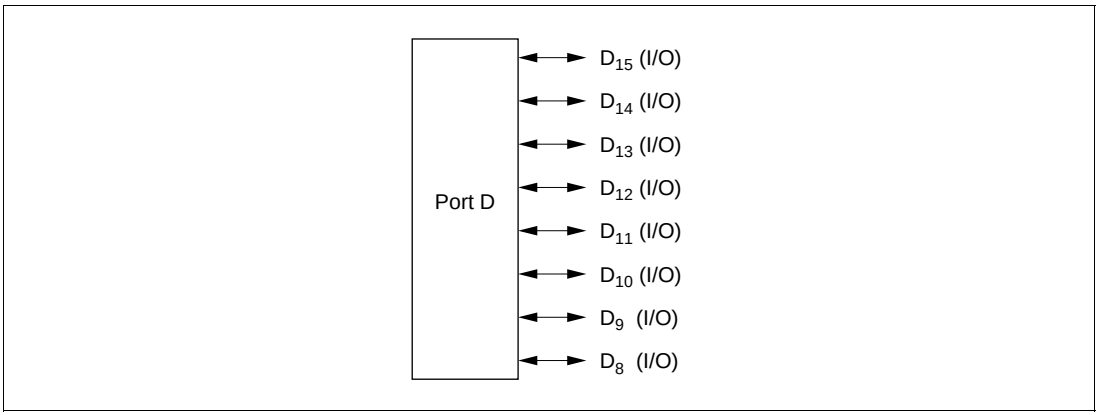


Figure 5.20 Port D Pin Functions (Modes 4 to 6)

Mode 7: In mode 7, port D pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

Port D pin functions in mode 7 are shown in figure 5.21.

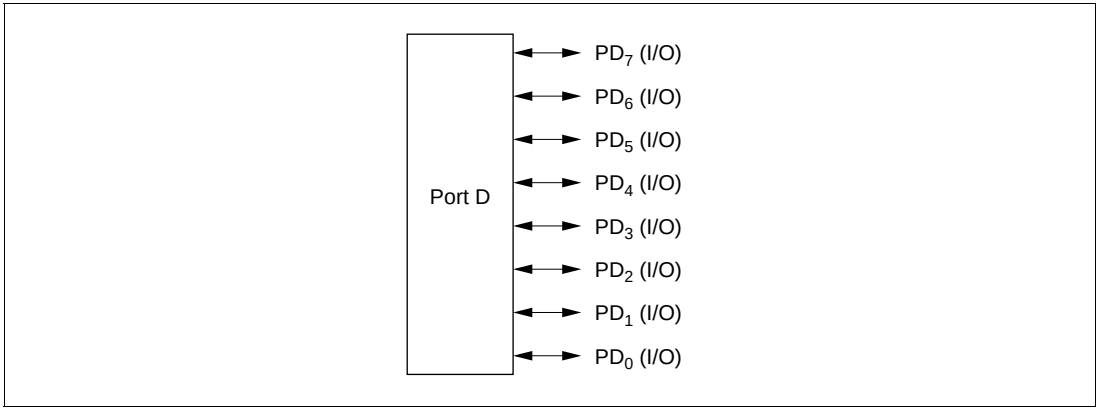


Figure 5.21 Port D Pin Functions (Mode 7)

5.14.4 MOS Input Pull-Up Function

Port D has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in mode 7, and can be specified as on or off on an individual bit basis.

When a PDDDR bit is cleared to 0 in mode 7, setting the corresponding PDPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.27 summarizes the MOS input pull-up states.

Table 5.27 MOS Input Pull-Up States (Port D)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4 to 6	Off	Off	Off	Off
7			On/off	On/off

Legend

Off: MOS input pull-up is always off.

On/off: On when PDDDR = 0 and PDPCR = 1; otherwise off.

5.15 Port E

5.15.1 Overview

Port E is an 8-bit I/O port. Port E has a data bus I/O function, and the pin functions change according to the operating mode and whether 8-bit or 16-bit bus mode is selected.

Port E has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.22 shows the port E pin configuration.

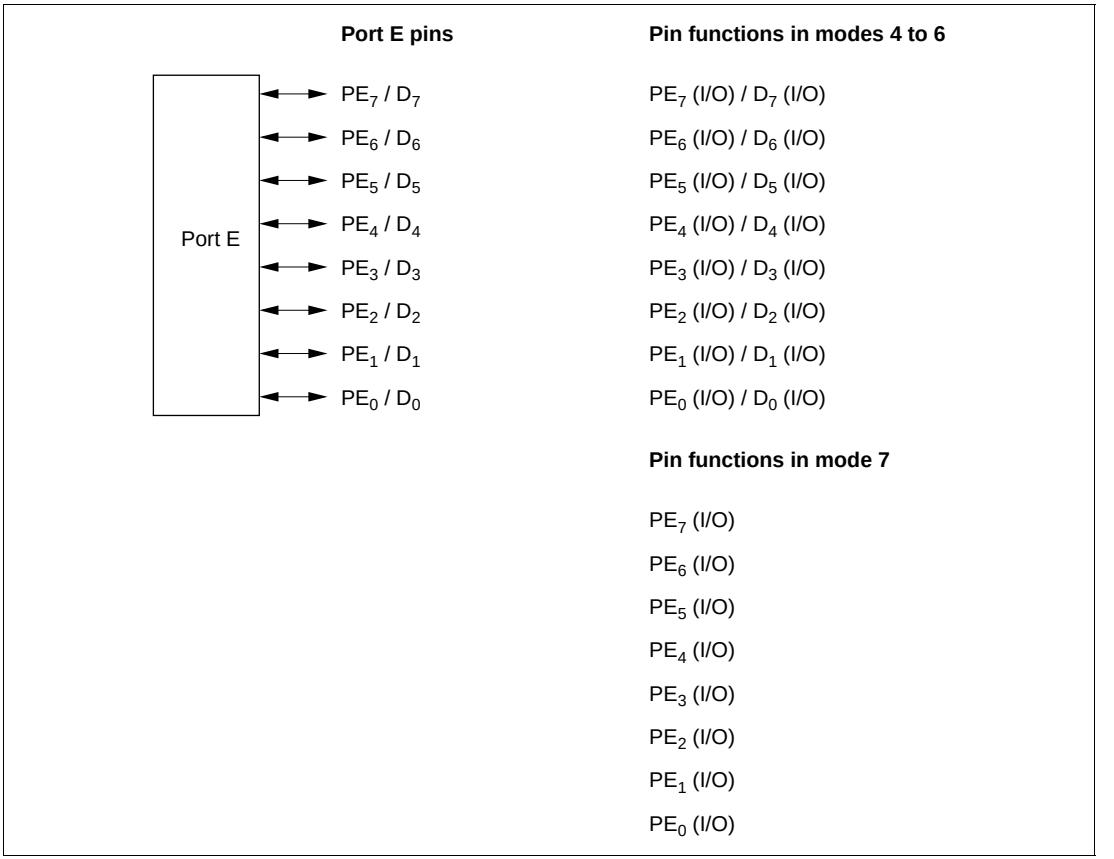


Figure 5.22 Port E Pin Functions

5.15.2 Register Configuration

Table 5.28 shows the port E register configuration.

Table 5.28 Port E Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port E data direction register	PEDDR	W	H'00	H'FEBD
Port E data register	PEDR	R/W	H'00	H'FF6D
Port E register	PORTE	R	Undefined	H'FF5D
Port E MOS pull-up control register	PEPCR	R/W	H'00	H'FF74

Note: * Lower 16 bits of the address.

Port E Data Direction Register (PEDDR)

Bit	:	7	6	5	4	3	2	1	0
		PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PEDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port E. PEDDR cannot be read; if it is, an undefined value will be read.

PEDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 4 to 6

  When 8-bit bus mode has been selected, port E pins function as I/O ports. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

  When 16-bit bus mode has been selected, the input/output direction specification by PEDDR is ignored, and port E is designated for data I/O.

  For details of 8-bit and 16-bit bus modes, see section 4, Bus Controller.

- Mode 7

  Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

Port E Data Register (PEDR)

Bit	:	7	6	5	4	3	2	1	0
		PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PEDR is an 8-bit readable/writable register that stores output data for the port E pins (PE_7 to PE_0).

PEDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port E Register (PORTE)

Bit	:	7	6	5	4	3	2	1	0
		PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PE_7 to PE_0.

PORTE is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port E pins (PE_7 to PE_0) must always be performed on PEDR.

If a port E read is performed while PEDDR bits are set to 1, the PEDR values are read. If a port E read is performed while PEDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTE contents are determined by the pin states, as PEDDR and PEDR are initialized. PORTE retains its prior state in software standby mode.

Port E MOS Pull-Up Control Register (PEPCR)

Bit	:	7	6	5	4	3	2	1	0
		PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PEPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port E on an individual bit basis.

When a PEDDR bit is cleared to 0 (input port setting) in mode 4, 5, or 6 with 8-bit bus mode selected, or in mode 7, setting the corresponding PEPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PEPCR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

5.15.3 Pin Functions

Modes 4 to 6: In modes 4 to 6, when 8-bit access is designated and 8-bit bus mode is selected, port E pins are automatically designated as I/O ports. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

When 16-bit bus mode is selected, the input/output direction specification by PEDDR is ignored, and port E is designated for data I/O.

Port E pin functions in modes 4 to 6 are shown in figure 5.23.

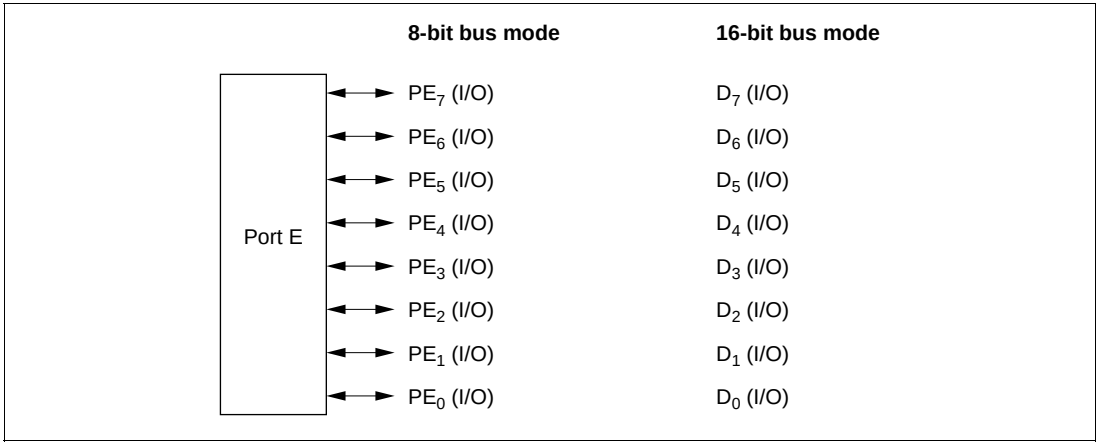


Figure 5.23 Port E Pin Functions (Modes 4 to 6)

Mode 7: In mode 7, port E pins function as I/O ports. Input or output can be specified for each pin on a bit-by-bit basis. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

Port E pin functions in mode 7 are shown in figure 5.24.

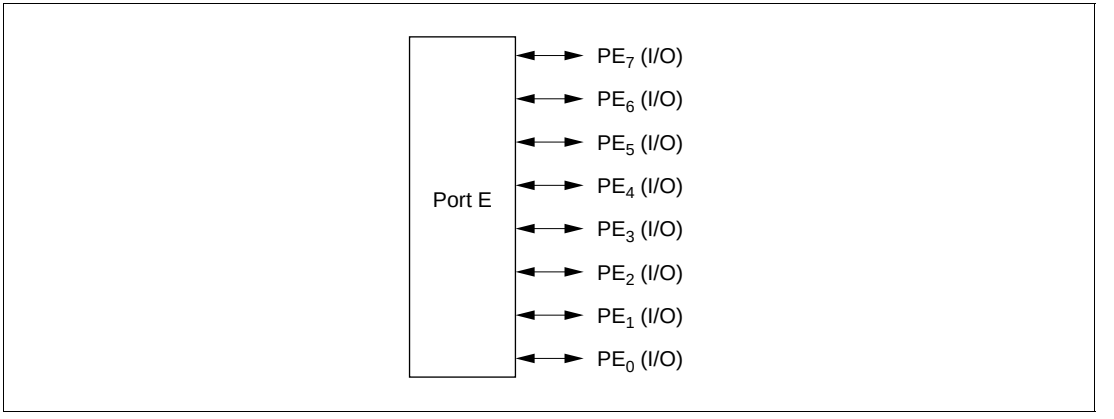


Figure 5.24 Port E Pin Functions (Mode 7)

5.15.4 MOS Input Pull-Up Function

Port E has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 4, 5, and 6 when 8-bit bus mode is selected, or in mode 7, and can be specified as on or off on an individual bit basis.

When a PEDDR bit is cleared to 0 in mode 4, 5, or 6 when 8-bit bus mode is selected, or in mode 7, setting the corresponding PEPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.29 summarizes the MOS input pull-up states.

Table 5.29 MOS Input Pull-Up States (Port E)

Modes		Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
7		Off	Off	On/off	On/off
4 to 6	8-bit bus				
	16-bit bus			Off	Off

Legend

Off: MOS input pull-up is always off.

On/off: On when PEDDR = 0 and PEPCR = 1; otherwise off.

5.16 Port F

5.16.1 Overview

Port F is an 8-bit I/O port. Port F pins also function as bus control signal input/output pins ($\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, $\overline{LWR}$, $\overline{LCAS}$, $\overline{BREQO}$, $\overline{BREQ}$, and $\overline{BACK}$) and the system clock (ø) output pin. The $\overline{AS}$, $\overline{LWR}$, and $\overline{BREQO}$ output pins can be switched by means of settings in PFCR2 and SYSCR.

Figure 5.25 shows the port F pin configuration.

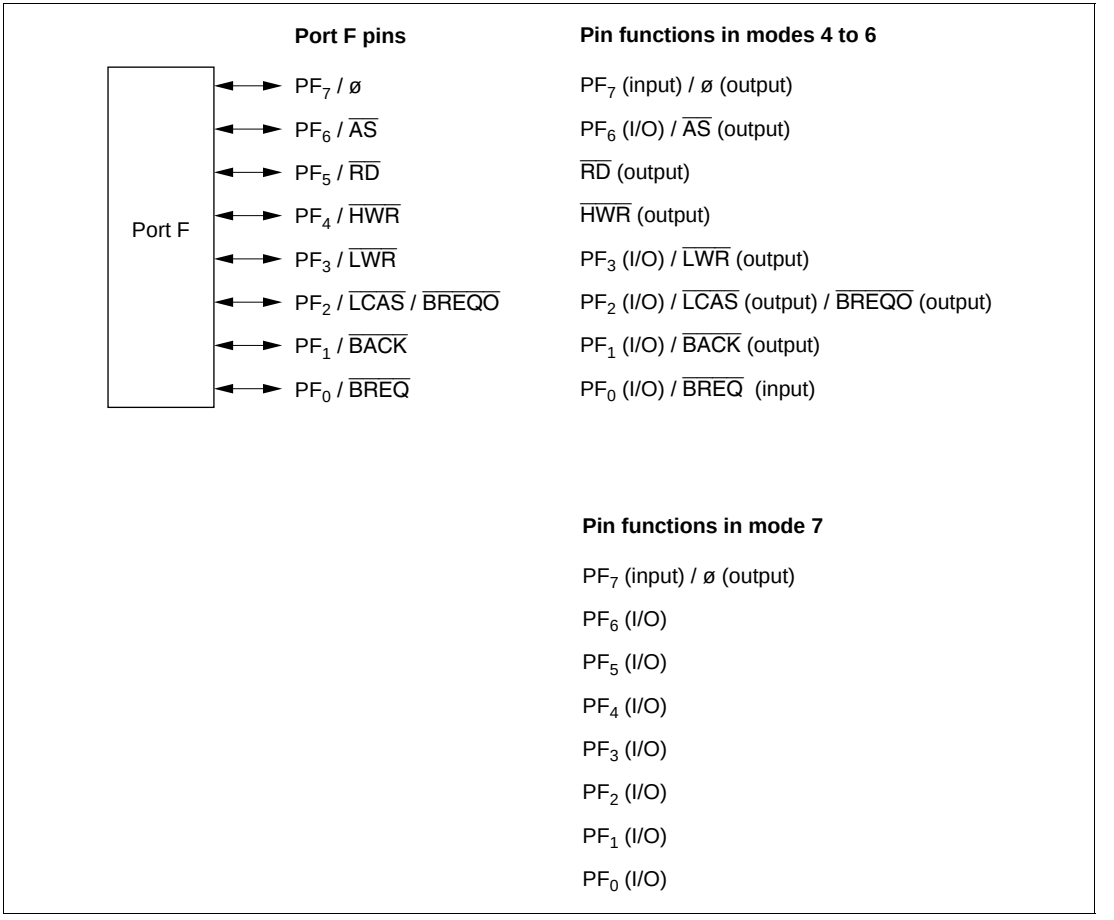


Figure 5.25 Port F Pin Functions

5.16.2 Register Configuration

Table 5.30 shows the port F register configuration.

Table 5.30 Port F Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port F data direction register	PFDDR	W	H'80/H'00*[2]	H'FEBE
Port F data register	PFDR	R/W	H'00	H'FF6E
Port F register	PORTF	R	Undefined	H'FF5E
Port function control register 2	PFCR2	R/W	H'30	H'FFAC
System control register	SYSCR	R/W	H'01	H'FF39

Notes: 1. Lower 16 bits of the address.
2. Initial value depends on the mode.

Port F Data Direction Register (PFDDR)

Bit	:	7	6	5	4	3	2	1	0
		PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 4 to 6									
Initial value	:	1	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W
Mode 7									
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PFDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port F. PFDDR cannot be read; if it is, an undefined value will be read.

PFDDR is initialized by a reset, and in hardware standby mode, to H'80 in modes 4 to 6, and to H'00 in mode 7. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

Port F Data Register (PFDR)

Bit	:	7	6	5	4	3	2	1	0
		PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFDR is an 8-bit readable/writable register that stores output data for the port F pins (PF_7 to PF_0).

PFDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port F Register (PORTF)

Bit	:	7	6	5	4	3	2	1	0
		PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PF_7 to PF_0.

PORTF is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port F pins (PF_7 to PF_0) must always be performed on PFDR.

If a port F read is performed while PFDDR bits are set to 1, the PFDR values are read. If a port F read is performed while PFDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTF contents are determined by the pin states, as PFDDR and PFDR are initialized. PORTF retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. For details, see section 5.6, Port 5.

Bit 6—BREQO Pin Select (BREQOPS): Seelects the $\overline{\text{BREQO}}$ output pin. Set the BREQOPS bit before setting the BREQOE bit in BCRL to 1.

Bit 6 BREQOPS	Description	
0	$\overline{\text{BREQO}}$ output pin PF_2	(Initial value)
1	$\overline{\text{BREQO}}$ output pin $P5_3$	

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{CS}_1$, $\overline{CS}_6$, and $\overline{CS}_7$ output. For details, see section 5.7, Port 6 and section 5.17, Port G.

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$, and $\overline{CS}_5$ output. For details, see section 5.7, Port 6 and section 5.17, Port G.

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. This bit is valid in modes 4 to 6.

Bit 3 ASOD	Description	
0	PF_6 is used as $\overline{\text{AS}}$ output pin	(Initial value)
1	PF_6 is designated as I/O port, and does not function as $\overline{\text{AS}}$ output pin	

Bits 2 to 0—Reserved

System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

SYSCR is an 8-bit readable/writable register that selects the interrupt control mode, controls the $\overline{\text{LWR}}$ pin, switches the $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input pins, and selects the detected edge for NMI. SYSCR is initialized to H'01 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select either of two interrupt control modes for the interrupt controller. For details, see section 3, Interrupt Controller, in the Hardware Manual.

Bit 3—NMI Edge Select (NMIEG): Selects the input edge for the NMI pin. For details, see section 3, Interrupt Controller, in the Hardware Manual.

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{\text{LWR}}$ output. This bit is valid in modes 4 to 6.

Bit 2 LWROD	Description	
0	PF_3 is designated as $\overline{\text{LWR}}$ output pin	(Initial value)
1	PF_3 is designated as I/O port, and does not function as $\overline{\text{LWR}}$ output pin	

Bit 1—IRQ Port Switching Select (IRQPAS): Selects switching of input pins for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$. For details, see section 5.6, Port 5.

Bit 0—RAM Enable (RAME): Enables or disables on-chip RAM. For details, see section 16, RAM, in the Hardware Manual.

5.16.3 Pin Functions

Port F pins also function as bus control signal input/output pins ($\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, $\overline{LWR}$, $\overline{LCAS}$, $\overline{BREQO}$, $\overline{BREQ}$, and $\overline{BACK}$) and the system clock (ø) output pin. The pin functions differ between modes 4 to 6, and mode 7. Port F pin functions are shown in table 5.31.

Table 5.31 Port F Pin Functions

Pin | **Selection Method and Pin Functions**

PF_7/ø

The pin function is switched as shown below according to bit PF7DDR.

PF7DDR	0	1
Pin function	PF_7 input pin	ø output pin

PF_6/$\overline{AS}$

The pin function is switched as shown below according to the operating mode, bit PF6DDR, and bit ASOD in PFCR2.

Operating Mode	Modes 4 to 6			Mode 7	
ASOD	0	1		—	
PF6DDR	—	0	1	0	1
Pin function	$\overline{AS}$ output pin	PF_6 input pin	PF_6 output pin	PF_6 input pin	PF_6 output pin

PF_5/$\overline{RD}$

The pin function is switched as shown below according to the operating mode and bit PF5DDR.

Operating Mode	Modes 4 to 6	Mode 7	
PF5DDR	—	0	1
Pin function	$\overline{RD}$ output pin	PF_5 input pin	PF_5 output pin

PF_4/$\overline{HWR}$

The pin function is switched as shown below according to the operating mode and bit PF4DDR.

Operating Mode	Modes 4 to 6	Mode 7	
PF4DDR	—	0	1
Pin function	$\overline{HWR}$ output pin	PF_4 input pin	PF_4 output pin

Pin	Selection Method and Pin Functions

$PF_3/\overline{LWR}$

The pin function is switched as shown below according to the operating mode, bit PF3DDR, and bit LWROD in SYSCR.

Operating Mode	Modes 4 to 6			Mode 7	
LWROD	0	1		—	
PF3DDR	—	0	1	0	1
Pin function	$\overline{LWR}$ output pin	PF_3 input pin	PF_3 output pin	PF_3 input pin	PF_3 output pin

$PF_2/\overline{LCAS}/\overline{BREQO}$

The pin function is switched as shown below according to the combination of the operating mode, and bits RMTS2 to RMTS0, BREQOE, ABW5 to ABW2, BREQOPS, and PF2DDR.

Operating Mode	Modes 4 to 6				Mode 7	
[DRAM space setting] · [16-bit access setting]	0			1	—	
[BREQOE · $\overline{BREQOPS}$]	0		1	—	—	
PF2DDR	0	1	—	—	0	1
Pin function	PF_2 input pin	PF_2 output pin	$\overline{BREQO}$ output pin	$\overline{LCAS}$ output pin	PF_2 input pin	PF_2 output pin

$PF_1/\overline{BACK}$

The pin function is switched as shown below according to the combination of the operating mode, and bits BRLE and PF1DDR.

Operating Mode	Modes 4 to 6			Mode 7	
BRLE	0		1	—	
PF1DDR	0	1	—	0	1
Pin function	PF_1 input pin	PF_1 output pin	$\overline{BACK}$ output pin	PF_1 input pin	PF_1 output pin

Pin	Selection Method and Pin Functions
$PF_0/\overline{BREQ}$	The pin function is switched as shown below according to the combination of the operating mode, and bits BRLE and PF0DDR.

Operating Mode	Modes 4 to 6			Mode 7	
BRLE	0		1	—	
PF0DDR	0	1	—	0	1
Pin function	PF_0 input pin	PF_0 output pin	$\overline{BREQ}$ input pin	PF_0 input pin	PF_0 output pin

5.17 Port G

5.17.1 Overview

Port G is a 5-bit I/O port. Port G pins also function as bus control signal output pins ($\overline{CS0}$ to $\overline{CS3}$, and $\overline{CAS}$). Enabling or disabling of $\overline{CS}_1$ to $\overline{CS}_2$ output can be changed by a setting in PFCR2.

Figure 5.26 shows the port G pin configuration.

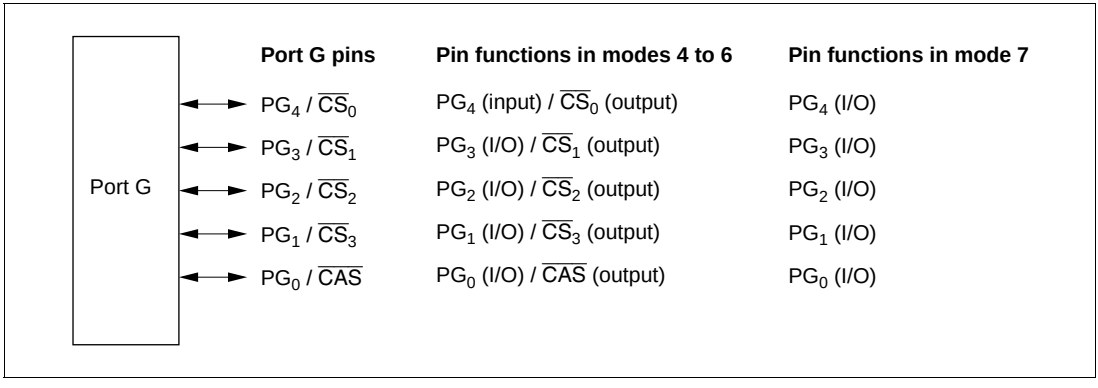


Figure 5.26 Port G Pin Functions

5.17.2 Register Configuration

Table 5.32 shows the port G register configuration.

Table 5.32 Port G Registers

Name	Abbreviation	R/W	Initial Value*2	Address*1
Port G data direction register	PGDDR	W	H'10/H'00*3	H'FEBF
Port G data register	PGDR	R/W	H'00	H'FF6F
Port G register	PORTG	R	Undefined	H'FF5F
Port function control register 2	PFCR2	R/W	H'30	H'FFAC

Notes: 1. Lower 16 bits of the address.
2. Value of bits 4 to 0.
3. Initial value depends on the mode.

Port G Data Direction Register (PGDDR)

Bit :	7	6	5	4	3	2	1	0
	—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 4 and 5								
Initial value :	Undefined	Undefined	Undefined	1	0	0	0	0
R/W :	—	—	—	W	W	W	W	W
Modes 6 and 7								
Initial value :	Undefined	Undefined	Undefined	0	0	0	0	0
R/W :	—	—	—	W	W	W	W	W

PGDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port G. PGDDR cannot be read, and bits 7 to 5 are reserved. If PGDDR is read, an undefined value will be read.

The PG4DDR bit is initialized by a reset, and in hardware standby mode, to 1 in modes 4 and 5, and to 0 in modes 6 and 7. PGDDR retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

Port G Data Register (PGDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
R/W	:	—	—	—	R/W	R/W	R/W	R/W	R/W

PGDR is an 8-bit readable/writable register that stores output data for the port G pins (PG_4 to PG_0).

Bits 7 to 5 are reserved; they return an undefined value if read, and cannot be modified.

PGDR is initialized to H'00 (bits 4 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port G Register (PORTG)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4	PG3	PG2	PG1	PG0
Initial value	:	Undefined	Undefined	Undefined	—*	—*	—*	—*	—*
R/W	:	—	—	—	R	R	R	R	R

Note: * Determined by state of pins PG_4 to PG_0.

PORTG is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port G pins (PG_4 to PG_0) must always be performed on PGDR.

Bits 7 to 5 are reserved; they return an undefined value if read, and cannot be modified.

If a port G read is performed while PGDDR bits are set to 1, the PGDR values are read. If a port G read is performed while PGDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTG contents are determined by the pin states, as PGDDR and PGDR are initialized. PORTG retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. For details, see section 5.6, Port 5.

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. For details, see section 5.6, Port 5.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output. Change the CS167E setting only when the DDR bits are cleared to 0.

Bit 5 CS167E	Description
0	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output disabled (can be used as I/O ports)
1	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output enabled (Initial value)

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output. Change the CS25E setting only when the DDR bits are cleared to 0.

Bit 4 CS25E	Description
0	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output disabled (can be used as I/O ports)
1	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output enabled (Initial value)

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 5.16, Port F.

Bits 2 to 0—Reserved

5.17.3 Pin Functions

Port G pins also function as bus control signal output pins ($\overline{CS0}$ to $\overline{CS3}$, and $\overline{CAS}$). The pin functions are different in mode 7, and modes 4 to 6. Port G pin functions are shown in table 5.33.

Table 5.33 Port G Pin Functions

Pin — **Selection Method and Pin Functions**

$PG_4/\overline{CS}_0$

The pin function is switched as shown below according to the operating mode and bit PG4DDR.

Operating Mode	Modes 4 to 6		Mode 7	
PG4DDR	0	1	0	1
Pin function	PG_4 input pin	$\overline{CS}_0$ output pin	PG_4 input pin	PG_4 output pin

$PG_3/\overline{CS}_1$

The pin function is switched as shown below according to the operating mode and bits PG3DDR and CS167E.

Operating Mode	Modes 4 to 6				Mode 7	
CS167E	0		1		0	1
PG3DDR	0	1	0	1	—	—
Pin function	PG_3 input pin	PG_3 output pin	PG_3 input pin	$\overline{CS}_1$ output pin	PG_3 input pin	PG_3 output pin

$PG_2/\overline{CS}_2$

The pin function is switched as shown below according to the operating mode and bits PG2DDR and CS25E.

Operating Mode	Modes 4 to 6				Mode 7	
CS25E	0		1		0	1
PG2DDR	0	1	0	1	—	—
Pin function	PG_2 input pin	PG_2 output pin	PG_2 input pin	$\overline{CS}_2$ output pin	PG_2 input pin	PG_2 output pin

Pin	Selection Method and Pin Functions

$PG_1/\overline{CS_3}$

The pin function is switched as shown below according to the operating mode and bits PG1DDR and CS25E.

Operating Mode	Modes 4 to 6				Mode 7	
CS25E	0		1		0	1
PG1DDR	0	1	0	1	—	—
Pin function	PG_1 input pin	PG_1 output pin	PG_1 input pin	$\overline{CS_3}$ output pin	PG_1 input pin	PG_1 output pin

$PG_0/\overline{CAS}$

The pin function is switched as shown below according to the combination of the operating mode and bits RMTS2 to RMTS0 and PG0DDR.

Operating Mode	Modes 4 to 6			Mode 7	
RMTS2 to RMTS0	B'000, B'100 to B'111		B'001 to B'011	—	
PG0DDR	0	1	—	0	1
Pin function	PG_0 input pin	PG_0 output pin	$\overline{CAS}$ output pin	PG_0 input pin	PG_0 output pin

5.18 Pin States

5.18.1 Port States in Each Mode

Table 5.34 I/O Port States in Each Processing State

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
Port 1	4 to 7	T	T	kept	kept	I/O port
Port 2	4 to 7	T	T	kept	kept	I/O port
Port 3	4 to 7	T	T	kept	kept	I/O port
$P4_7/DA_1$	4 to 7	T	T	[DAOE1 = 1] kept [DAOE1 = 0] T	kept	I/O port
$P4_6/DA_0$	4 to 7	T	T	[DAOE0 = 1] kept [DAOE0 = 0] T	kept	I/O port
$P4_5$ to $P4_0$	4 to 7	T	T	T	T	Input port
$P5_7$ to DA_3	4 to 7	T	T	[DAOE3 = 1] kept [DAOE3 = 0] T	kept	I/O port
$P5_6$ to DA_2	4 to 7	T	T	[DAOE2 = 1] kept [DAOE2 = 0] T	kept	I/O port
$P5_5$, $P5_4$	4 to 7	T	T	T	T	Input port
$P5_3/\overline{WAIT}/\overline{BREQO}$	4 to 6	T	T	[BREQOE · BREQOPS + WAITE · WAITPS = 0] kept [BREQOE · BREQOPS = 1] kept [BREQOE · BREQOPS = 0] and [WAITE · WAITPS · $\overline{DDR}$ = 1] T	[BREQOE · BREQOPS + WAITE · WAITPS = 0] kept [BREQOE · BREQOPS = 1] $\overline{BREQO}$ [BREQOE · BREQOPS = 0] and [WAITE · WAITPS · $\overline{DDR}$ = 1] T	[BREQOE · BREQOPS + WAITE · WAITPS = 0] I/O port [BREQOE · BREQOPS = 1] $\overline{BREQO}$ [BREQOE · BREQOPS = 0] and [WAITE · WAITPS · $\overline{DDR}$ = 1] $\overline{WAIT}$
	7	T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
$P5_2$ to $P5_0$	4 to 7	T	T	kept	kept	I/O port
$P6_7/\overline{CS_7}$	4 to 6	T	T	[CS167E = 0], [CS167E · $\overline{DDR}$ = 1] kept [CS167E · DDR · $\overline{OPE}$ = 1] T [CS167E · DDR · OPE = 1] H	[CS167E = 0] kept [CS167E · $\overline{DDR}$ = 1] kept [CS167E · DDR = 1] T	[CS167E = 0] I/O port [CS167E · $\overline{DDR}$ = 1] Input port [CS167E · DDR = 1] $\overline{CS_7}$ to $\overline{CS_6}$
$P6_6/\overline{CS_6}$	7	T	T	kept	kept	I/O port
$P6_5$ to $P6_2$	4 to 7	T	T	kept	kept	I/O port
$P6_1/\overline{CS_5}$	4 to 6	T	T	[CS25E · DDR · $\overline{OPE}$ = 1] T [CS25E · DDR · OPE = 1] H [CS25E = 0], [CS25E · $\overline{DDR}$ = 1] kept	[CS25E = 0] kept [CS25E · $\overline{DDR}$ = 1] kept [CS25E · DDR = 1] T	[CS25E = 0] I/O port [CS25E · $\overline{DDR}$ = 1] Input port [CS25E · DDR = 1] $\overline{CS_5}$ to $\overline{CS_4}$
$P6_0/\overline{CS_4}$	7	T	T	kept	kept	I/O port
Port 7	4 to 7	T	T	kept	kept	I/O port
$P8_6/\overline{WAIT}$	4 to 6	T	T	[WAITE · $\overline{WAITPS}$ · $\overline{DDR}$ = 1] T [WAITE · $\overline{WAITPS}$ = 0] kept	[WAITE · $\overline{WAITPS}$ · $\overline{DDR}$ = 1] T [WAITE · $\overline{WAITPS}$ = 0] kept	[WAITE · $\overline{WAITPS}$ · $\overline{DDR}$ = 1] $\overline{WAIT}$ [WAITE · $\overline{WAITPS}$ = 0] I/O port
	7	T	T	kept	kept	I/O port
$P8_5$ to $P8_0$	4 to 7	T	T	kept	kept	I/O port
Port 9	4 to 7	T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PA_7/A_{23} PA_6/A_{22} PA_5/A_{21}	4, 5, 6	T	T	[AnE = 0] kept [AnE · $\overline{DDR}$ = 1] T [AnE · DDR · $\overline{OPE}$ = 1] T [AnE · DDR · OPE = 1] kept	[AnE = 0] kept [AnE · $\overline{DDR}$ = 1] T [AnE · DDR = 1] T	[AnE = 0] I/O port [AnE · $\overline{DDR}$ = 1] Input port [AnE · DDR = 1] Address output
	7	T	T	kept	kept	I/O port
PA_4/A_{20}	4, 5	L	T	[$\overline{A20E}$ · DDR = 1] kept [A20E · $\overline{OPE}$ = 1] T [A20E · OPE = 1] kept	[$\overline{A20E}$ · DDR = 1] kept [A20E+$\overline{A20E}$ · $\overline{DDR}$ = 1] T	[$\overline{A20E}$ · DDR = 1] Output port [A20E+$\overline{A20E}$ · $\overline{DDR}$ = 1] Address output
	6	T	T	[A20E = 0], [A20E · $\overline{DDR}$ = 1] kept [A20E · DDR · $\overline{OPE}$ = 1] T [A20E · DDR · OPE = 1] kept	[A20E = 0], [A20E · $\overline{DDR}$ = 1] kept [A20E · DDR = 1] T	[A20E = 0] I/O port [A20E · $\overline{DDR}$ = 1] Input port [A20E · DDR = 1] Address output
	7	T	T	kept	kept	I/O port
PA_3/A_{19} PA_2/A_{18} PA_1/A_{17} PA_0/A_{16}	4, 5	L	T	[OPE = 0] T [OPE = 1] kept	T	Address output
	6	T	T	[DDR · OPE = 0] T [DDR · OPE = 1] kept	T	[DDR = 0] Input port [DDR = 1] Address output
	7	T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
Port B	4, 5	L	T	[OPE = 0] T [OPE = 1] kept	T	Address output
	6	T	T	[DDR · OPE = 0] T [DDR · OPE = 1] kept	T	[DDR = 0] Input port [DDR = 1] Address output
	7	T	T	kept	kept	I/O port
Port C	4, 5	L	T	[OPE = 0] T [OPE = 1] kept	T	Address output
	6	T	T	[DDR · OPE = 0] T [DDR · OPE = 1] kept	T	[DDR = 0] Input port [DDR = 1] Address output
	7	T	T	kept	kept	I/O port
Port D	4 to 6	T	T	T	T	Data bus
	7	T	T	kept	kept	I/O port
Port E	4 to 6 8-bit bus	T	T	kept	kept	I/O port
	16-bit bus	T	T	T	T	Data bus
	7		T	kept	kept	I/O port
PF_7 /ø	4 to 6	Clock output	T	[DDR = 0] Input port [DDR = 1] H	[DDR = 0] Input port [DDR = 1] Clock output	[DDR = 0] Input port [DDR = 1] Clock output
	7	T	T	[DDR = 0] Input port [DDR = 1] H	[DDR = 0] Input port [DDR = 1] Clock output	[DDR = 0] Input port [DDR = 1] Clock output

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PF_6/$\overline{AS}$	4 to 6	H	T	[ASOD = 1] kept	[ASOD = 1] kept	[ASOD = 1] I/O port
				[$\overline{ASOD}$ · $\overline{OPE}$ = 1] T	[ASOD = 0] T	[ASOD = 0] $\overline{AS}$
				[$\overline{ASOD}$ · OPE = 1] H		
	7	T	T	kept	kept	I/O port
PF_5/$\overline{RD}$ PF_4/$\overline{HWR}$	4 to 6	H	T	[OPE = 0] T	T	$\overline{RD}$, $\overline{HWR}$
				[OPE = 1] H		
	7	T	T	kept	kept	I/O port
PF_3/$\overline{LWR}$	4 to 6	H	T	[LWROD = 1] kept	[LWROD = 1] kept	[LWROD = 1] I/O port
				[$\overline{LWROD}$ · $\overline{OPE}$ = 1] T	[LWROD = 0] T	[LWROD = 0] $\overline{LWR}$
				[$\overline{LWROD}$ · OPE = 1] H		
	7	T	T	kept	kept	I/O port
PF_2/$\overline{LCAS}$/ $\overline{BREQO}$	4 to 6	T	T	[BREQOE · $\overline{BREQOPS}$ + LCASE = 0] kept	[BREQOE · $\overline{BREQOPS}$ + LCASE = 0] kept	[BREQOE · $\overline{BREQOPS}$ + LCASE = 0] I/O port
				[BREQOE · $\overline{BREQOPS}$ = 1] kept	[BREQOE · $\overline{BREQOPS}$ = 1] $\overline{BREQO}$	[BREQOE · $\overline{BREQOPS}$ = 1] $\overline{BREQO}$
				[LCASE = 1, OPE = 0] T	[LCASE = 1] T	[LCASE = 1] $\overline{LCAS}$
				[LCASE = 1, OPE = 1] H		
	7	T	T	kept	kept	I/O port
PF_1/$\overline{BACK}$	4 to 6	T	T	[BRLE=0] kept	L	[BRLE = 0] I/O port
				[BRLE=1] $\overline{BACK}$		[BRLE = 1] $\overline{BACK}$
	7	T	T	kept	kept	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
$PF_0/\overline{BREQ}$	4 to 6	T	T	[BRLE=0] kept	T	[BRLE = 0] I/O port
				[BRLE=1] T		[BRLE = 1] $\overline{BREQ}$
	7	T	T	kept	kept	I/O port
$PG_4/\overline{CS_0}$	4, 5	H	T	[DDR · OPE = 0] T	T	[DDR = 0] Input port
	6	T		[DDR · OPE = 1] H		[DDR = 1] $\overline{CS_0}$
	7	T	T	kept	kept	I/O port
$PG_3/\overline{CS_1}$	4 to 6	T	T	[CS167E = 0] kept	[CS167E = 0] kept	[CS167E = 0] I/O port
				[CS167E · $\overline{DDR}$ = 1] T	[CS167E = 1] T	[CS167E · $\overline{DDR}$ = 1] Input port
				[CS167E · DDR · $\overline{OPE}$ = 1] T		[CS167E · DDR = 1] $\overline{CS_1}$
				[CS167E · DDR · OPE = 1] H		
	7	T	T	kept	kept	I/O port
$PG_2/\overline{CS_2}$ $PG_1/\overline{CS_3}$	4 to 6	T	T	[CS25E = 0] kept	[CS25E = 0] kept	[CS25E = 0] I/O port
				[CS25E · $\overline{DDR}$ = 1] T	[CS25E = 1] T	[CS25E · $\overline{DDR}$ = 1] Input port
				[CS25E · DDR · $\overline{OPE}$ = 1] T		[CS25E · DDR = 1] $\overline{CS_2}$ to $\overline{CS_3}$
				[CS25E · DDR · OPE = 1] H		
	7	T	T	kept	kept	I/O port
$\overline{PG}0/\overline{CAS}$	4 to 6	T	T	[DRAME = 0] kept	T	[DRAME = 0] Input port
				[DRAME · $\overline{OPE}$ = 1] T		[DRAME = 1] $\overline{CAS}$
				[DRAME · OPE = 1] $\overline{CAS}$		
	7	T	T	kept	kept	I/O port

Legend

H:	High level
L:	Low level
T:	High impedance
kept:	Input port becomes high-impedance, output port retains state
DDR:	Data direction register
OPE:	Output port enable
WAITE:	Wait input enable
BRLE:	Bus release enable
BREQOE:	BREQO pin enable
DRAME:	DRAM space setting
LCASE:	DRAM space setting, 16-bit bus mode setting
AnE:	Address n enable (n = 23 to 21)
A20E:	Address 20 enable
BREQOPS:	BREQO pin select
ASOD:	AS output disable
WAITPS:	WAIT pin select
CS167E:	CS167 enable
CS25E:	CS25 enable
LWROD:	LWR output disable

5.19 I/O Port Block Diagrams

5.19.1 Port 1

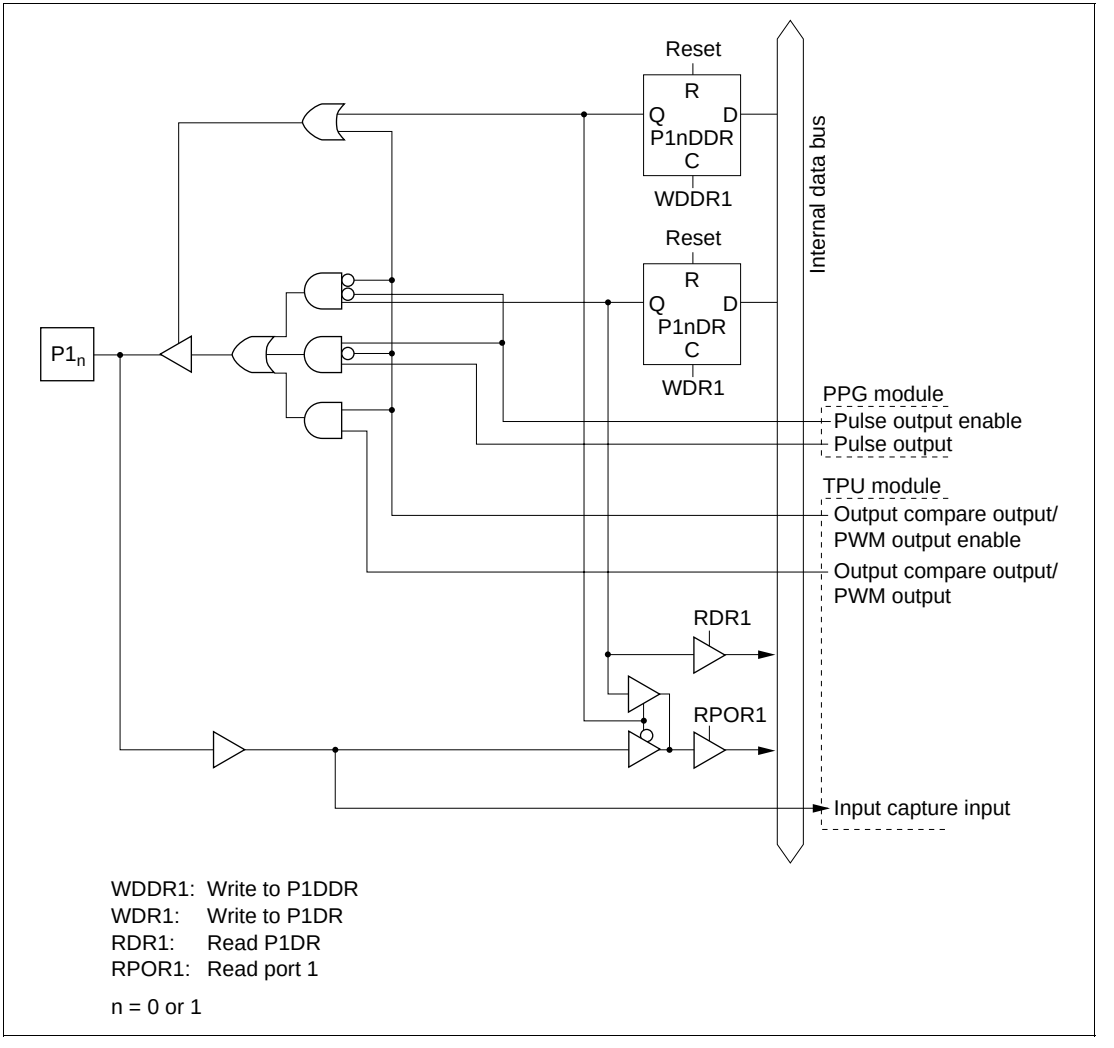


Figure 5.27 (a) Port 1 Block Diagram (Pins $P1_0$ and $P1_1$)

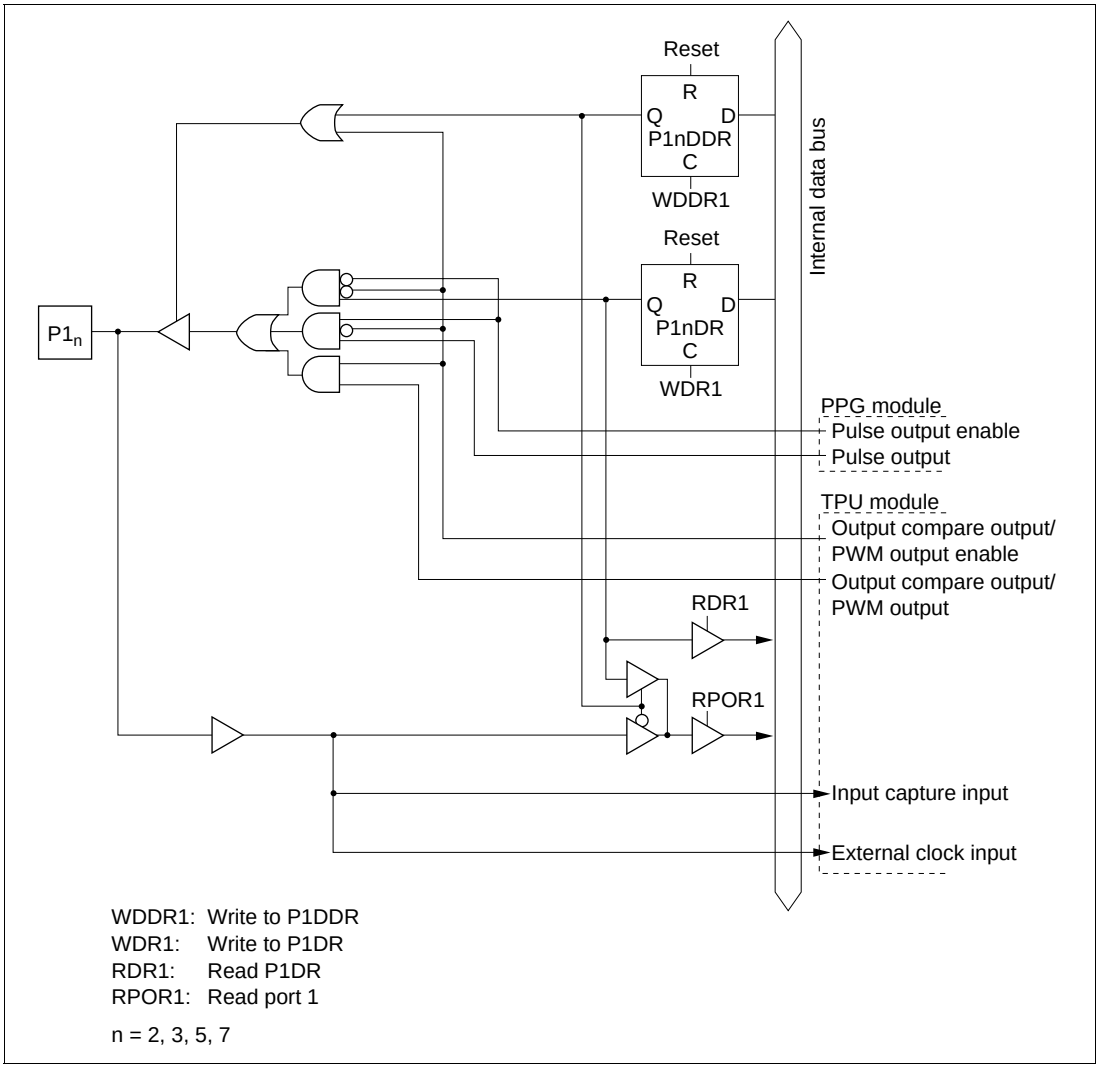


Figure 5.27 (b) Port 1 Block Diagram (Pins $P1_2$, $P1_3$, $P1_5$, and $P1_7$)

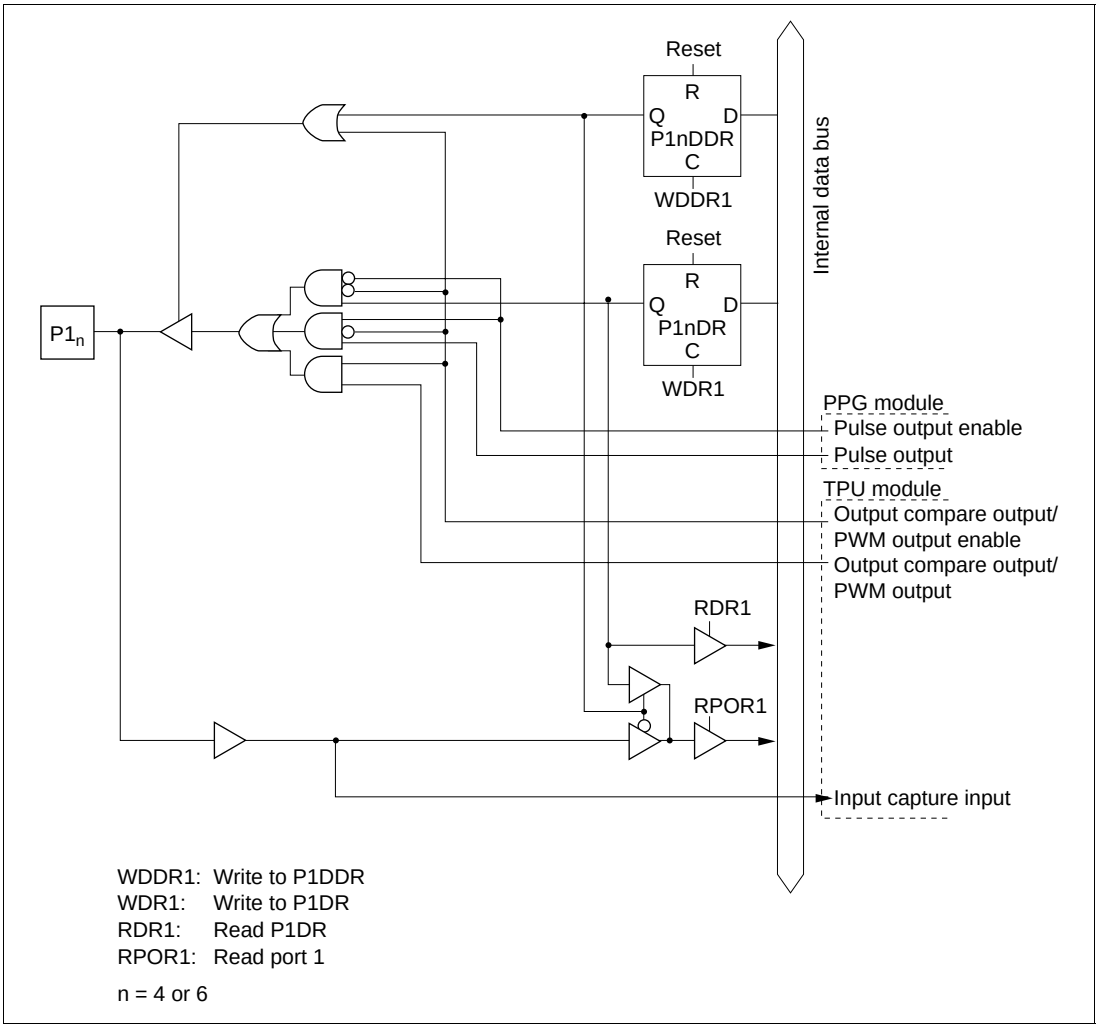


Figure 5.27 (c) Port 1 Block Diagram (Pins $P1_4$ and $P1_6$)

5.19.2 Port 2

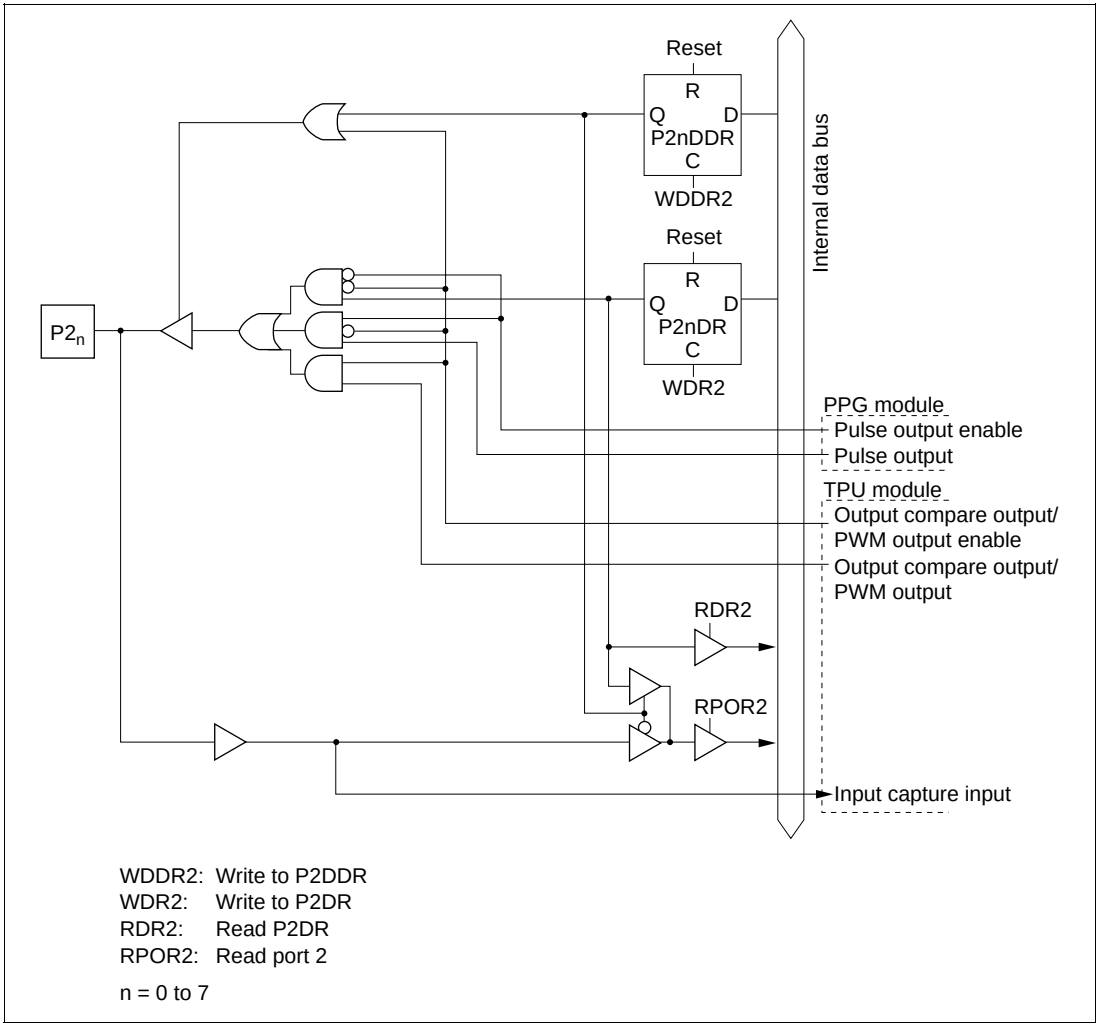
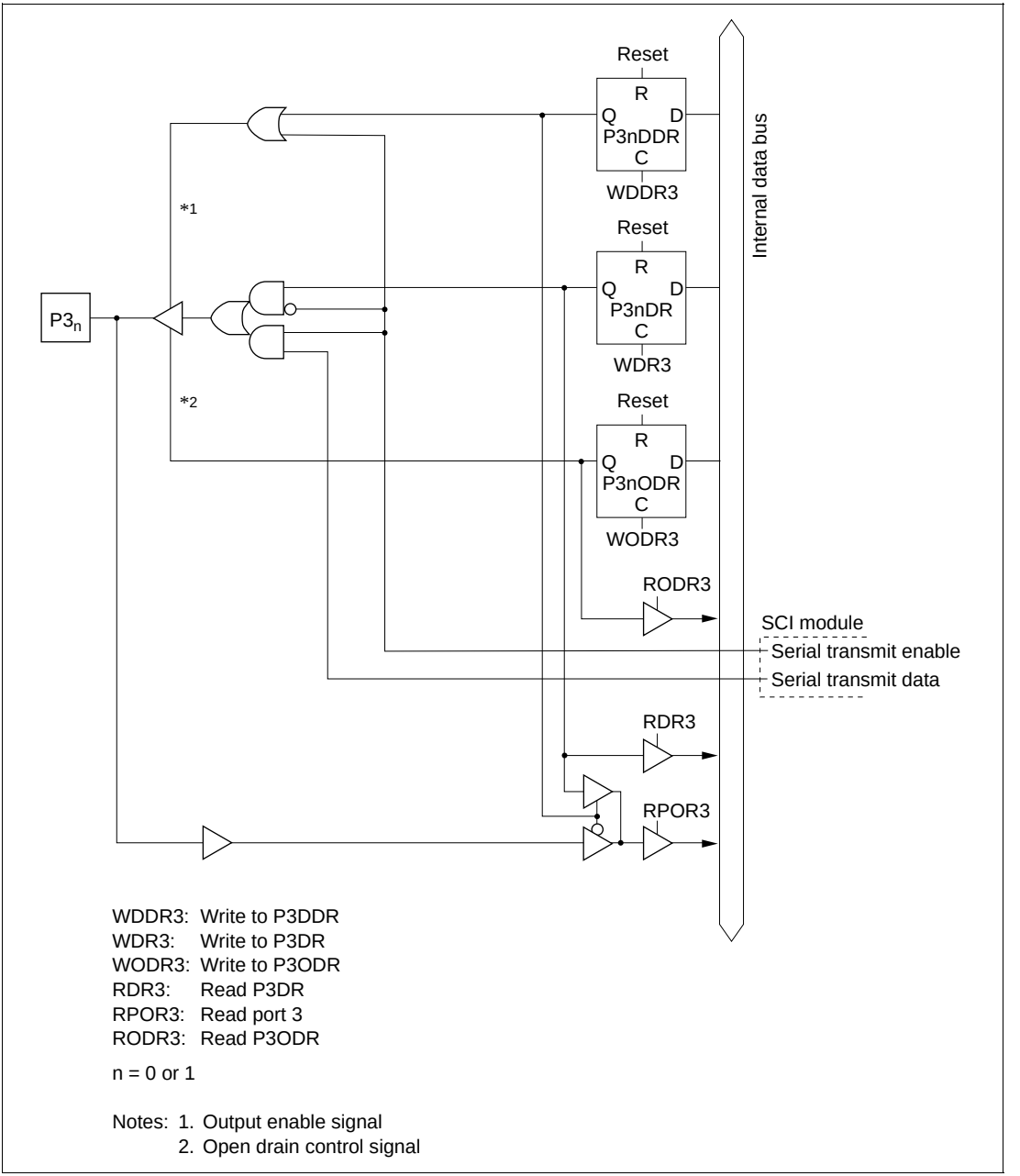


Figure 5.28 Port 2 Block Diagram (Pins $P2_n$)

5.19.3 Port 3

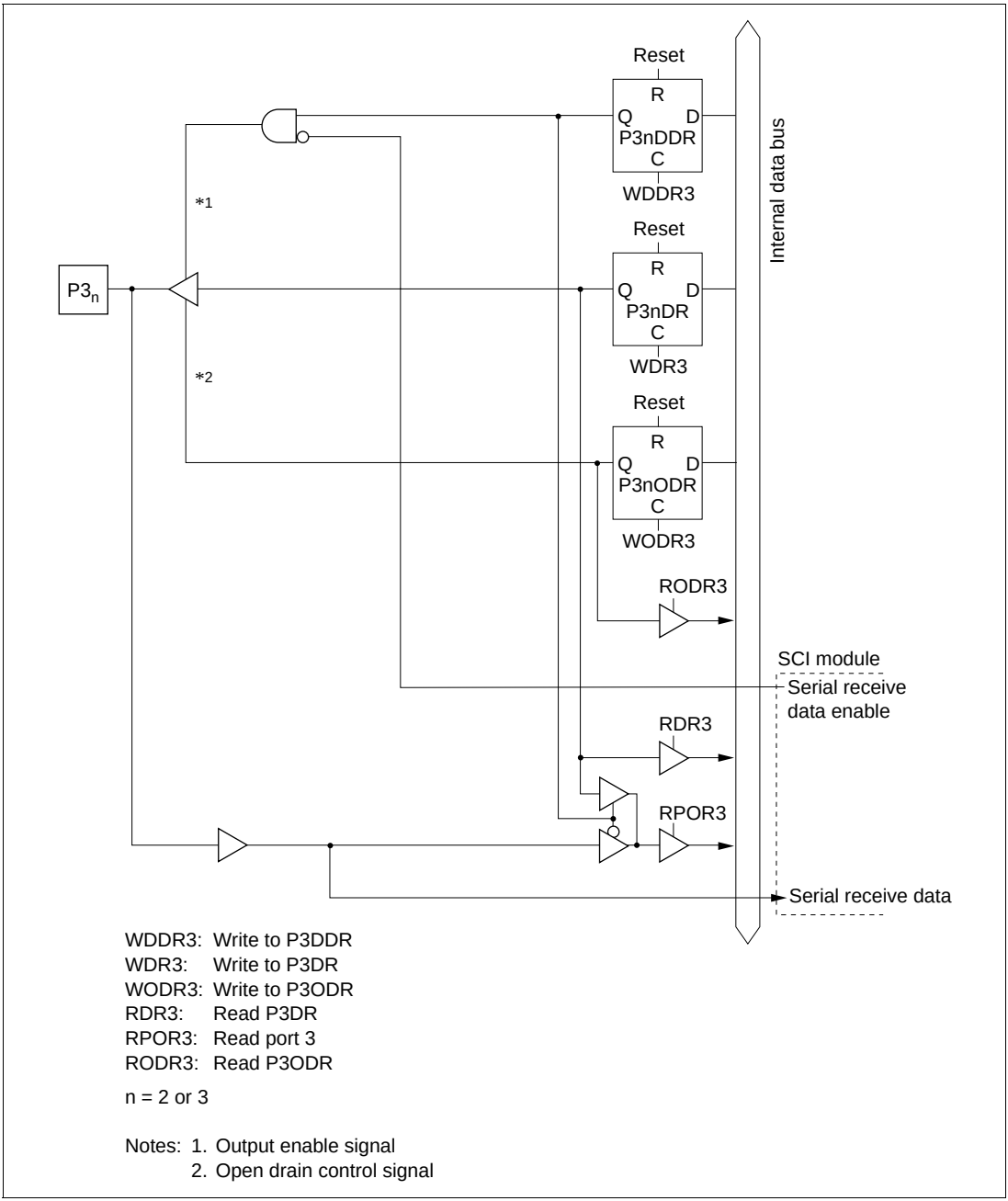


WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RDR3: Read P3DR
RPOR3: Read port 3
RODR3: Read P3ODR

n = 0 or 1

Notes: 1. Output enable signal
2. Open drain control signal

Figure 5.29 (a) Port 3 Block Diagram (Pins $P3_0$ and $P3_1$)

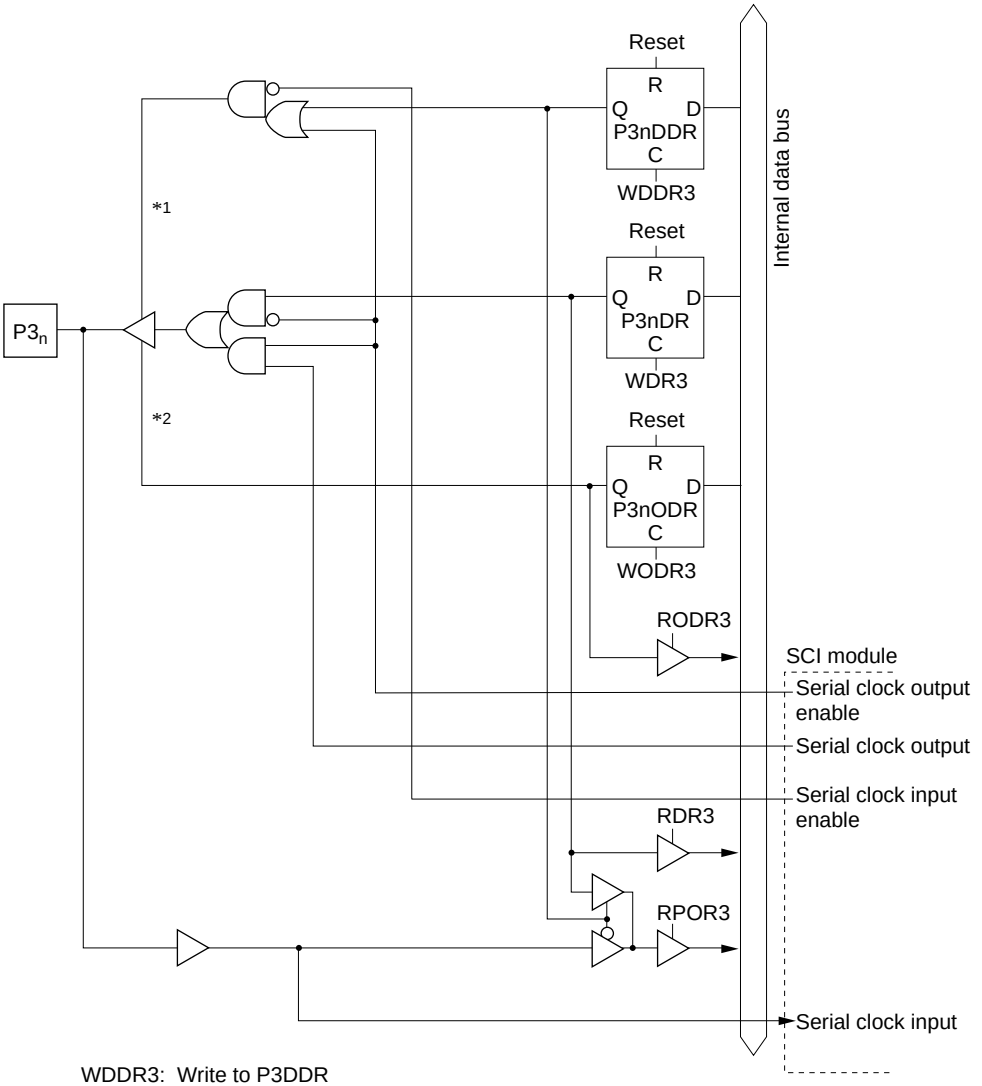


WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RDR3: Read P3DR
RPOR3: Read port 3
RODR3: Read P3ODR

n = 2 or 3

Notes: 1. Output enable signal
2. Open drain control signal

Figure 5.29 (b) Port 3 Block Diagram (Pins $P3_2$ and $P3_3$)



WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RDR3: Read P3DR
RPOR3: Read port 3
RODR3: Read P3ODR

n = 4 or 5

Notes: 1. Output enable signal
2. Open drain control signal

Figure 5.29 (c) Port 3 Block Diagram (Pins $P3_4$ and $P3_5$)

5.19.4 Port 4

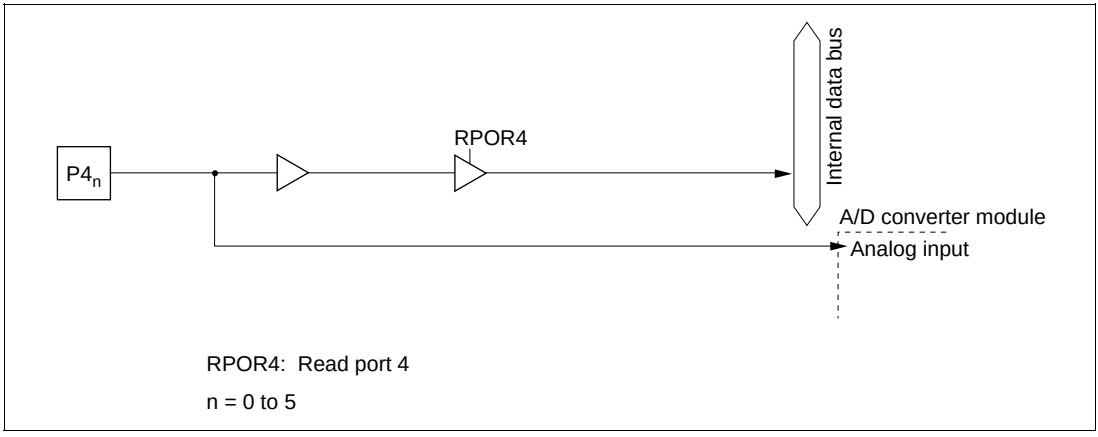


Figure 5.30 (a) Port 4 Block Diagram (Pins $P4_0$ to $P4_5$)

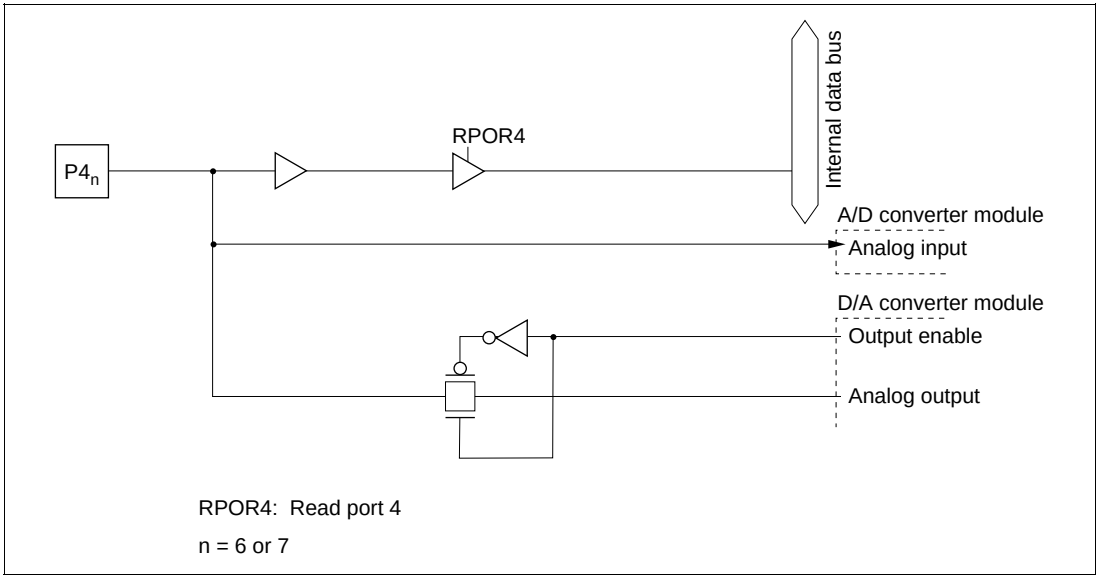


Figure 5.30 (b) Port 4 Block Diagram (Pins $P4_6$ and $P4_7$)

5.19.5 Port 5

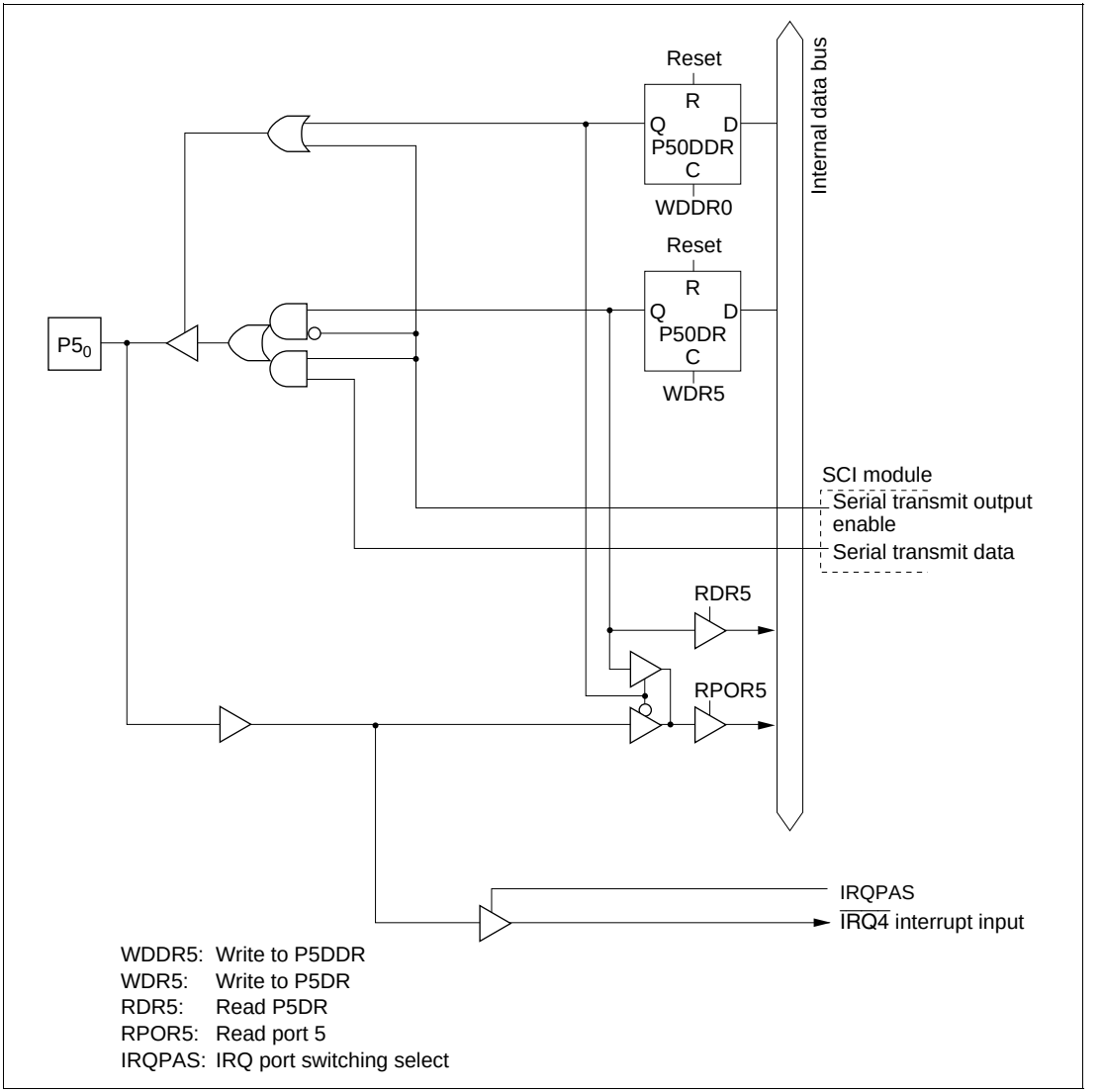


Figure 5.31 (a) Port 5 Block Diagram (Pin $P5_0$)

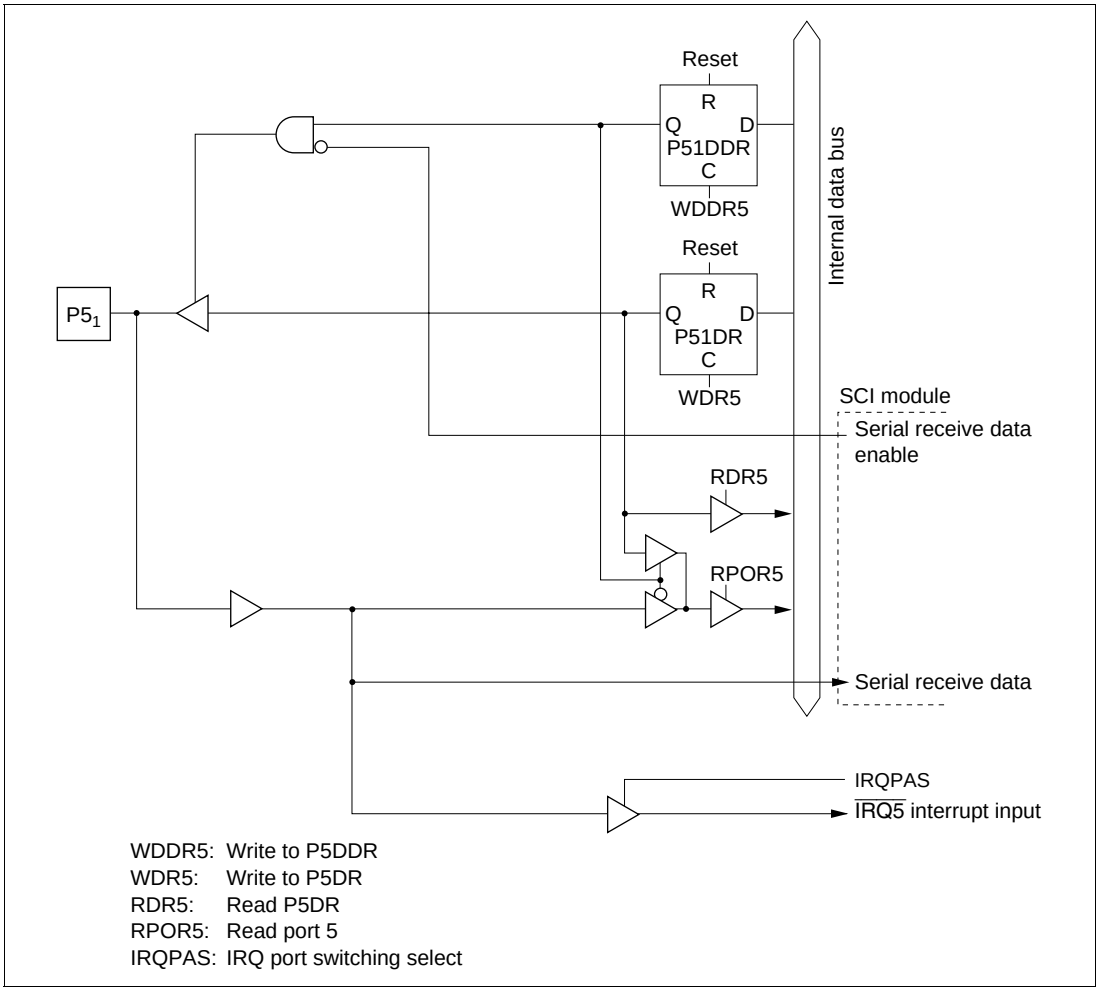


Figure 5.31 (b) Port 5 Block Diagram (Pin P5$_1$)

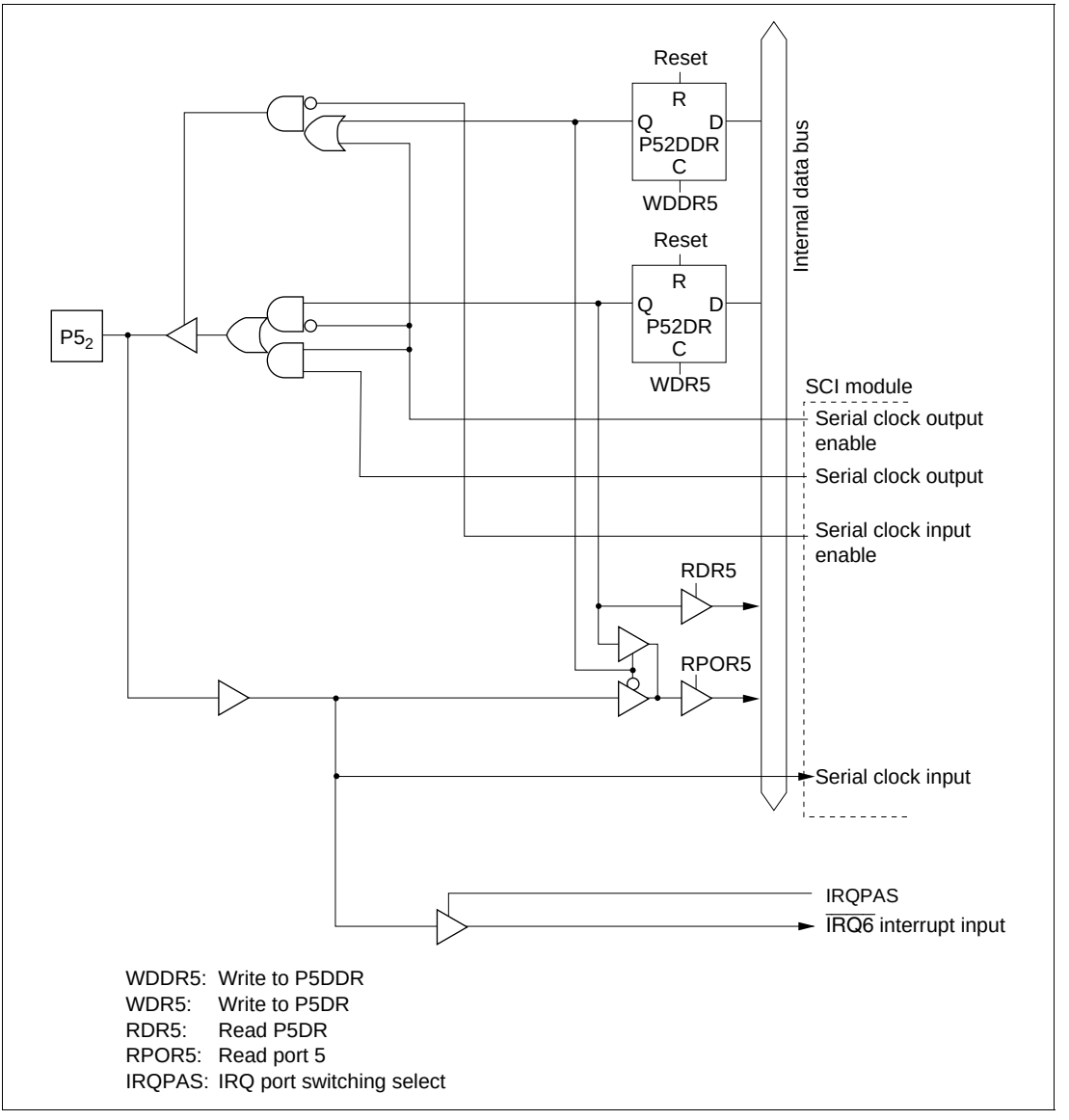


Figure 5.31 (c) Port 5 Block Diagram (Pin P5$_2$)

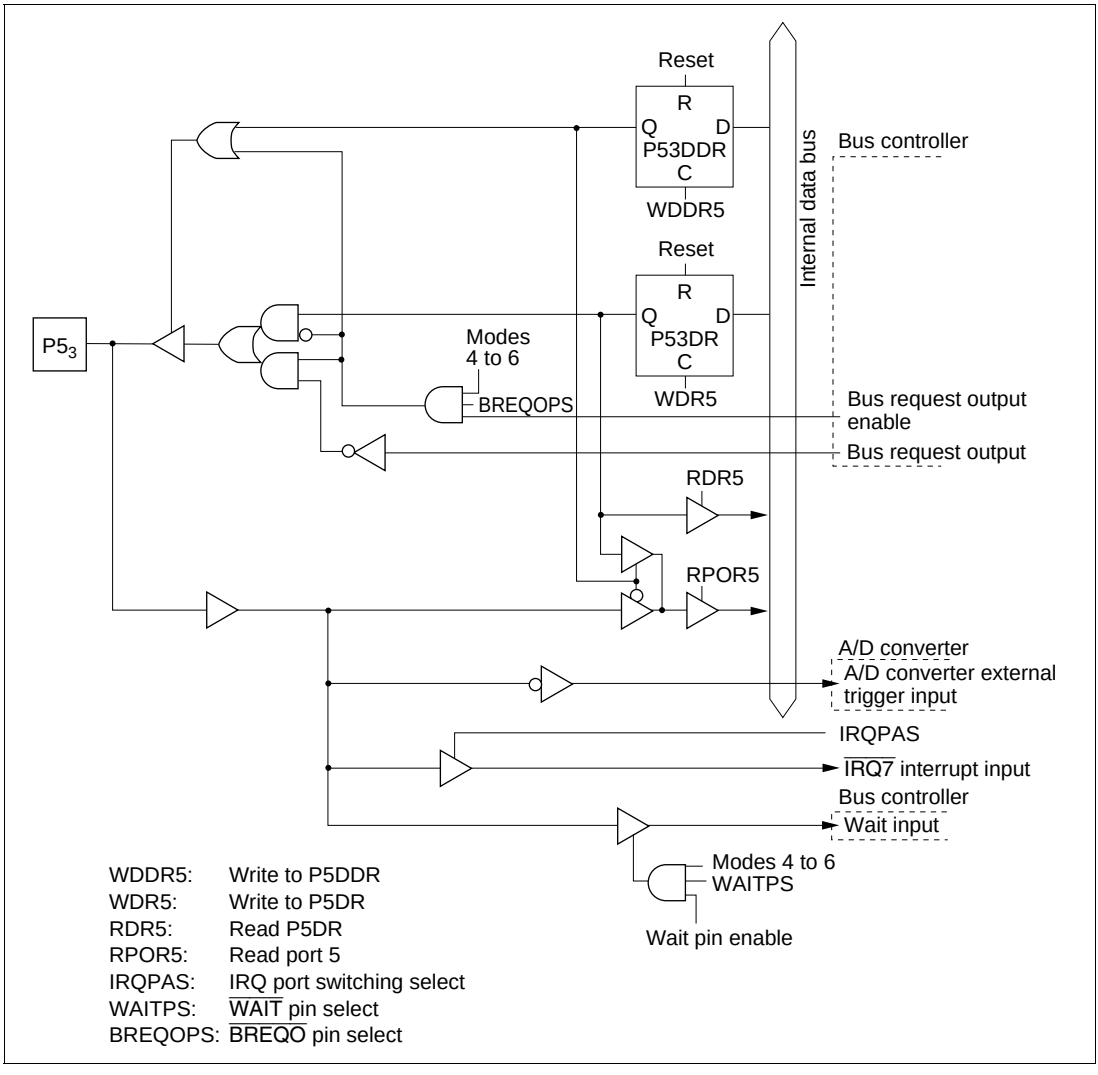


Figure 5.31 (d) Port 5 Block Diagram (Pin P5$_3$)

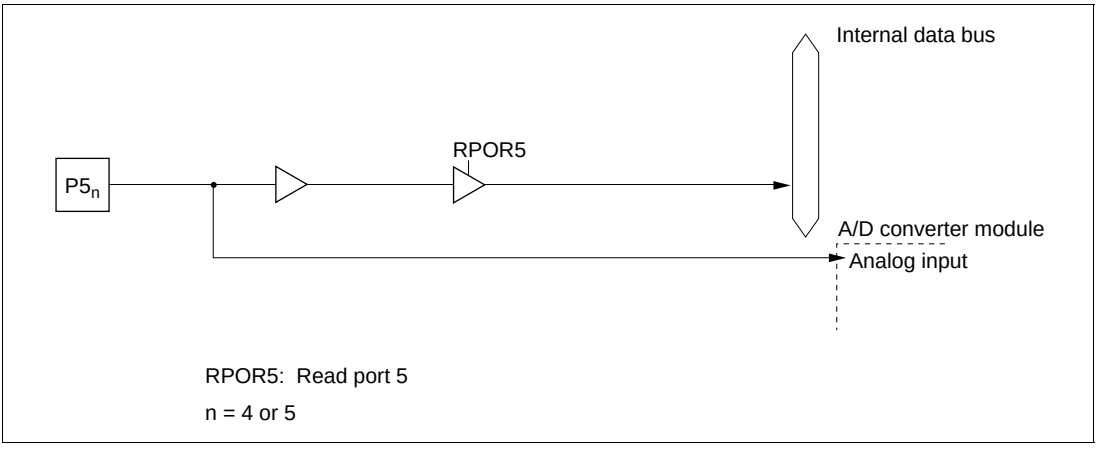


Figure 5.31 (e) Port 5 Block Diagram (Pins $P5_4$ and P_5)

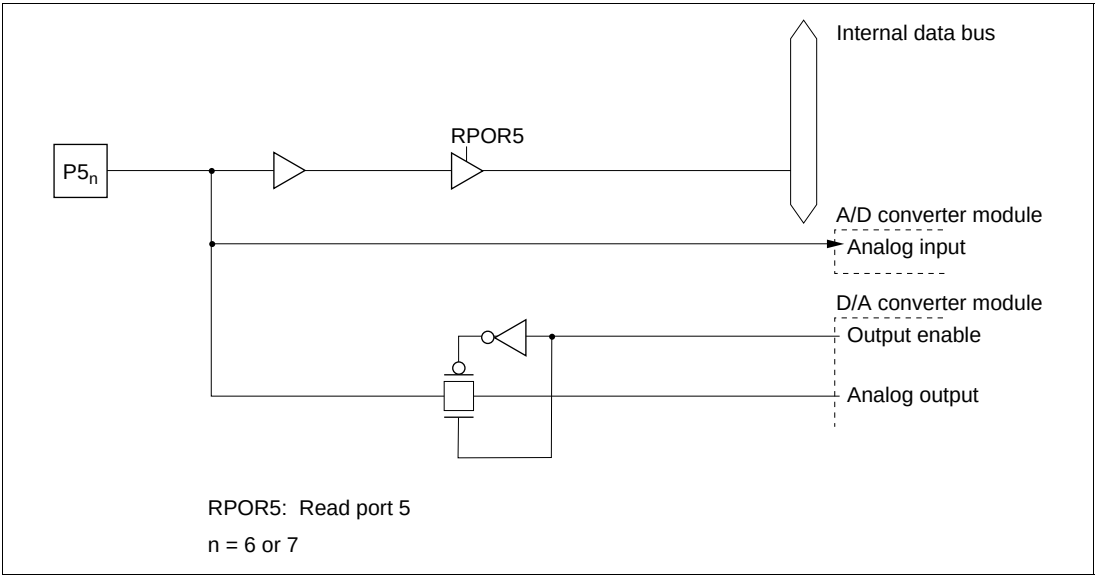


Figure 5.31 (f) Port 5 Block Diagram (Pins $P5_6$ and P_7)

5.19.6 Port 6

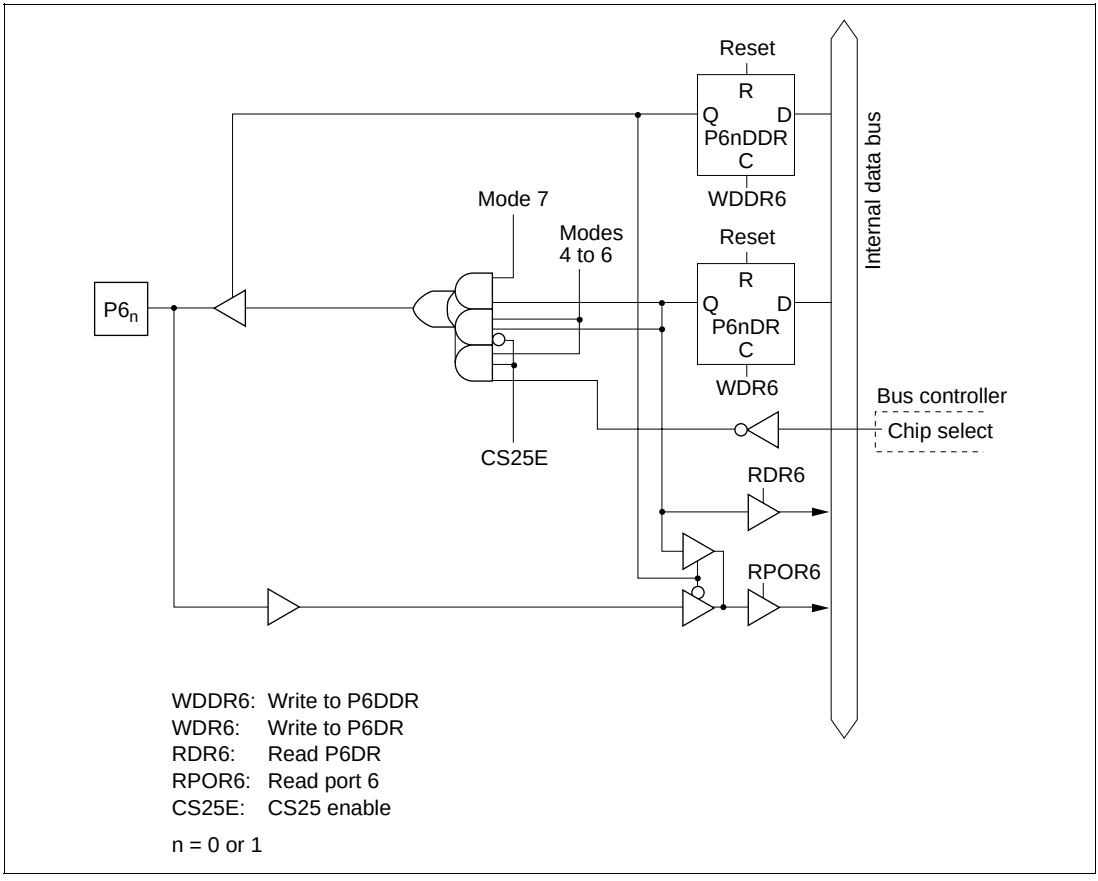


Figure 5.32 (a) Port 6 Block Diagram (Pins $P6_0$ and $P6_1$)

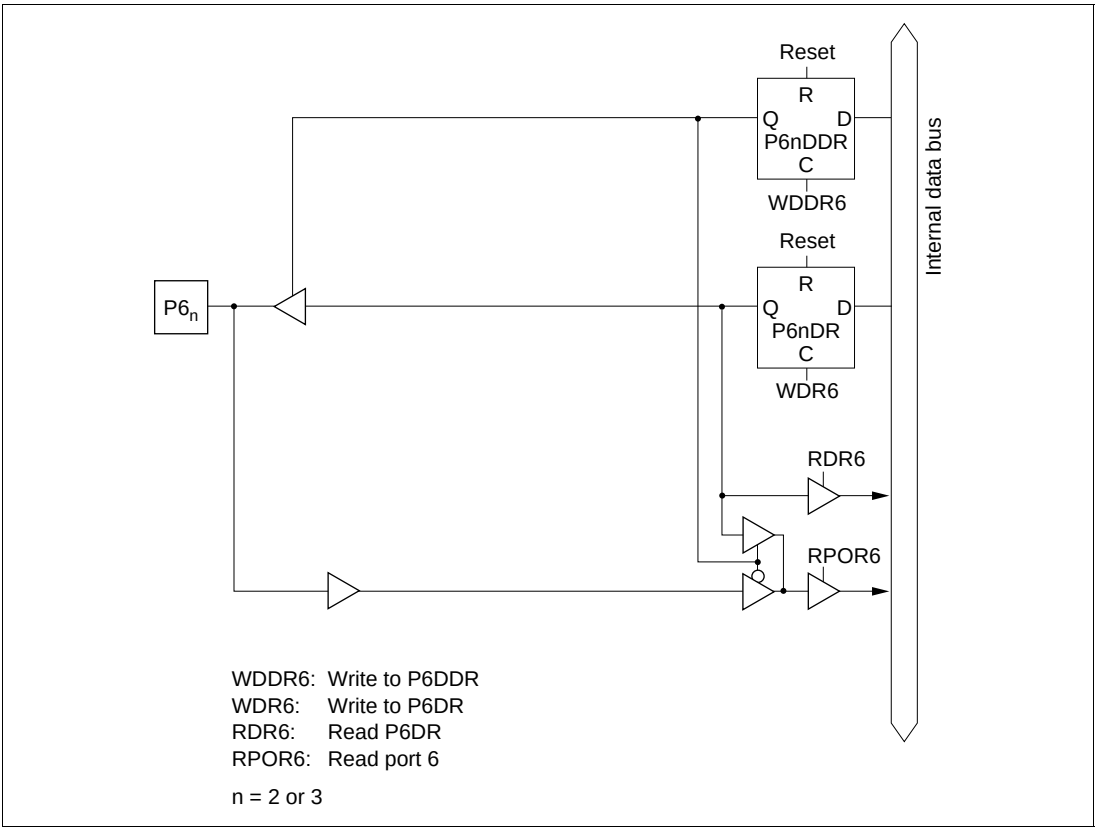


Figure 5.32 (b) Port 6 Block Diagram (Pins $P6_2$ and $P6_3$)

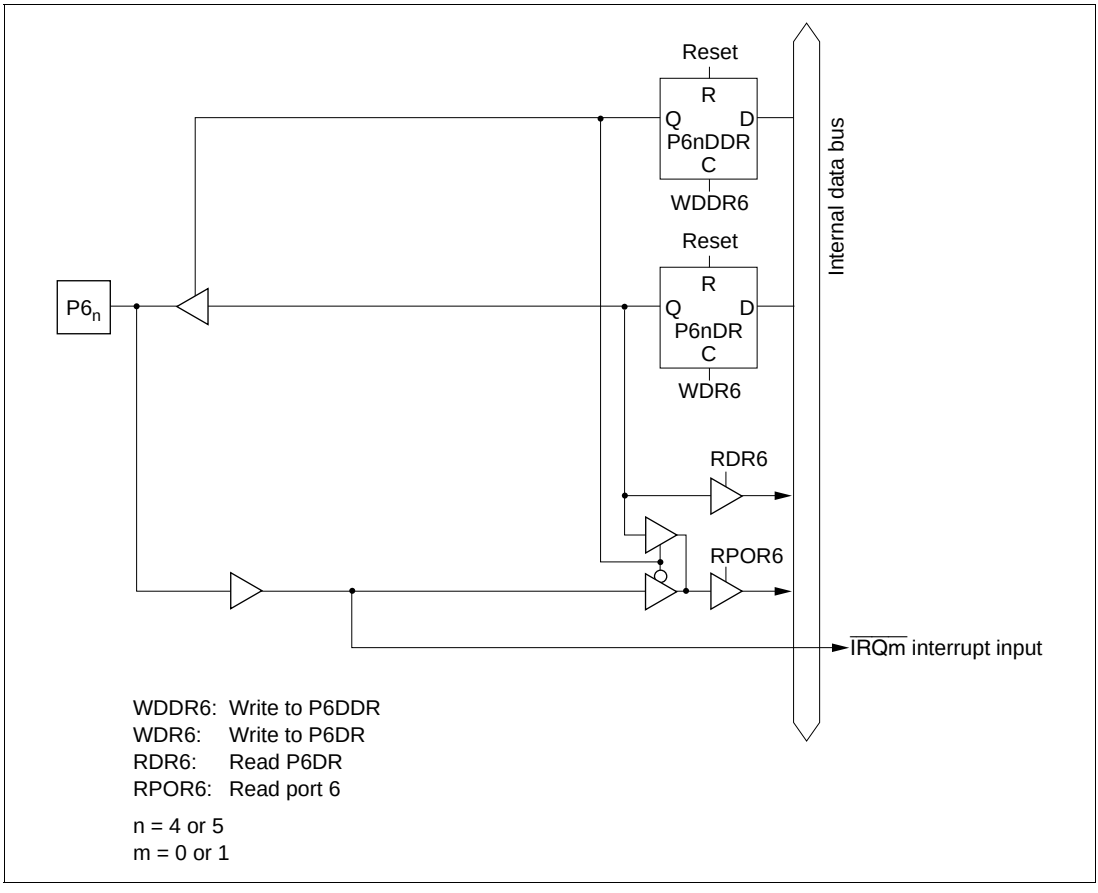


Figure 5.32 (c) Port 6 Block Diagram (Pins $P6_4$ and $P6_5$)

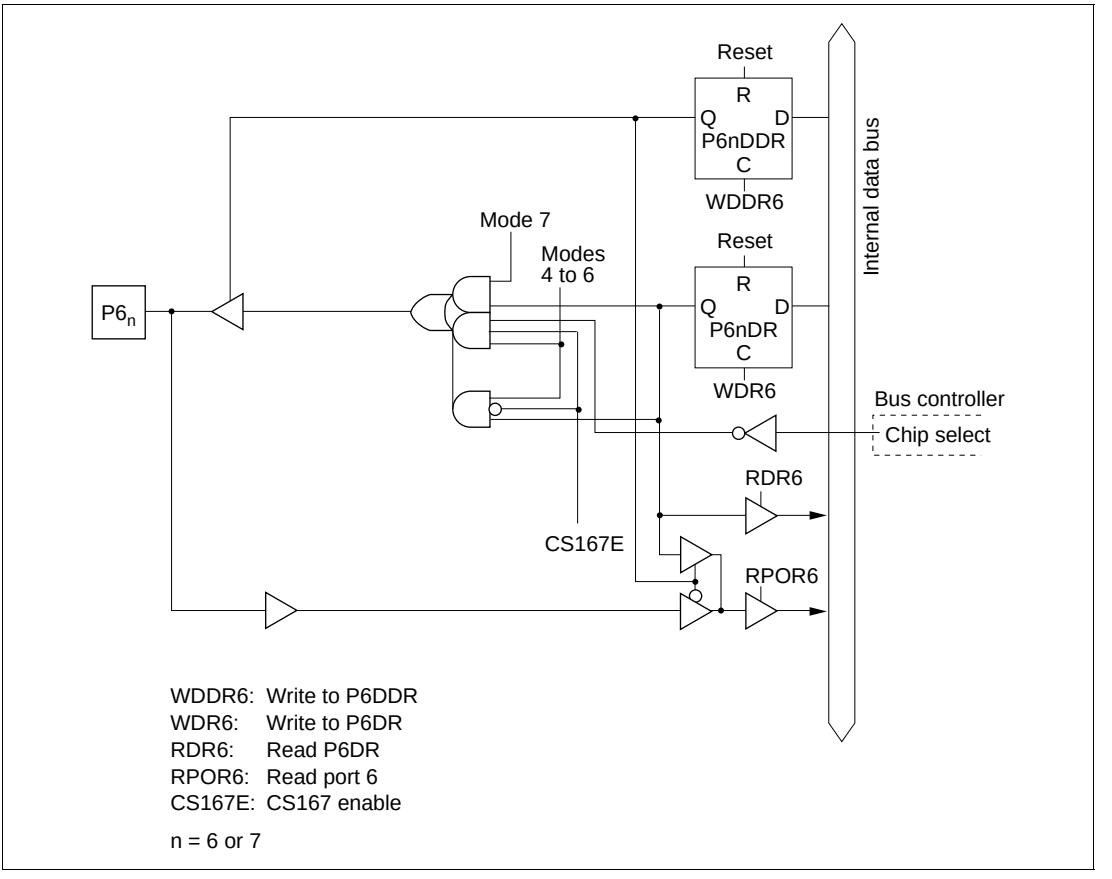


Figure 5.32 (d) Port 6 Block Diagram (Pins $P6_6$ and $P6_7$)

5.19.7 Port 7

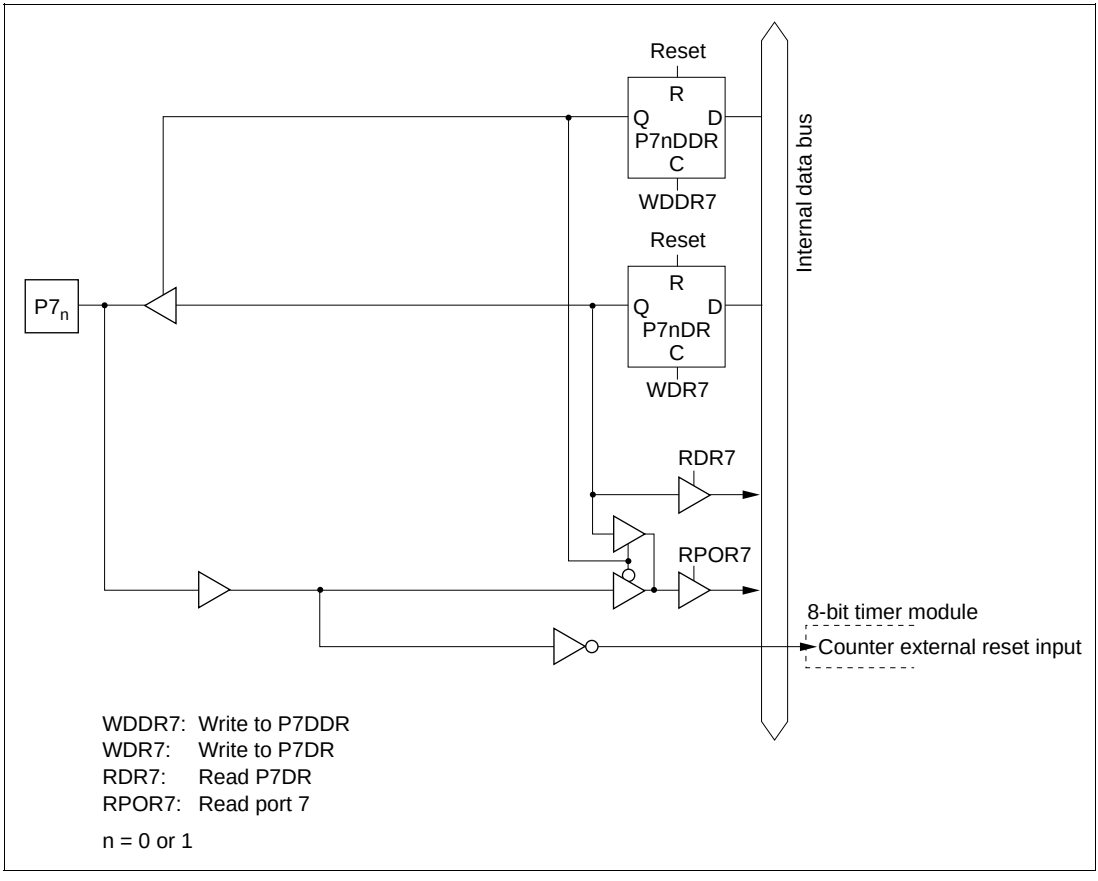


Figure 5.33 (a) Port 7 Block Diagram (Pins $P7_0$ and $P7_1$)

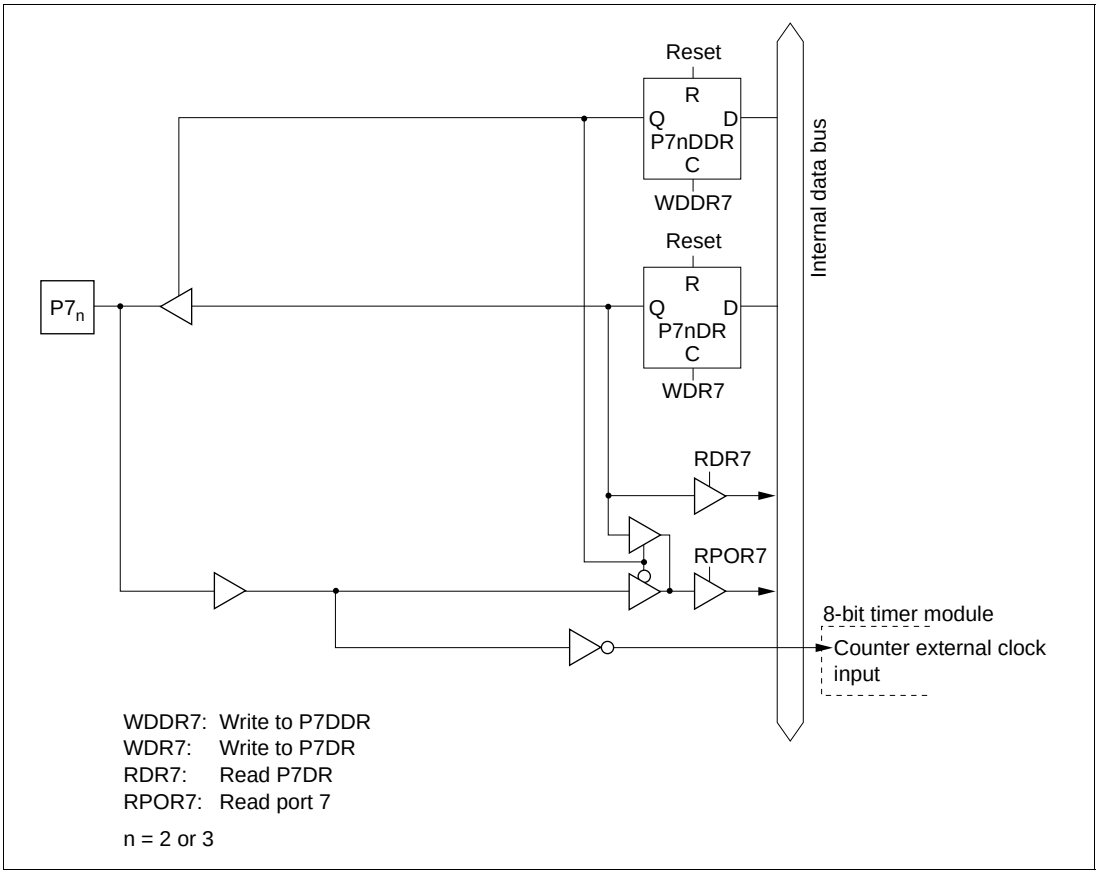


Figure 5.33 (b) Port 7 Block Diagram (Pins $P7_2$ and $P7_3$)

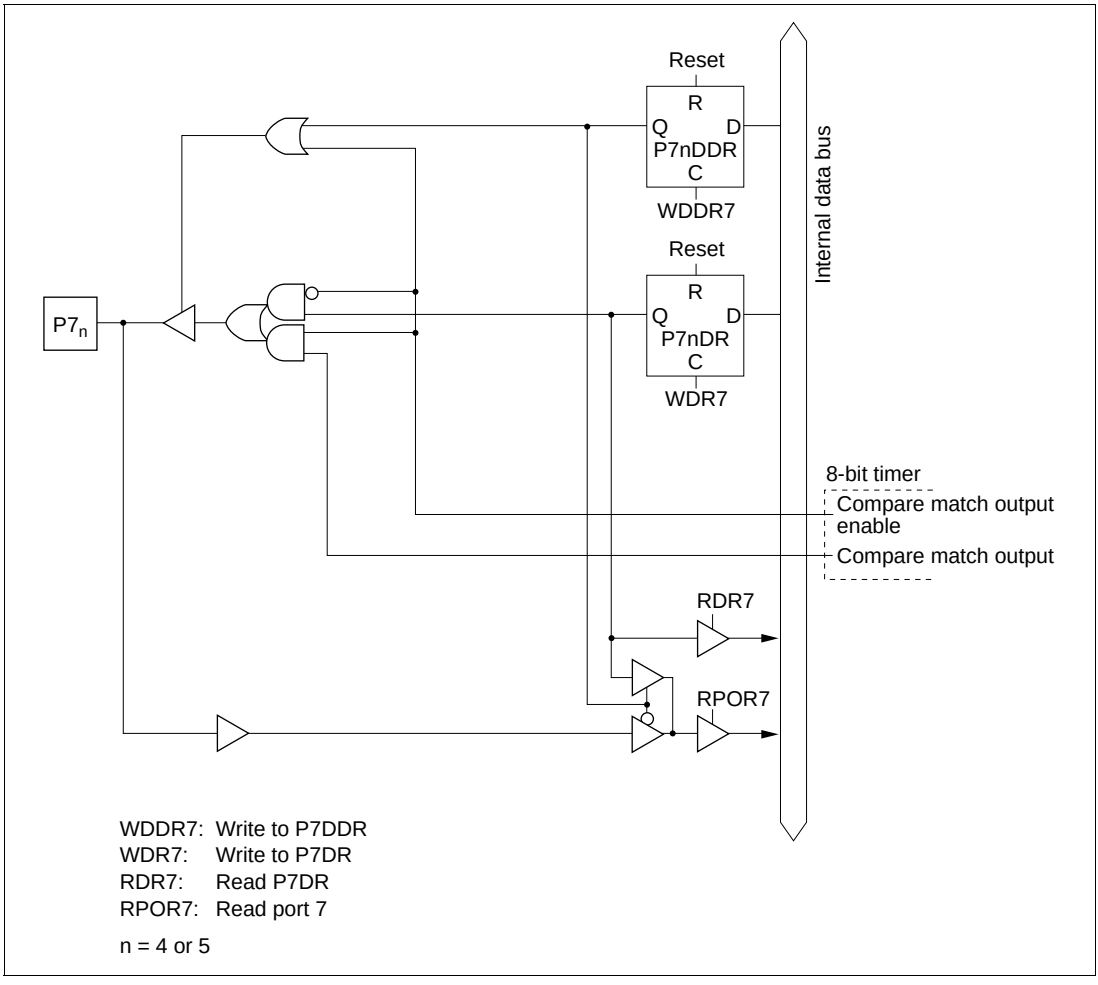


Figure 5.33 (c) Port 7 Block Diagram (Pins $P7_4$ and $P7_5$)

5.19.8 Port 8

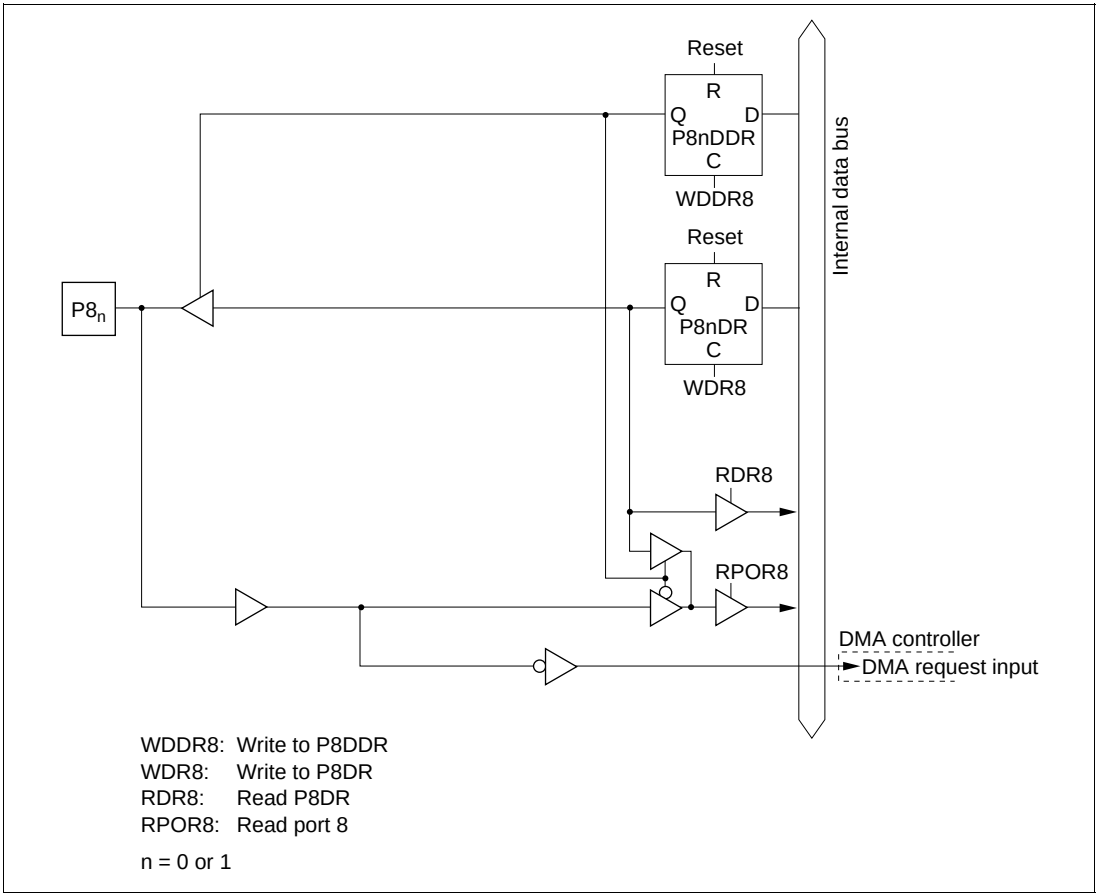


Figure 5.34 (a) Port 8 Block Diagram (Pins $P8_0$ and $P8_1$)

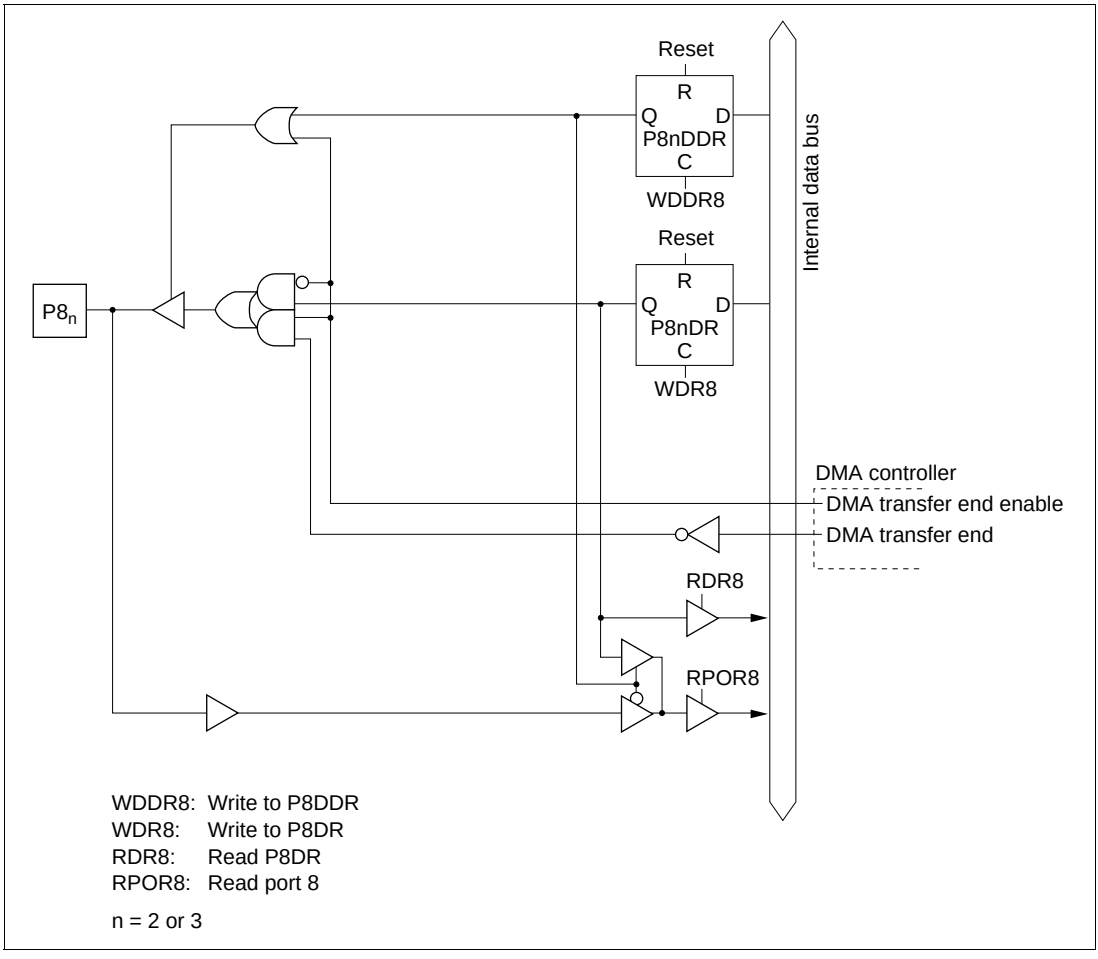


Figure 5.34 (b) Port 8 Block Diagram (Pins $P8_2$ and $P8_3$)

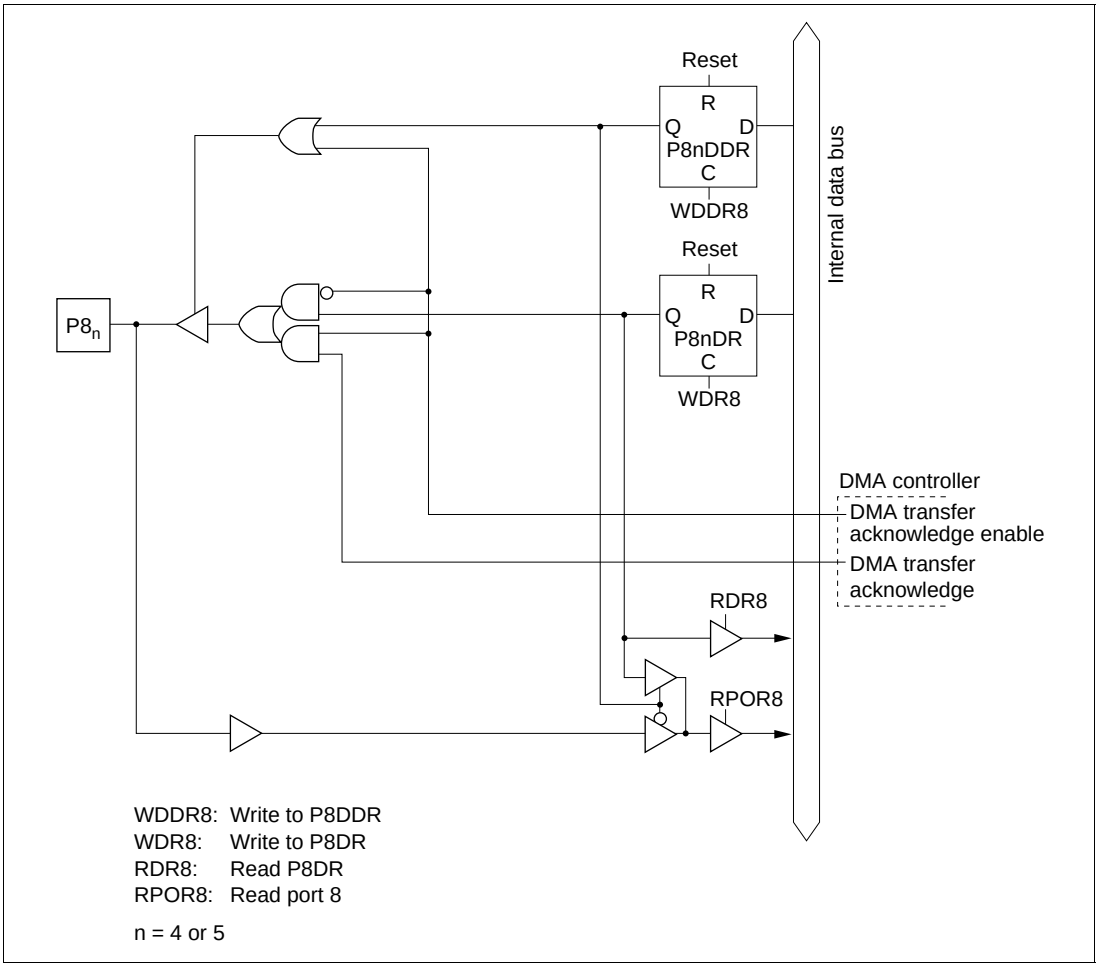


Figure 5.34 (c) Port 8 Block Diagram (Pins $P8_4$ and $P8_5$)

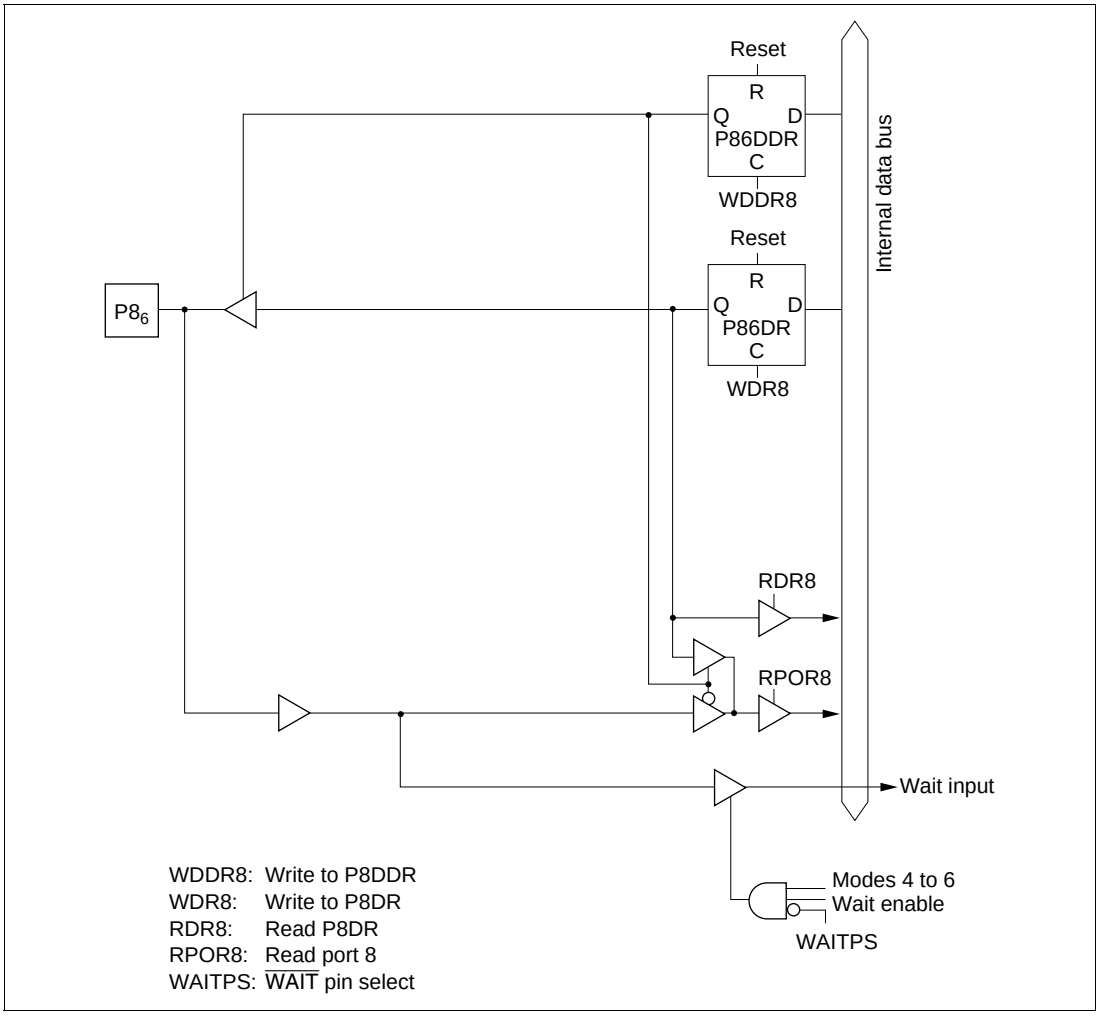


Figure 5.34 (d) Port 8 Block Diagram (Pin P8$_6$)

5.19.9 Port 9

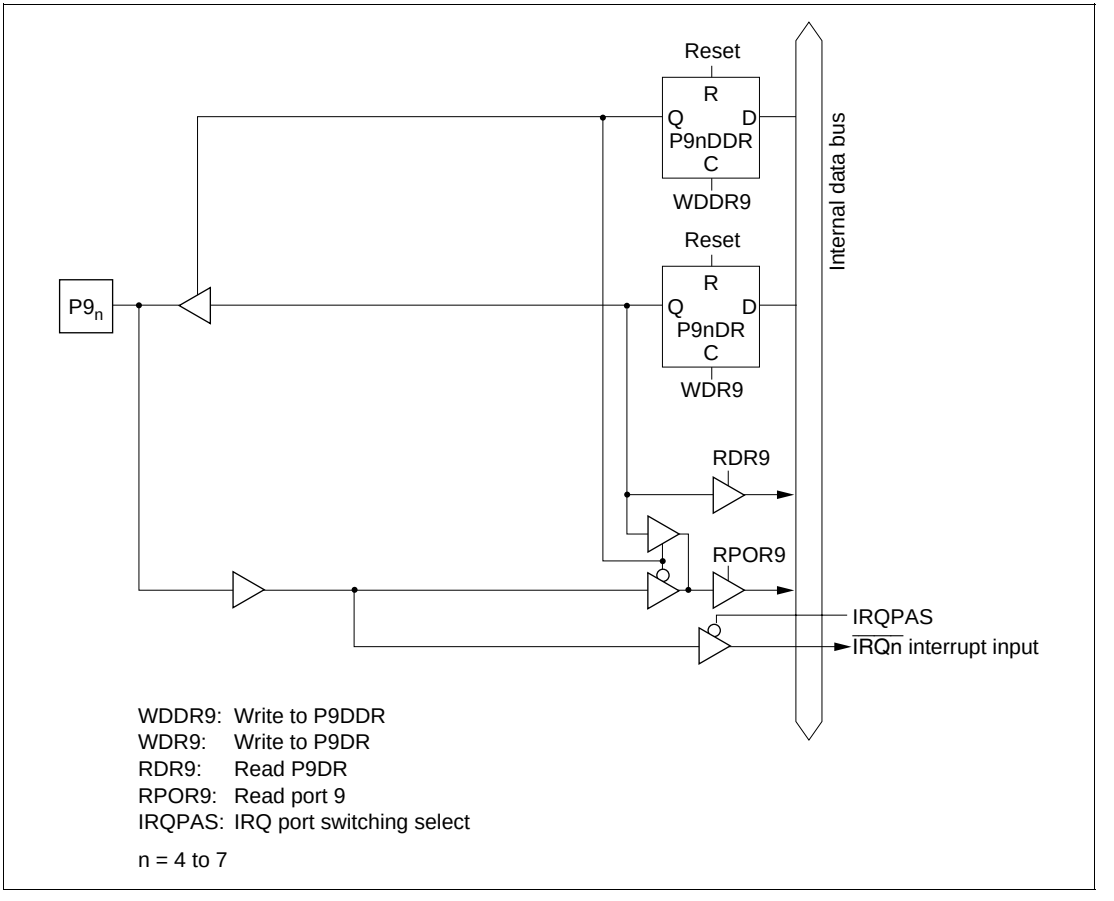


Figure 5.35 (a) Port 9 Block Diagram (Pins $P9_4$ to $P9_7$)

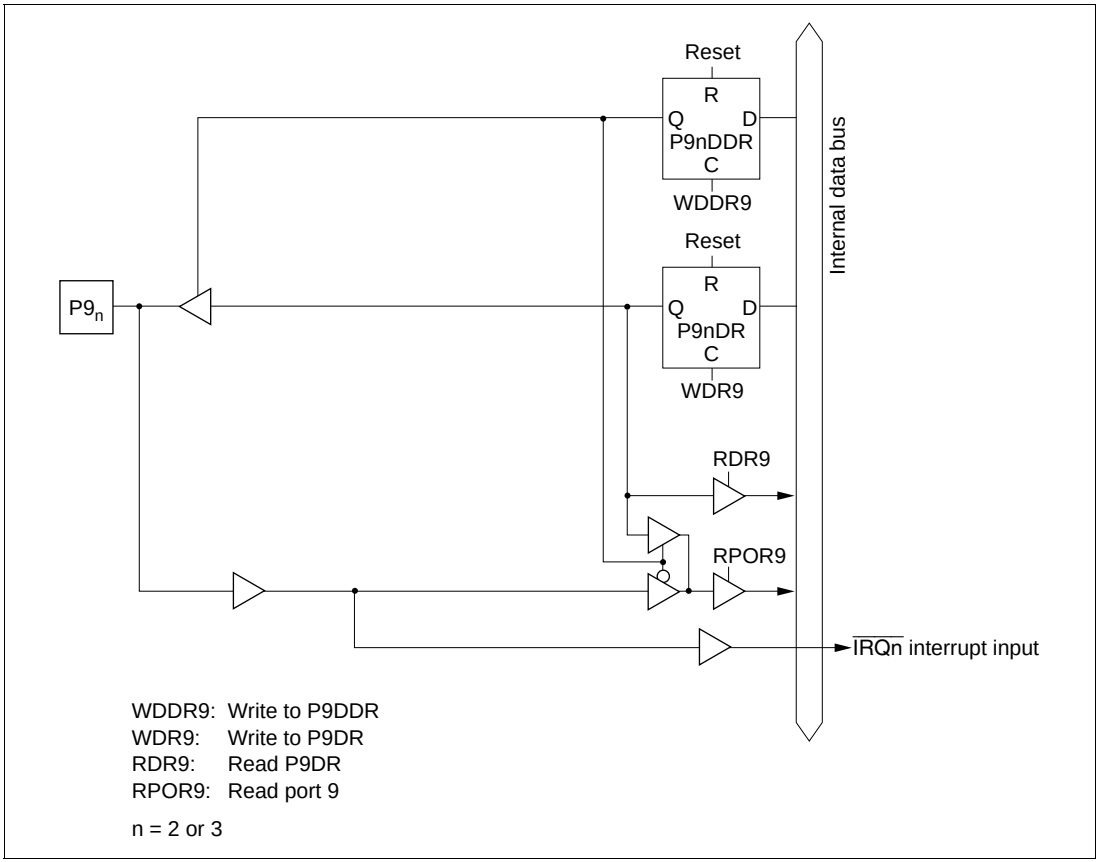


Figure 5.35 (b) Port 9 Block Diagram (Pins $P9_2$ and $P9_3$)

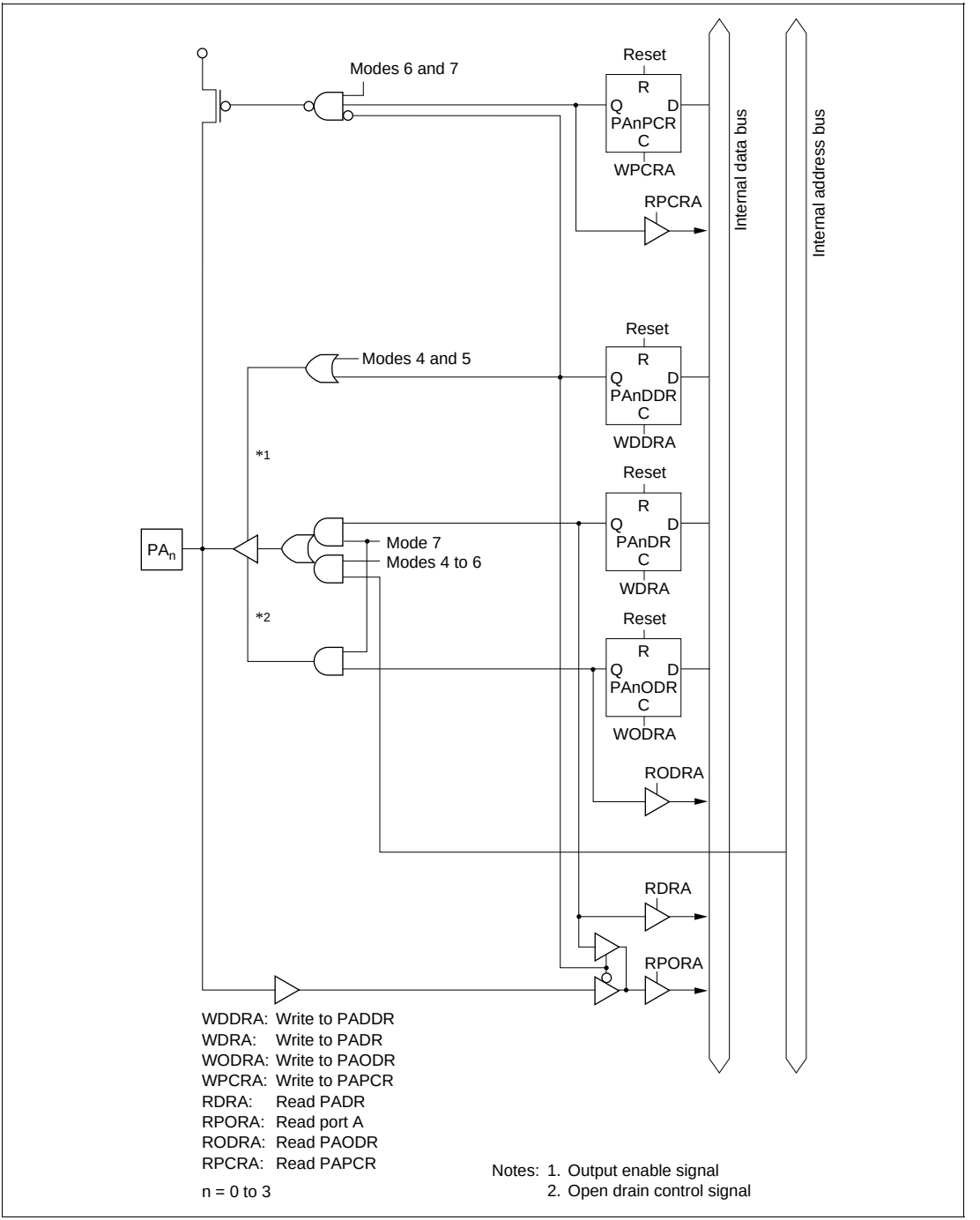


Figure 5.36 (a) Port A Block Diagram (Pins PA_0, PA_1, PA_2, and PA_3)

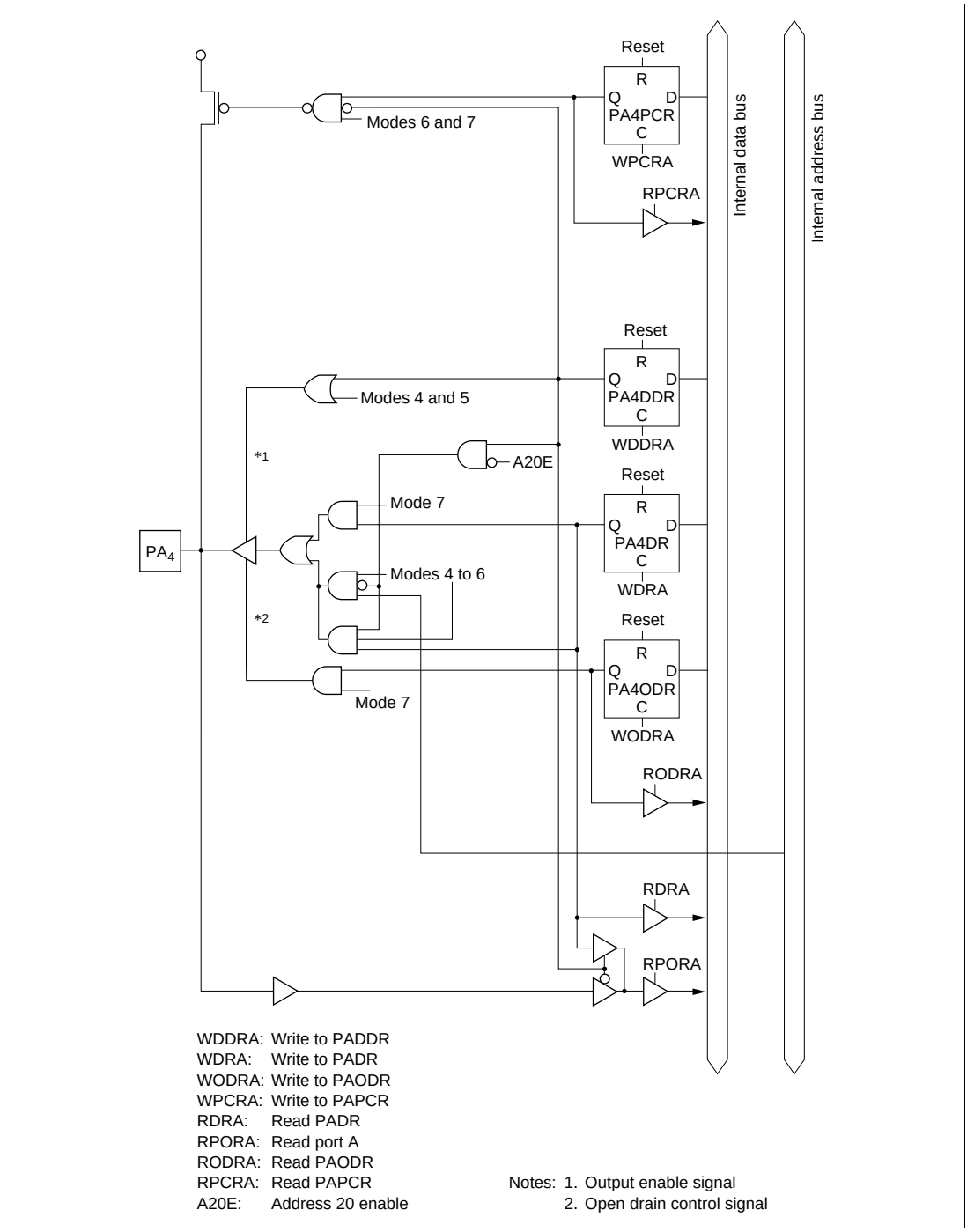


Figure 5.36 (b) Port A Block Diagram (Pin PA_4)

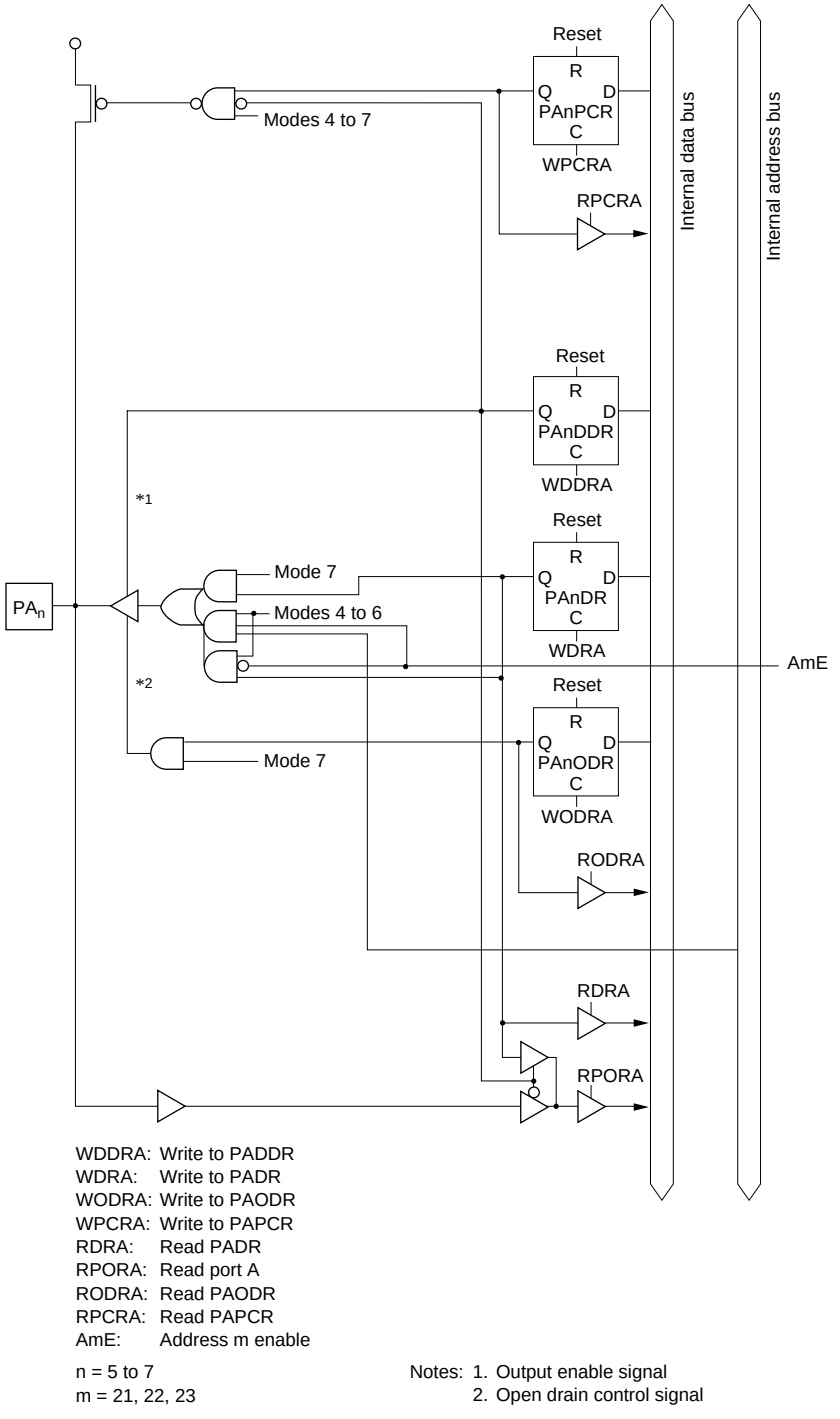


Figure 5.36 (c) Port A Block Diagram (Pins PA_5, PA_6, and PA_7)

5.19.11 Port B

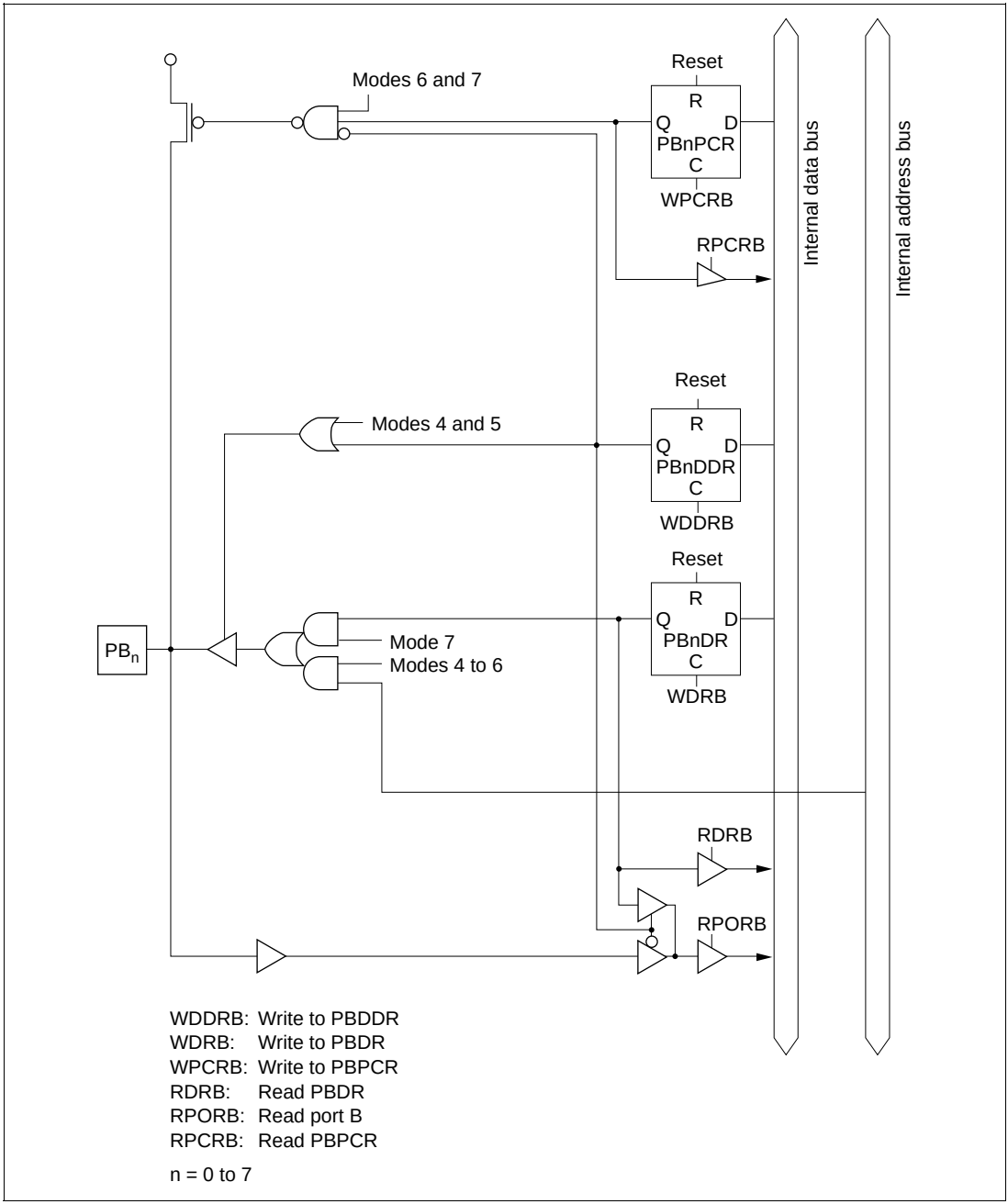


Figure 5.37 Port B Block Diagram (Pins PB_n)

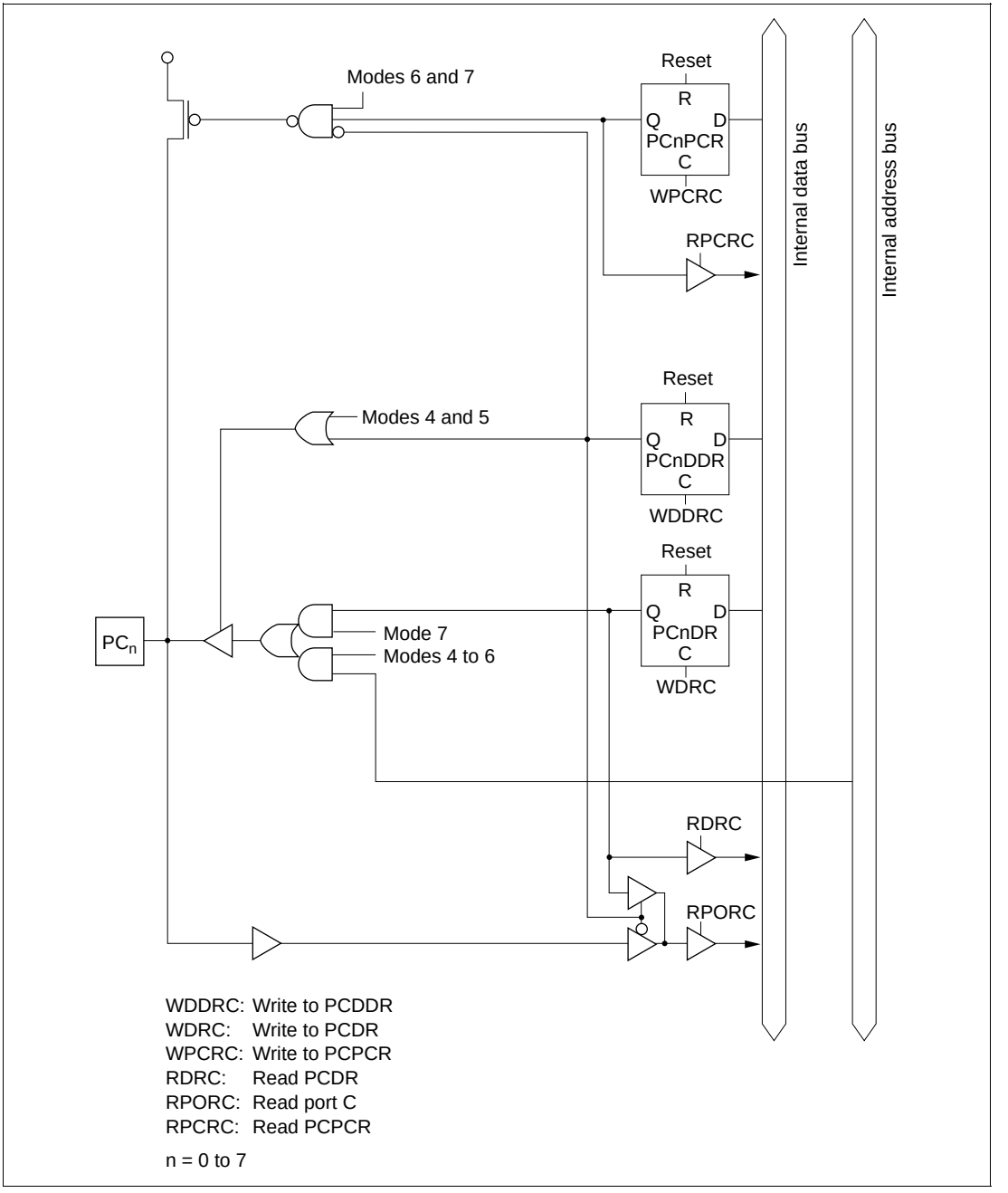


Figure 5.38 Port C Block Diagram (Pins PC_n)

5.19.13 Port D

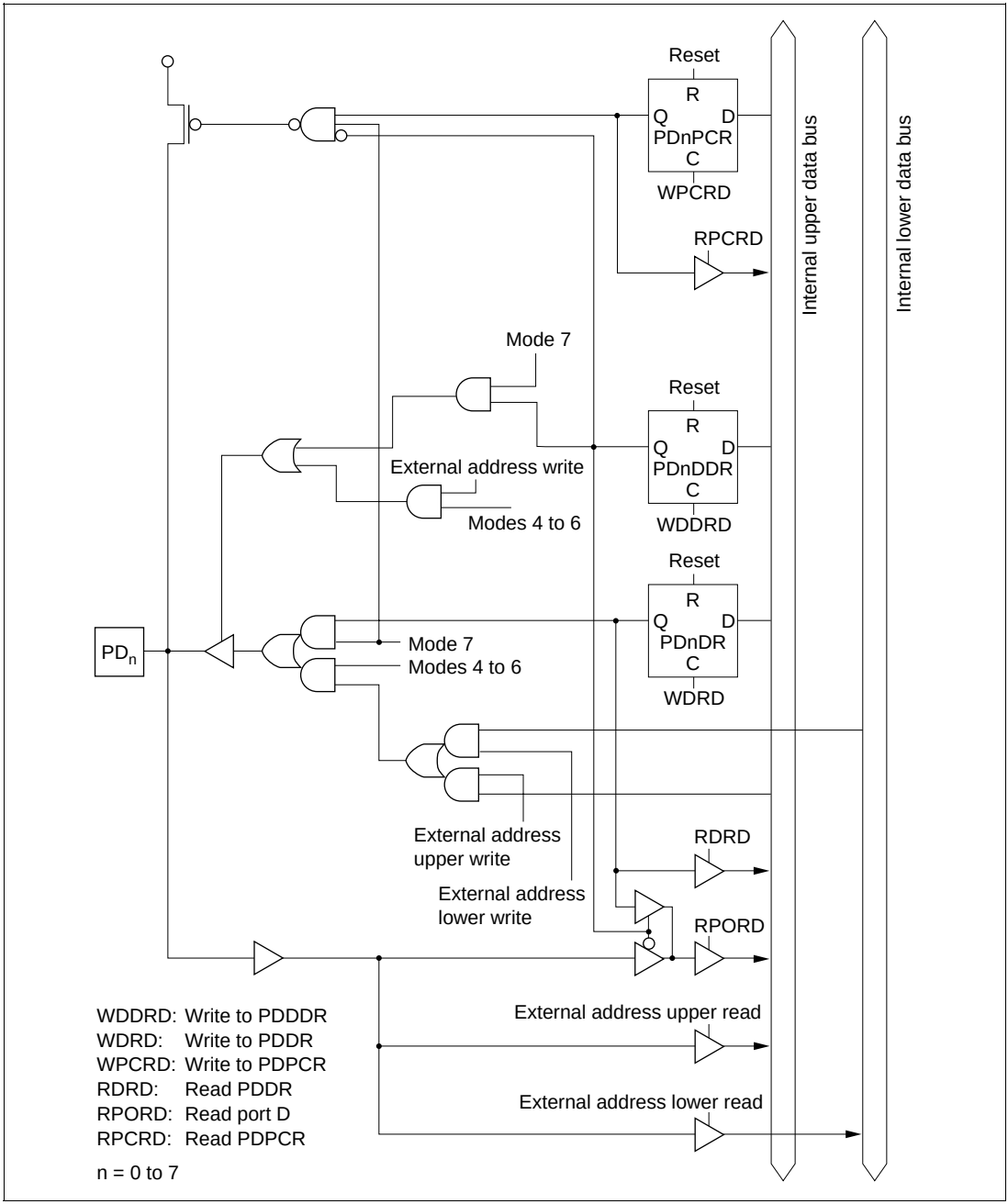


Figure 5.39 Port D Block Diagram (Pins PD_n)

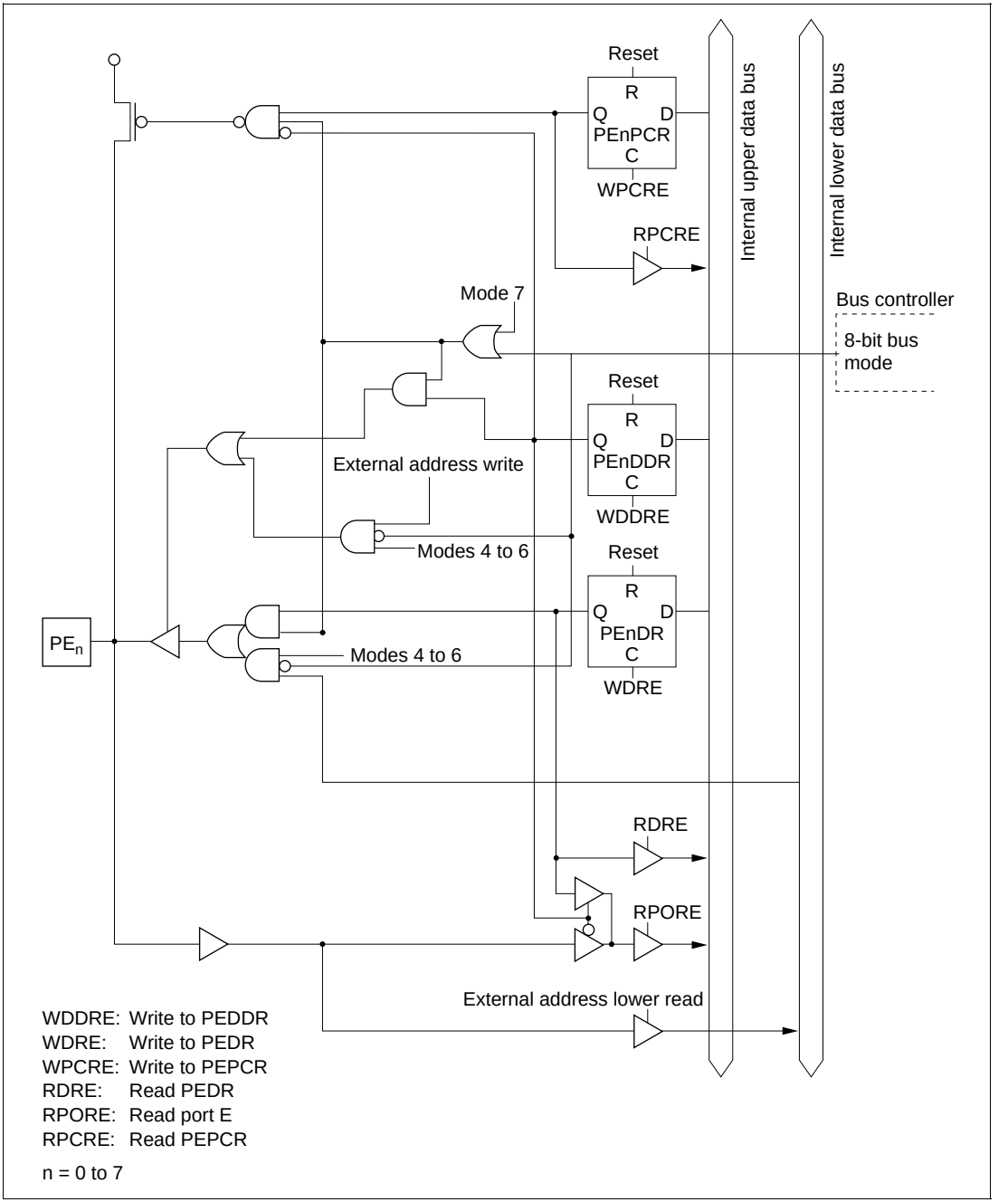


Figure 5.40 Port E Block Diagram (Pins PE_n)

5.19.15 Port F

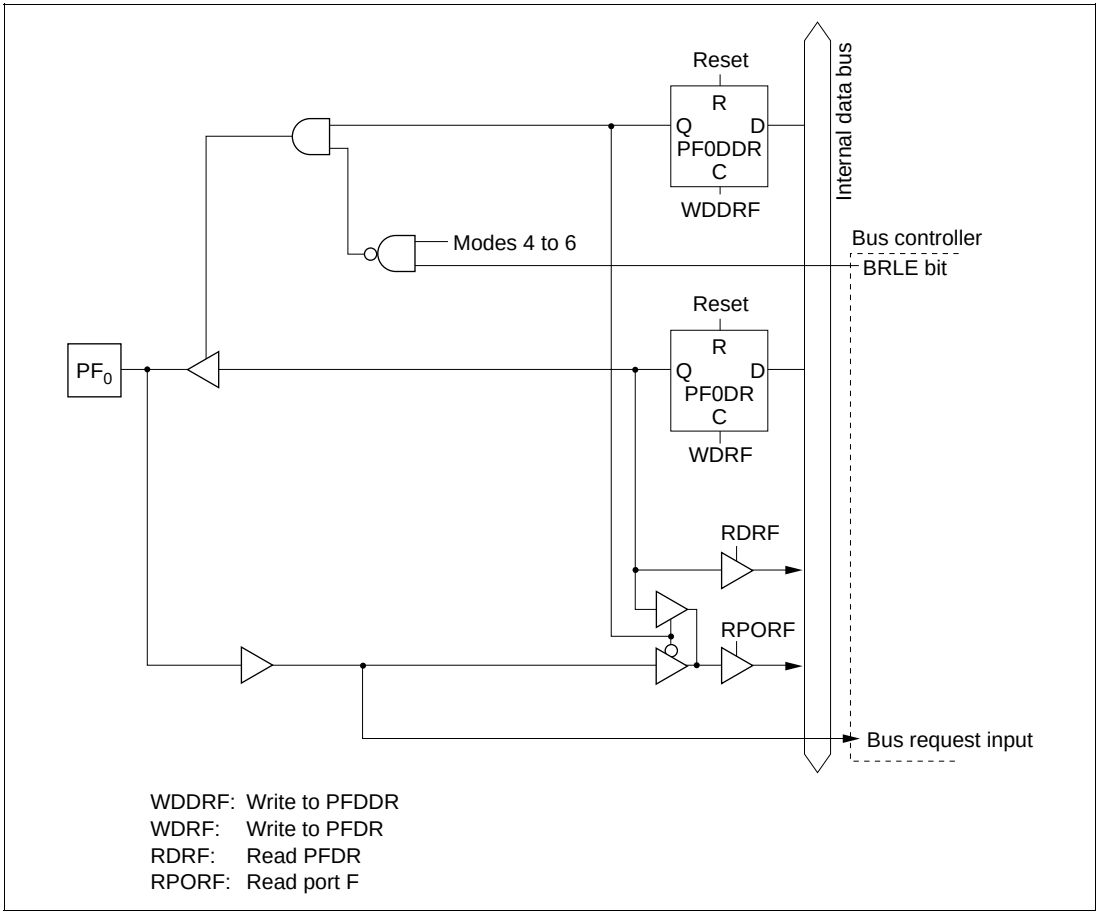


Figure 5.41 (a) Port F Block Diagram (Pin PF_0)

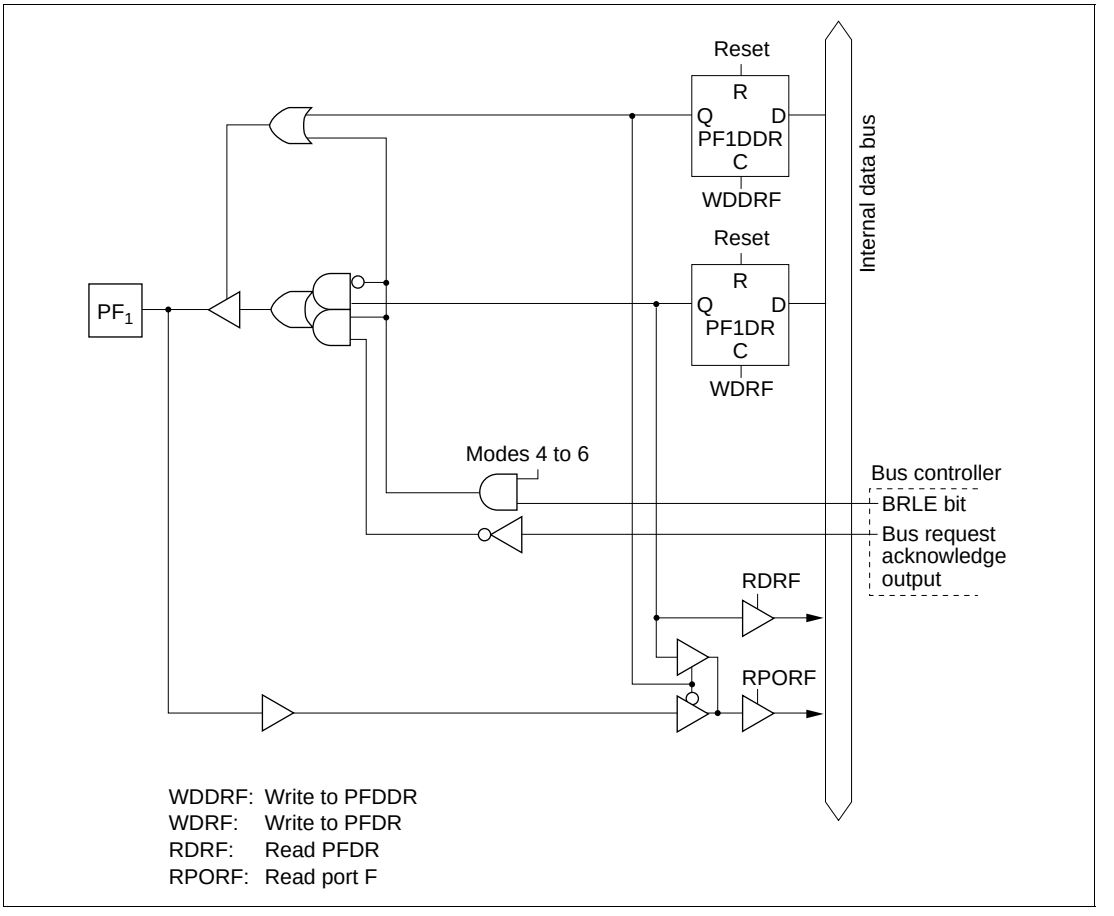


Figure 5.41 (b) Port F Block Diagram (Pin PF_1)

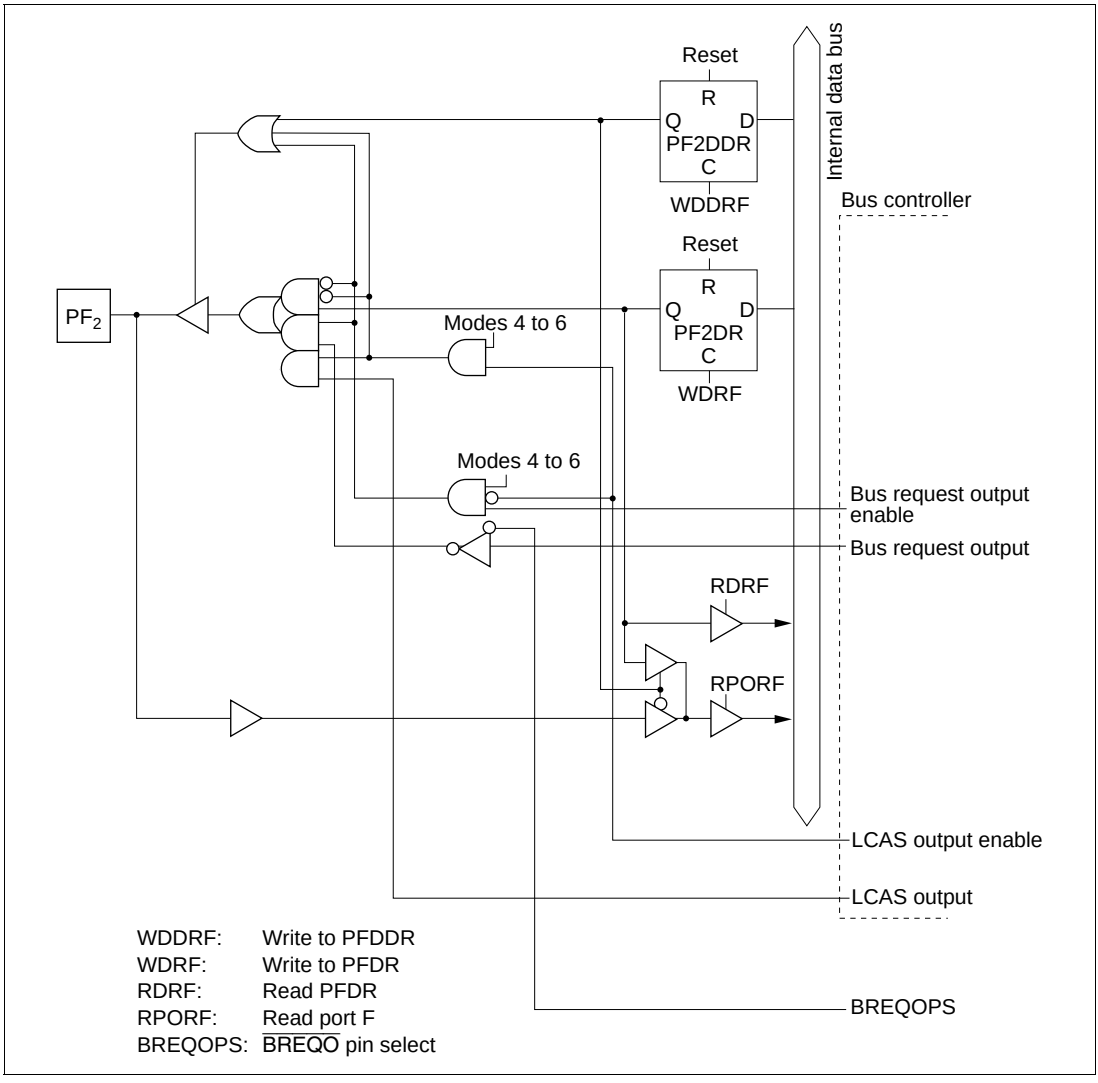


Figure 5.41 (c) Port F Block Diagram (Pin PF_2)

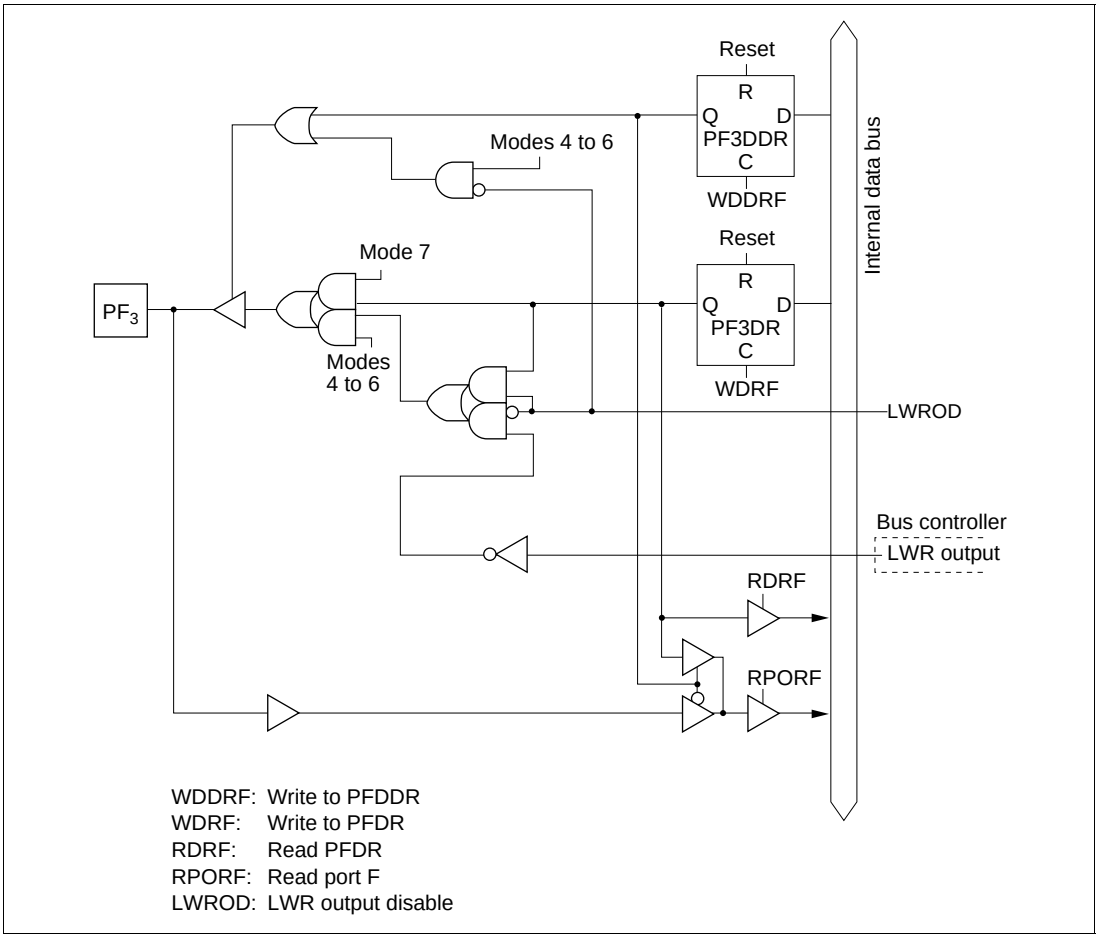


Figure 5.41 (d) Port F Block Diagram (Pin PF_3)

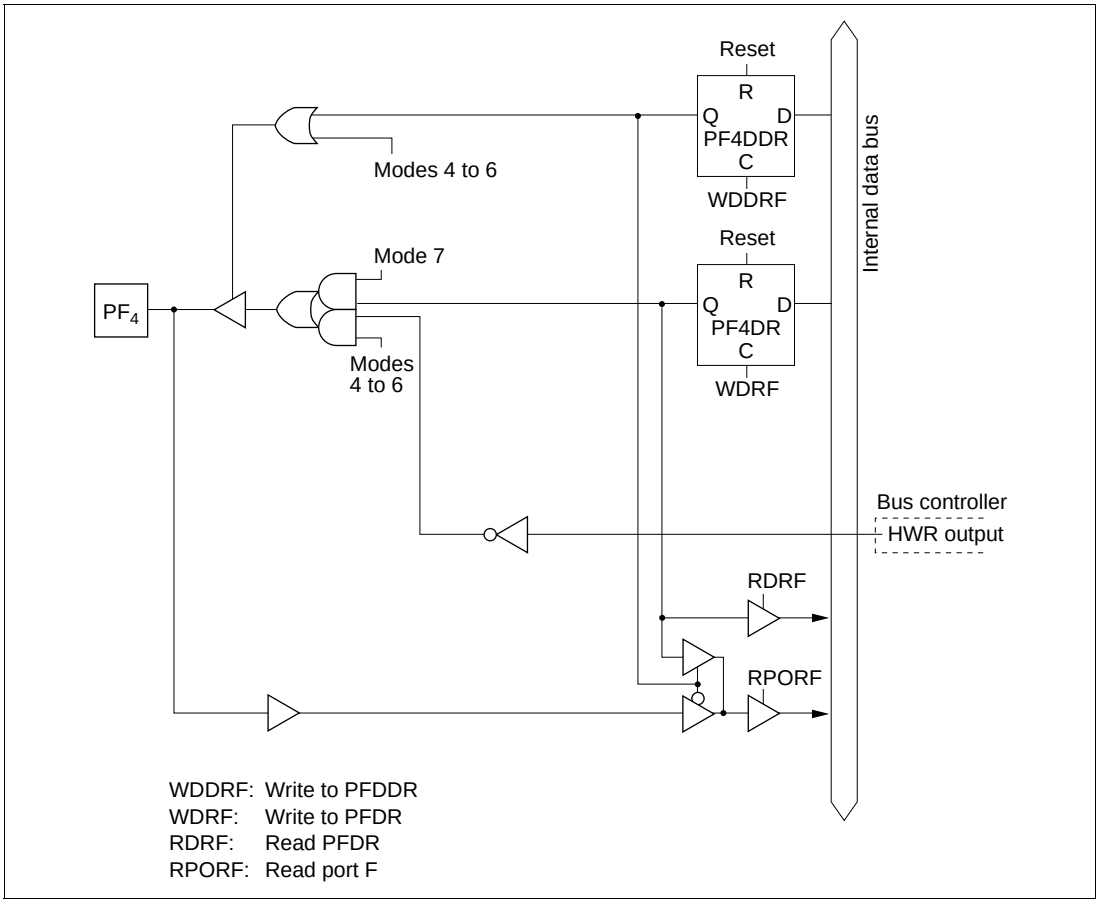


Figure 5.41 (e) Port F Block Diagram (Pin PF_4)

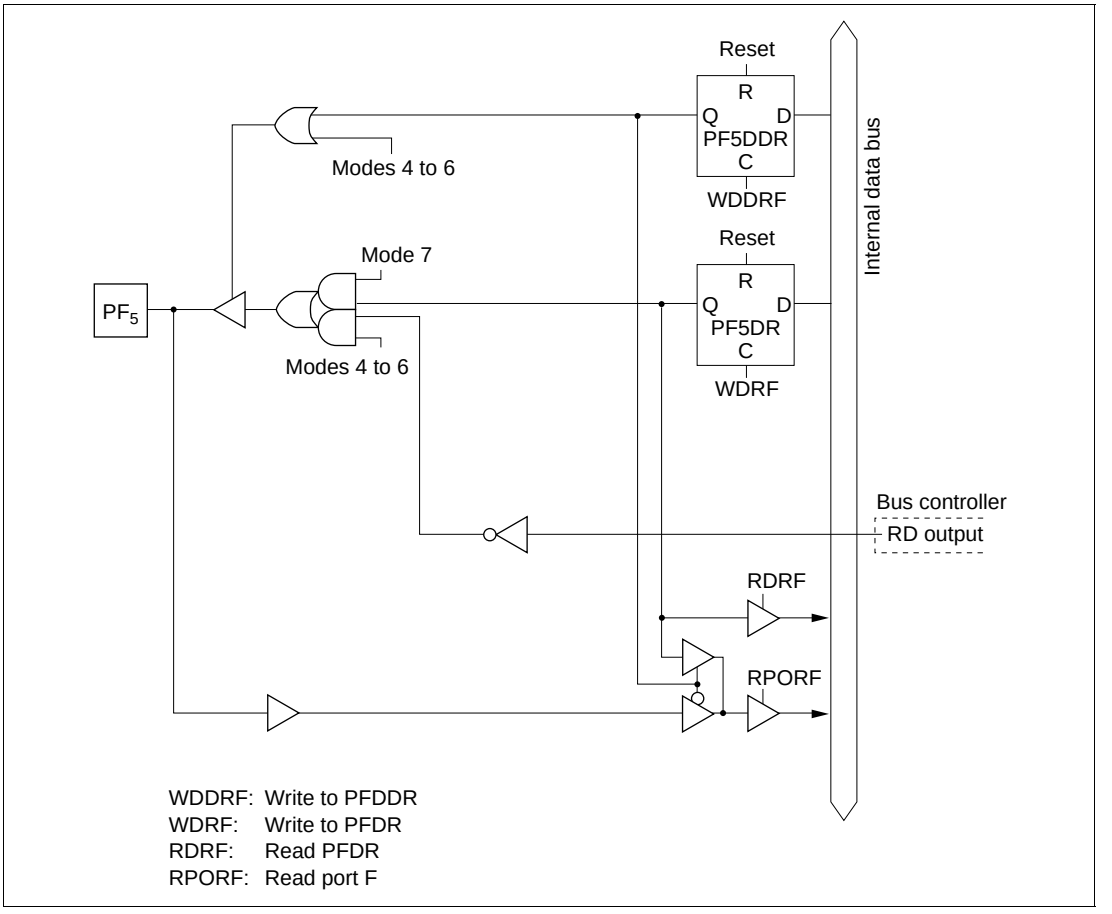


Figure 5.41 (f) Port F Block Diagram (Pin PF_5)

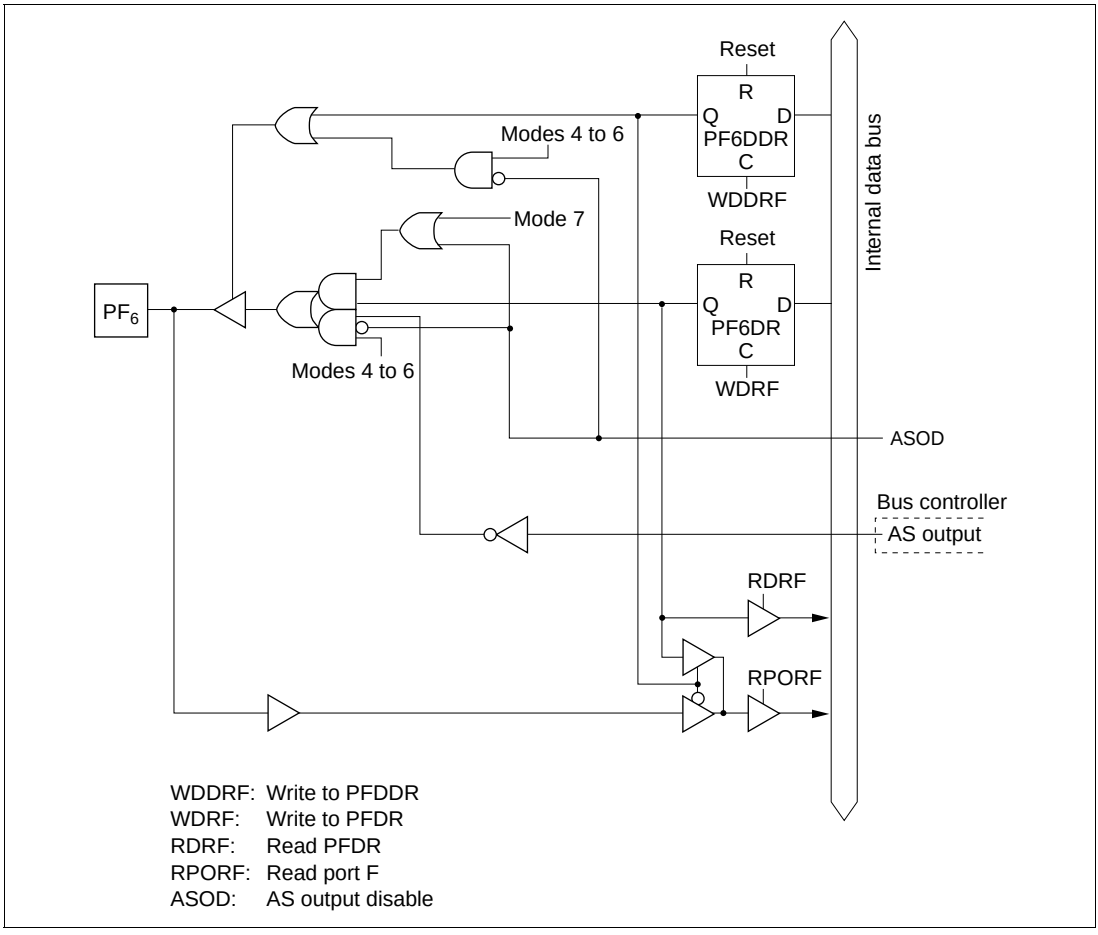


Figure 5.41 (g) Port F Block Diagram (Pin PF_6)

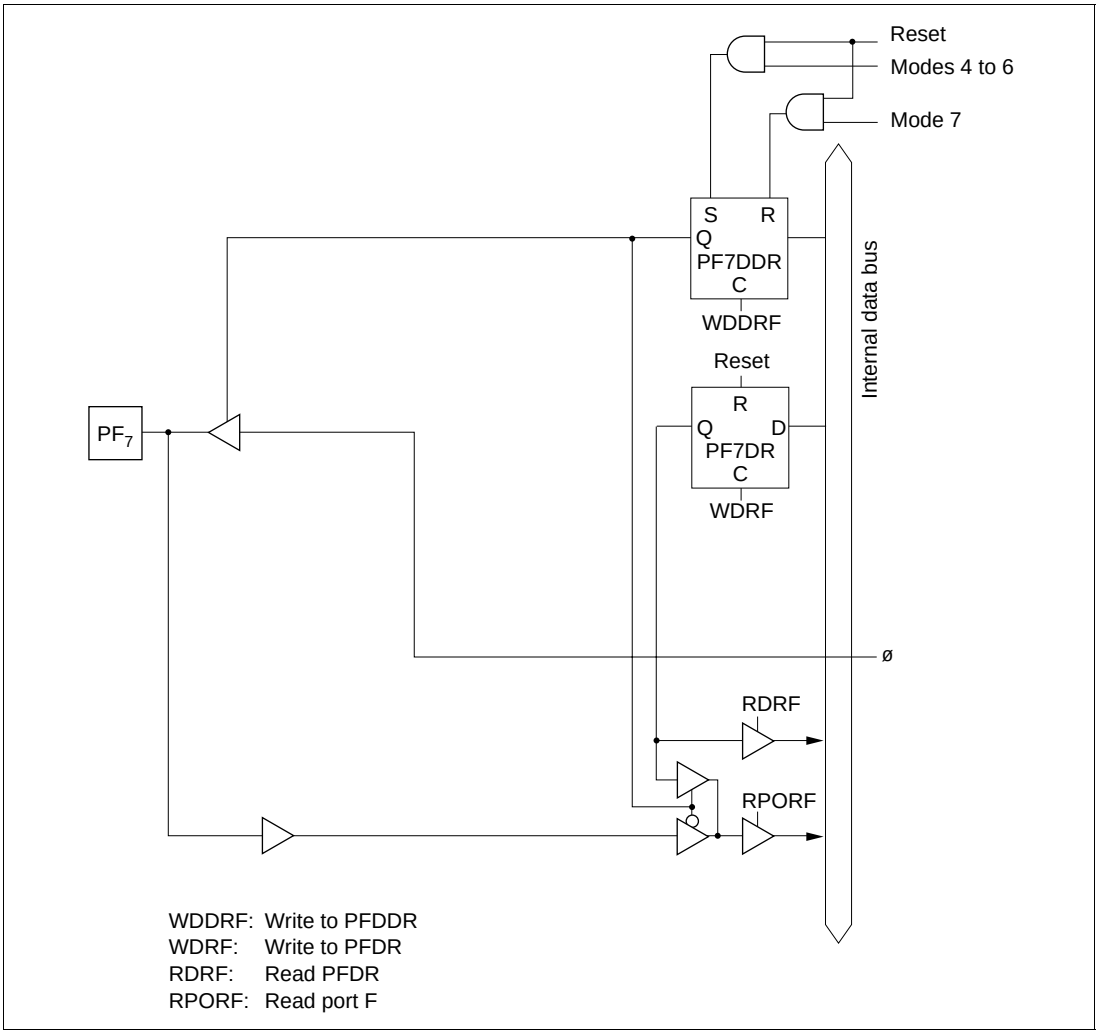


Figure 5.41 (h) Port F Block Diagram (Pin PF_7)

5.19.16 Port G

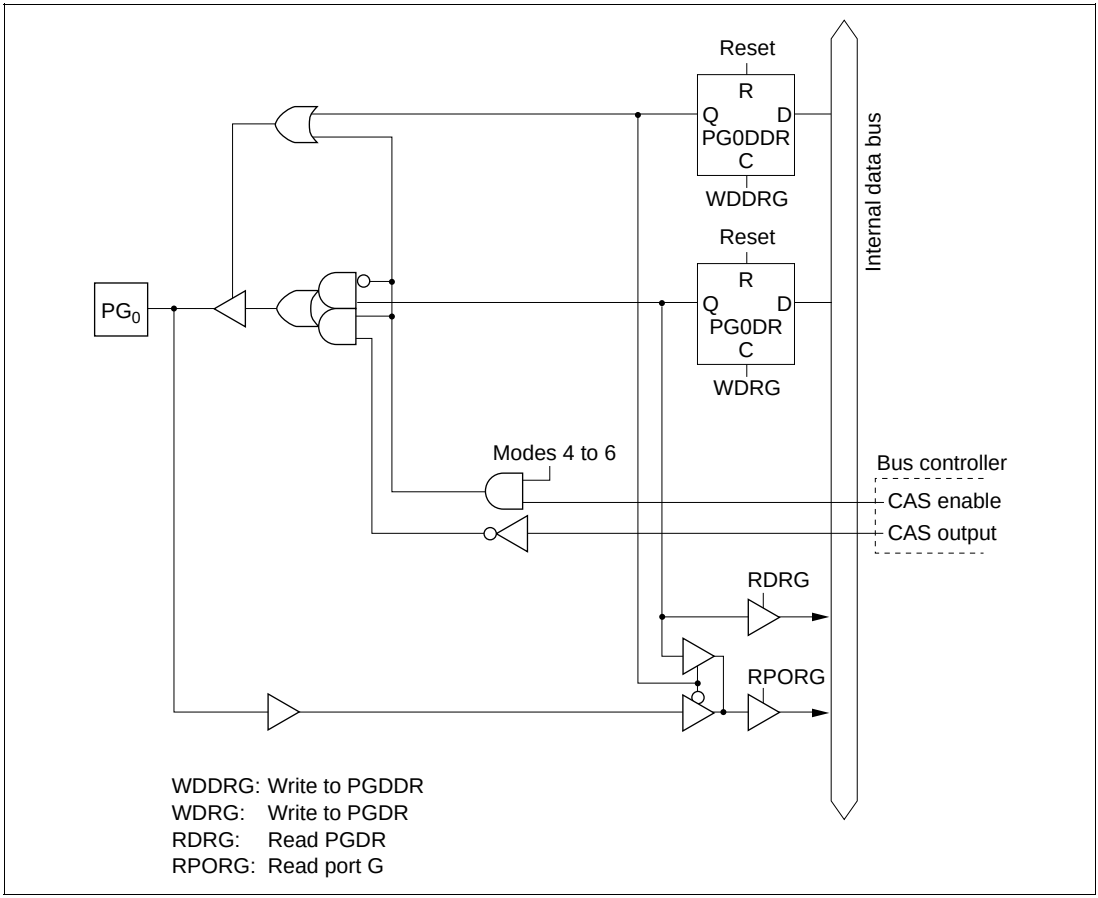


Figure 5.42 (a) Port G Block Diagram (Pin PG_0)

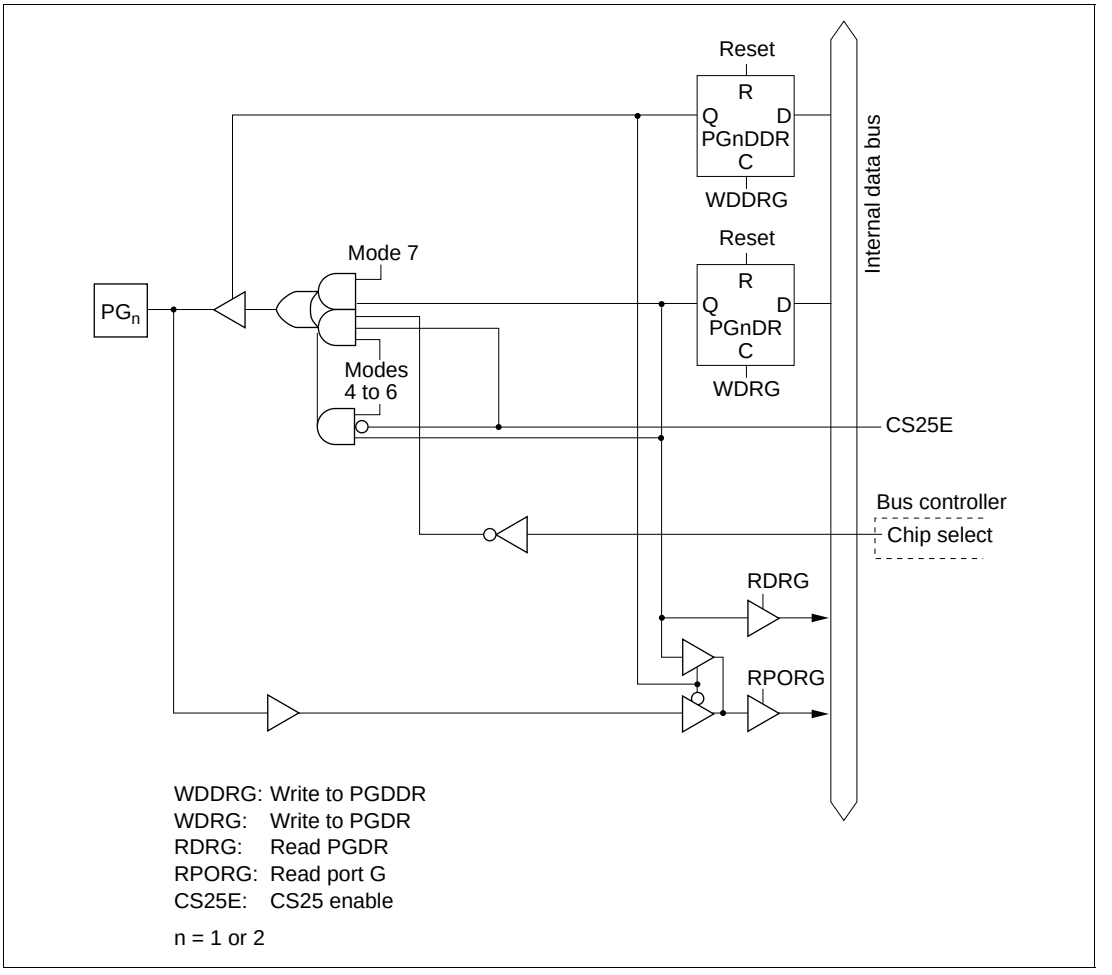


Figure 5.42 (b) Port G Block Diagram (Pins PG_1 and PG_2)

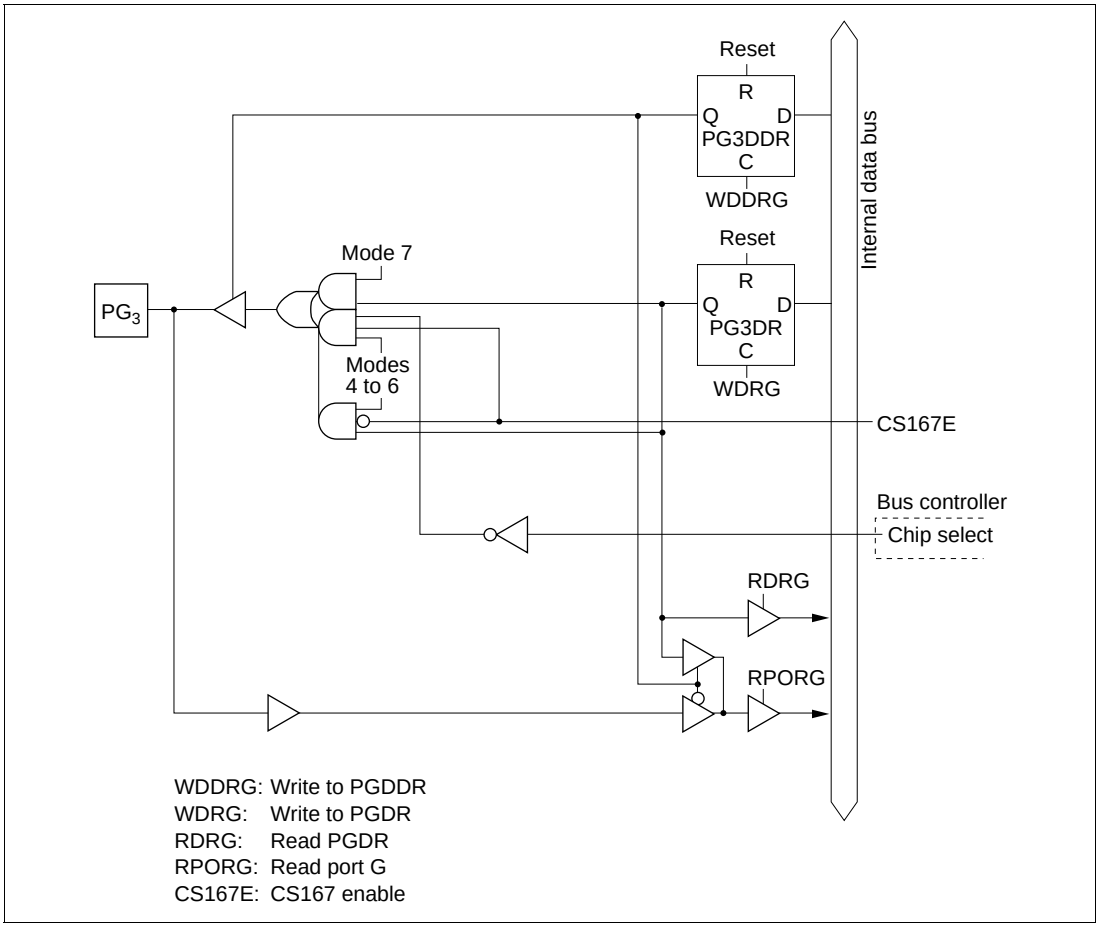


Figure 5.42 (c) Port G Block Diagram (Pin PG_3)

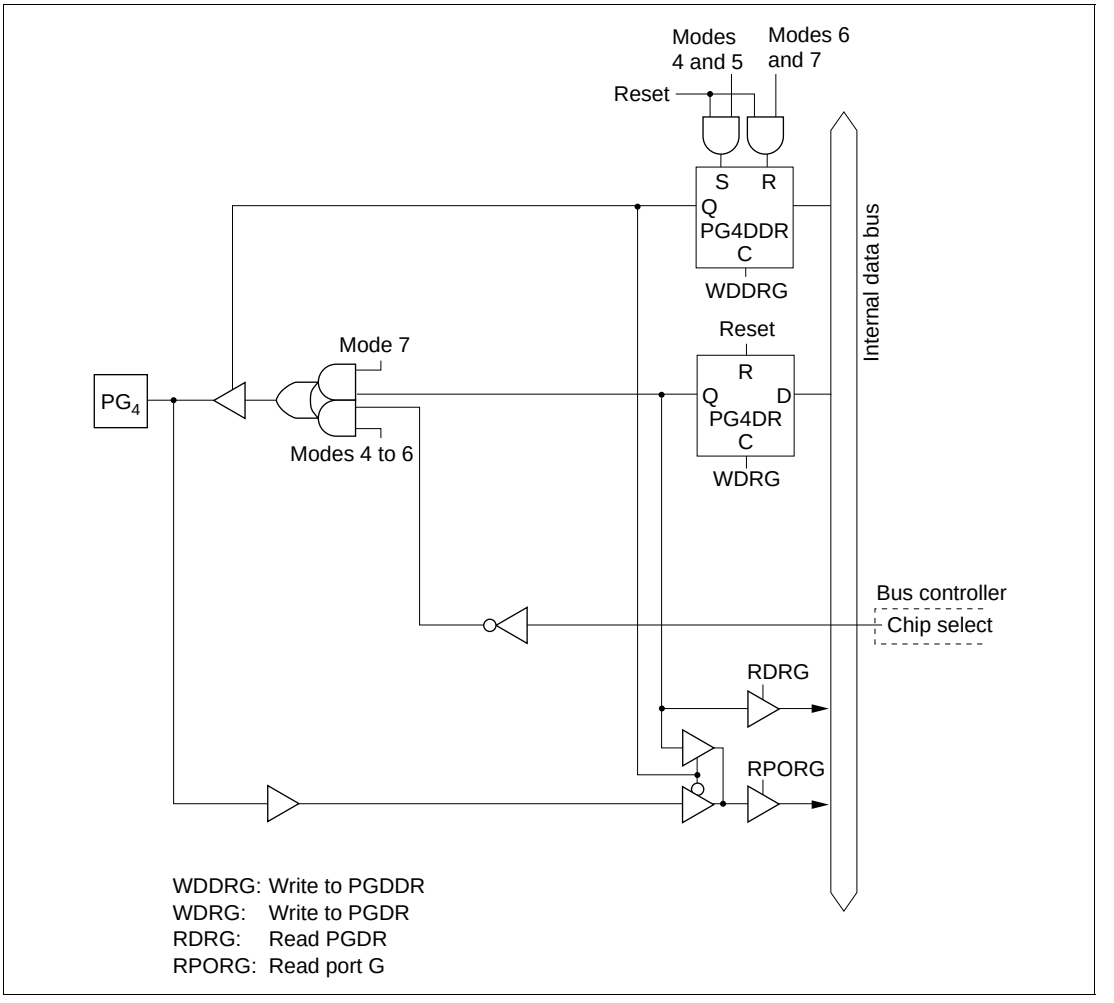


Figure 5.42 (d) Port G Block Diagram (Pin PG_4)

Section 6 Supporting Module Block Diagrams

6.1 Interrupt Controller

6.1.1 Features

- Selection of two interrupt control modes
- Eight priority levels can be set for each module with IPR
- Independent vector addresses (NMI, $\overline{IRQ}_7$ to $\overline{IRQ}_0$)
- Nine external interrupt pins
- DTC and DMAC activation control

6.1.2 Block Diagram

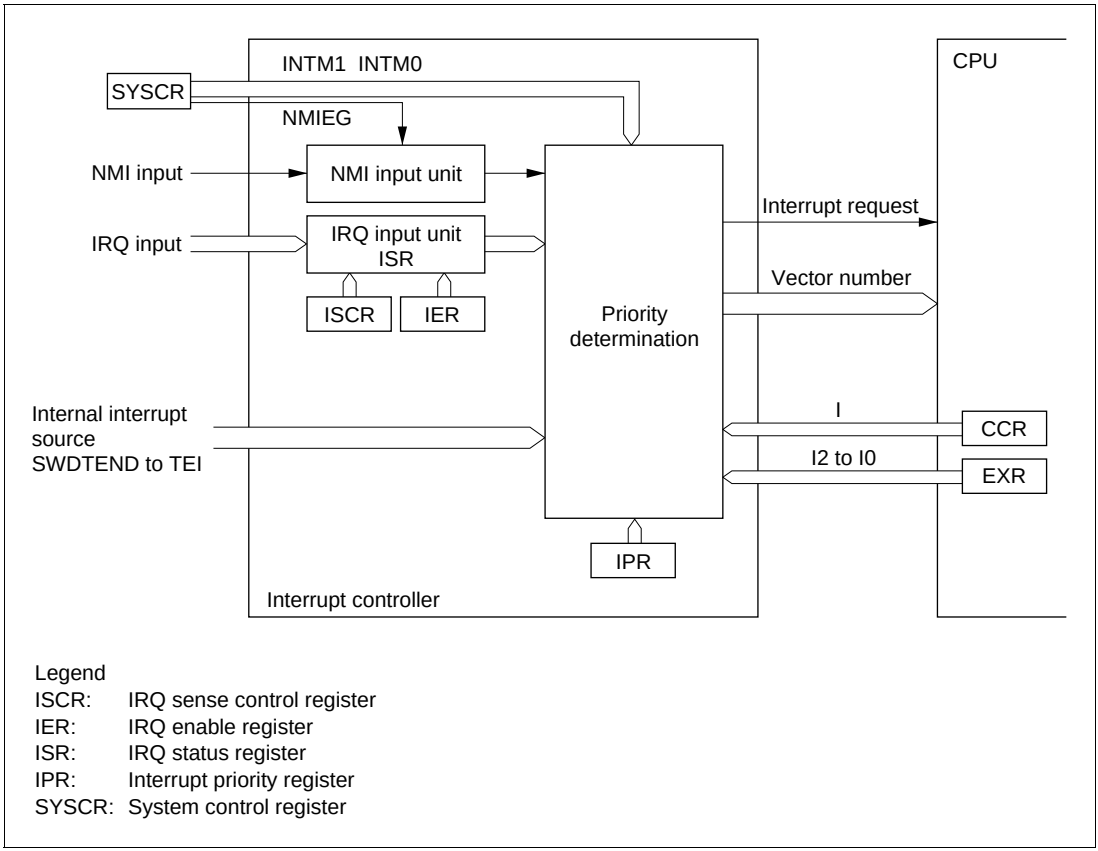


Figure 6.1 Block Diagram of Interrupt Controller

6.1.3 Pins

Table 6.1 Interrupt Controller Pins

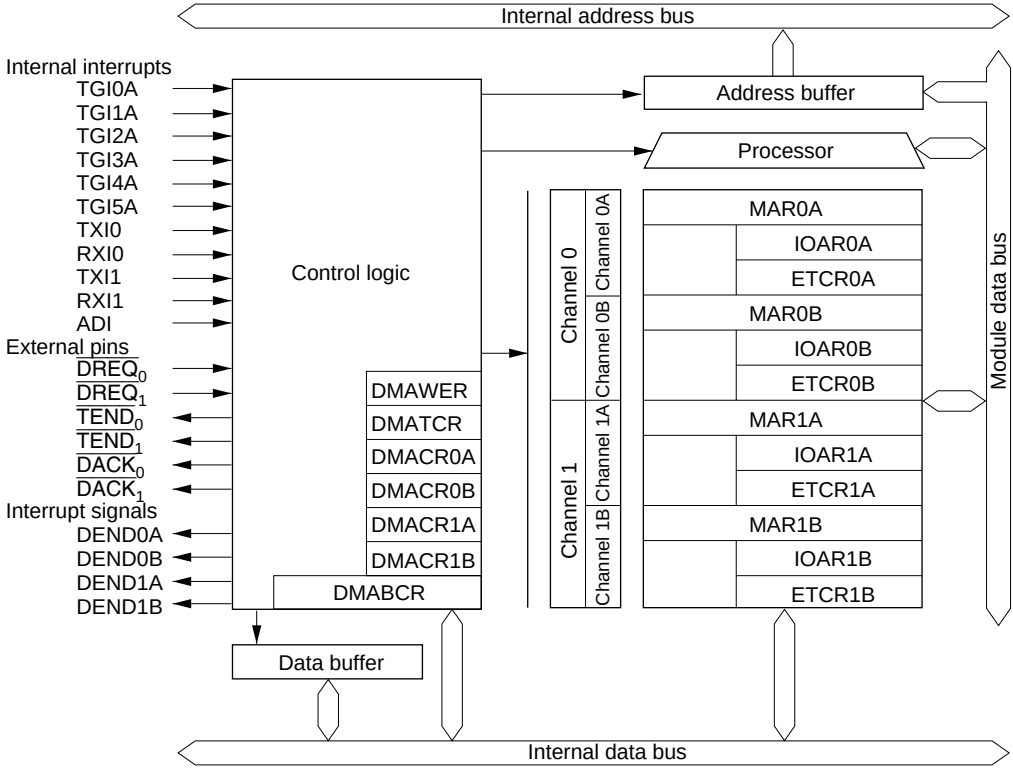
Name	Symbol	I/O	Function
Nonmaskable interrupt	NMI	Input	Nonmaskable external interrupt; rising or falling edge can be selected
External interrupt requests 7 to 0	$\overline{IRQ}_7$ to $\overline{IRQ}_0$	Input	Maskable external interrupts; rising, falling, or both edges, or level sensing, can be selected

6.2 DMA Controller

6.2.1 Features

- Selection of short address mode or full address mode
- 16-Mbyte address space can be specified directly
- Byte or word can be set as the transfer unit
- Activation sources: internal interrupt, external request, auto-request (depending on transfer mode)
- Module stop mode can be set

6.2.2 Block Diagram



Legend

DMAWER:	DMA write enable register
DMATCR:	DMA terminal control register
DMABCR:	DMA band control register (for all channels)
DMACR:	DMA control register
MAR:	Memory address register
IOAR:	I/O address register
ETCR:	Execute transfer counter register

Figure 6.2 Block Diagram of DMAC

6.2.3 Pins

Table 6.2 DMAC Pins

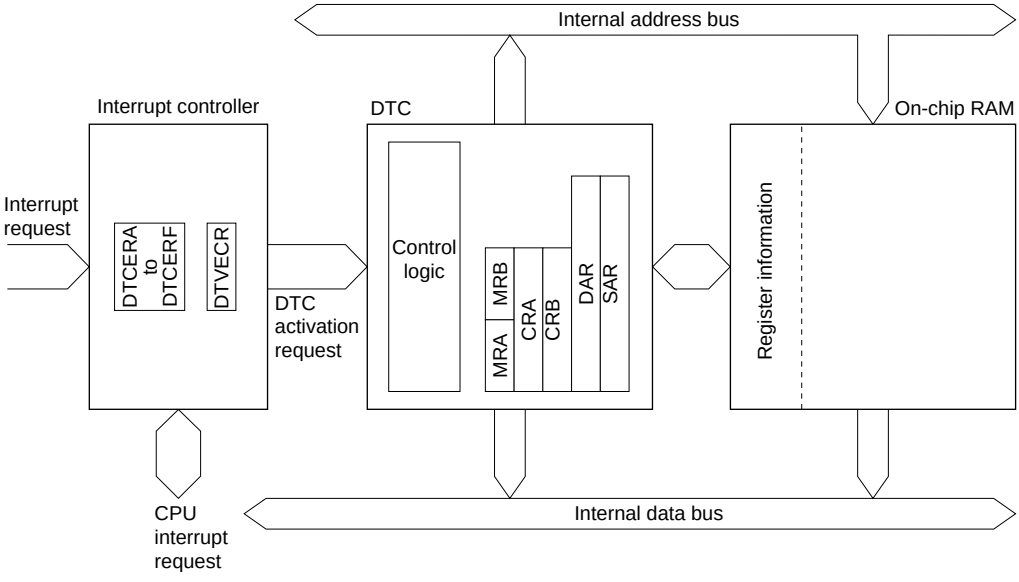
Channel	Name	Symbol	I/O	Function
0	DMA request 0	$\overline{DREQ_0}$	Input	DMAC channel 0 external request
	DMA transfer acknowledge 0	$\overline{DACK_0}$	Output	DMAC channel 0 single address transfer acknowledge
	DMA transfer end 0	$\overline{TEND_0}$	Output	DMAC channel 0 transfer end
1	DMA request 1	$\overline{DREQ_1}$	Output	DMAC channel 1 external request
	DMA transfer acknowledge 1	$\overline{DACK_1}$	Output	DMAC channel 1 single address transfer acknowledge
	DMA transfer end 1	$\overline{TEND_1}$	Output	DMAC channel 1 transfer end

6.3 Data Transfer Controller

6.3.1 Features

- Transfer possible over any number of channels
- Variety of transfer modes, including normal, repeat, and block transfer
- Direct specification of 16-Mbyte address space possible
- Byte or word can be selected as the transfer unit
- A CPU interrupt can be requested for an interrupt that activates the DTC
- Can be activated by software
- Module stop mode can be set
- DTC register information is located in on-chip RAM

6.3.2 Block Diagram



Legend

MRA, MRB:	DTC mode registers A and B
CRA, CRB:	DTC transfer count registers A and B
SAR:	DTC source address register
DAR:	DTC destination address register
DTCERA to DTCERF:	DTC enable registers A to F
DTVECR:	DTC vector register

Note: The RAME bit in SYSCR must be set to 1 when the DTC is used.

Figure 6.3 Block Diagram of DTC

6.4 16-Bit Timer Pulse Unit

6.4.1 Features

- Comprises six 16-bit timer channels
- Maximum 16 pulse inputs/outputs
- Selection of 8 counter input clocks for each channel
- Compare match, input capture, counter clear operation, synchronous operation, and PWM mode can be set for each channel
- Buffer operation can be set for channels 0 and 3
- Phase counting mode can be set independently for each of channels 1, 2, 4, and 5
- Cascaded operation possible by connecting two 16-bit counter channels to form a 32-bit counter
- Fast access via internal 16-bit bus
- Programmable pulse generator (PPG) output trigger can be generated
- A/D converter conversion start trigger can be generated
- Module stop mode can be set

6.4.2 Block Diagram

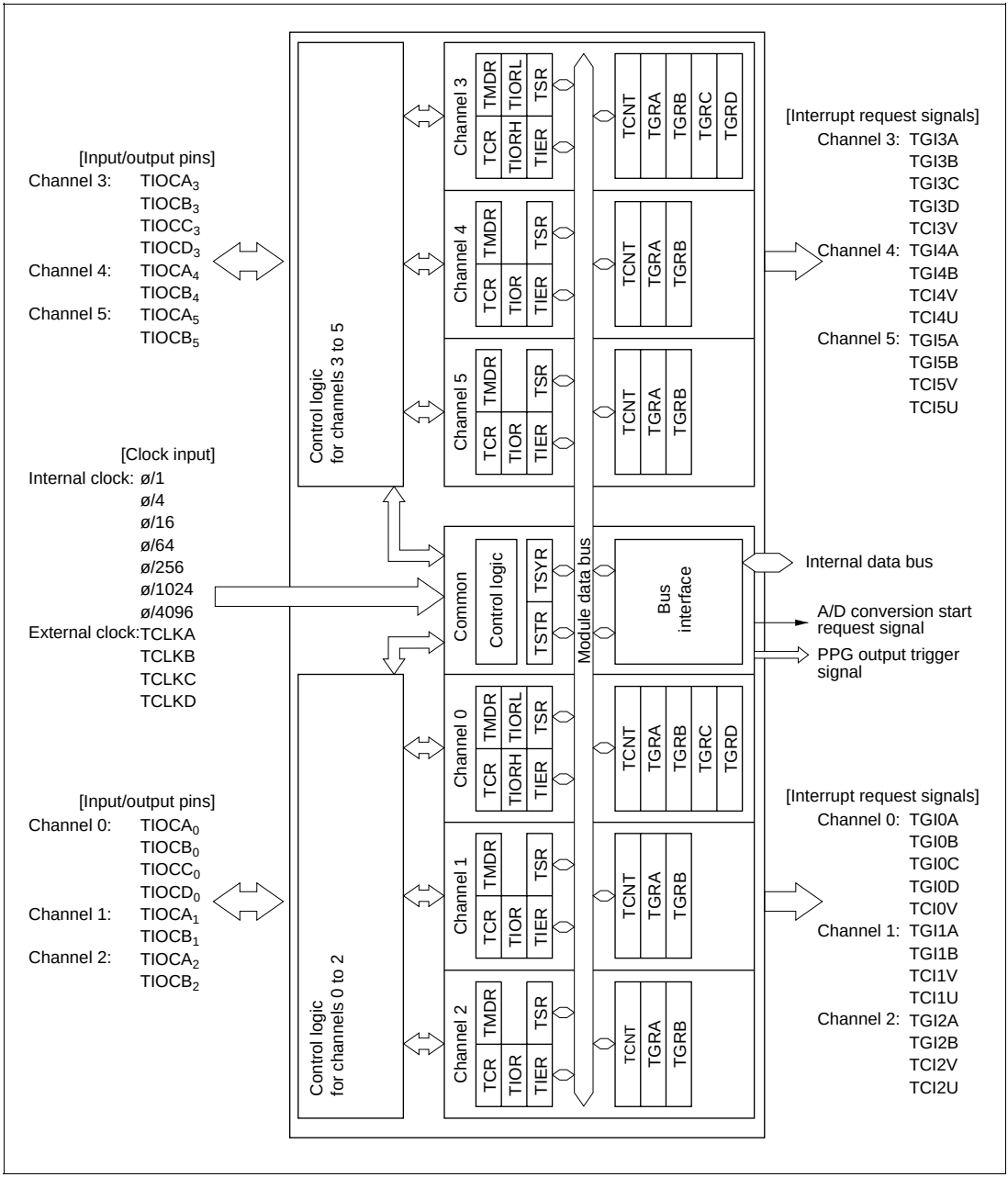


Figure 6.4 Block Diagram of TPU

6.4.3 Pins

Table 6.3 TPU Pins

Channel	Name	Symbol	I/O	Function
All	Clock input A	TCLKA	Input	External clock A input pin (Channel 1 and 5 phase counting mode A-phase input)
	Clock input B	TCLKB	Input	External clock B input pin (Channel 1 and 5 phase counting mode B-phase input)
	Clock input C	TCLKC	Input	External clock C input pin (Channel 2 and 4 phase counting mode A-phase input)
	Clock input D	TCLKD	Input	External clock D input pin (Channel 2 and 4 phase counting mode B-phase input)
0	Input capture/out compare match A0	$TIOCA_0$	I/O	TGR0A input capture input/output compare output/PWM output pin
	Input capture/out compare match B0	$TIOCB_0$	I/O	TGR0B input capture input/output compare output/PWM output pin
	Input capture/out compare match C0	$TIOCC_0$	I/O	TGR0C input capture input/output compare output/PWM output pin
	Input capture/out compare match D0	$TIOCD_0$	I/O	TGR0D input capture input/output compare output/PWM output pin
1	Input capture/out compare match A1	$TIOCA_1$	I/O	TGR1A input capture input/output compare output/PWM output pin
	Input capture/out compare match B1	$TIOCB_1$	I/O	TGR1B input capture input/output compare output/PWM output pin
2	Input capture/out compare match A2	$TIOCA_2$	I/O	TGR2A input capture input/output compare output/PWM output pin
	Input capture/out compare match B2	$TIOCB_2$	I/O	TGR2B input capture input/output compare output/PWM output pin
3	Input capture/out compare match A3	$TIOCA_3$	I/O	TGR3A input capture input/output compare output/PWM output pin
	Input capture/out compare match B3	$TIOCB_3$	I/O	TGR3B input capture input/output compare output/PWM output pin
	Input capture/out compare match C3	$TIOCC_3$	I/O	TGR3C input capture input/output compare output/PWM output pin
	Input capture/out compare match D3	$TIOCD_3$	I/O	TGR3D input capture input/output compare output/PWM output pin

Channel	Name	Symbol	I/O	Function
4	Input capture/out compare match A4	$TIOCA_4$	I/O	TGR4A input capture input/output compare output/PWM output pin
	Input capture/out compare match B4	$TIOCB_4$	I/O	TGR4B input capture input/output compare output/PWM output pin
5	Input capture/out compare match A5	$TIOCA_5$	I/O	TGR5A input capture input/output compare output/PWM output pin
	Input capture/out compare match B5	$TIOCB_5$	I/O	TGR5B input capture input/output compare output/PWM output pin

6.5 Programmable Pulse Generator

6.5.1 Features

- Maximum 16-bit data output capability
- Up to four different 4-bit outputs
- Output trigger signals can be selected
- Non-overlap margin can be set
- Can operate together with the data transfer controller (DTC) and DMA controller (DMAC)
- Inverse output can be selected
- Module stop mode can be set

6.5.2 Block Diagram

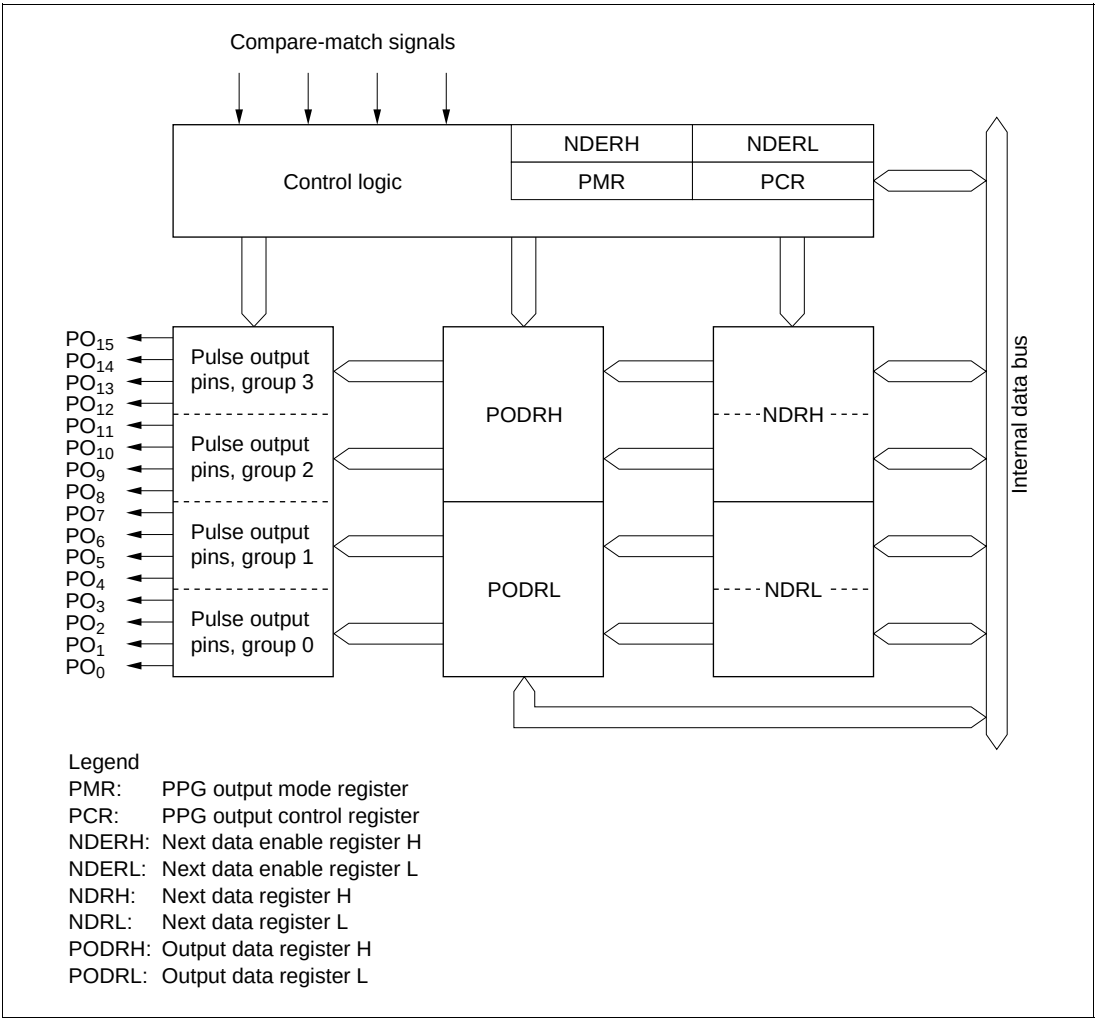


Figure 6.5 Block Diagram of PPG

6.5.3 Pins

Table 6.4 PPG Pins

Name	Symbol	I/O	Function
Pulse output 0	PO_0	Output	Group 0 pulse output
Pulse output 1	PO_1	Output	
Pulse output 2	PO_2	Output	
Pulse output 3	PO_3	Output	
Pulse output 4	PO_4	Output	Group 1 pulse output
Pulse output 5	PO_5	Output	
Pulse output 6	PO_6	Output	
Pulse output 7	PO_7	Output	
Pulse output 8	PO_8	Output	Group 2 pulse output
Pulse output 9	PO_9	Output	
Pulse output 10	PO_{10}	Output	
Pulse output 11	PO_{11}	Output	
Pulse output 12	PO_{12}	Output	Group 3 pulse output
Pulse output 13	PO_{13}	Output	
Pulse output 14	PO_{14}	Output	
Pulse output 15	PO_{15}	Output	

6.6 8-Bit Timer

6.6.1 Features

- Two-channel timer using 8-bit counters as base
- Selection of four counter input clocks
- Counter clearing can be specified
- Timer output by combination of two compare match signals
- Cascaded operation possible by connecting both counter channels to form a 16-bit counter
- Three interrupt sources for each channel
- A/D converter conversion start trigger can be generated
- Module stop mode can be set

6.6.2 Block Diagram

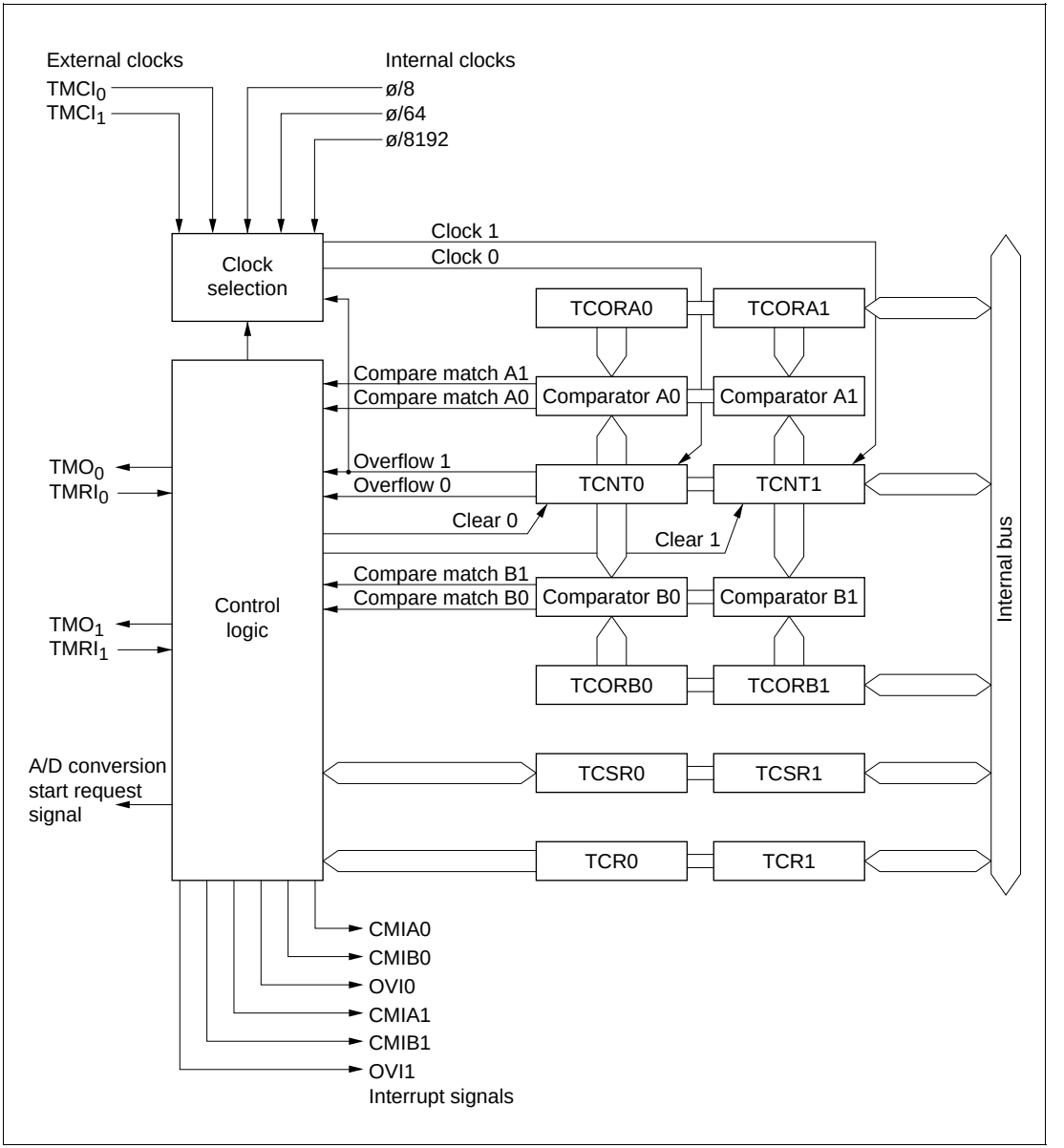


Figure 6.6 Block Diagram of 8-Bit Timer

6.6.3 Pins

Table 6.5 8-Bit Timer Pins

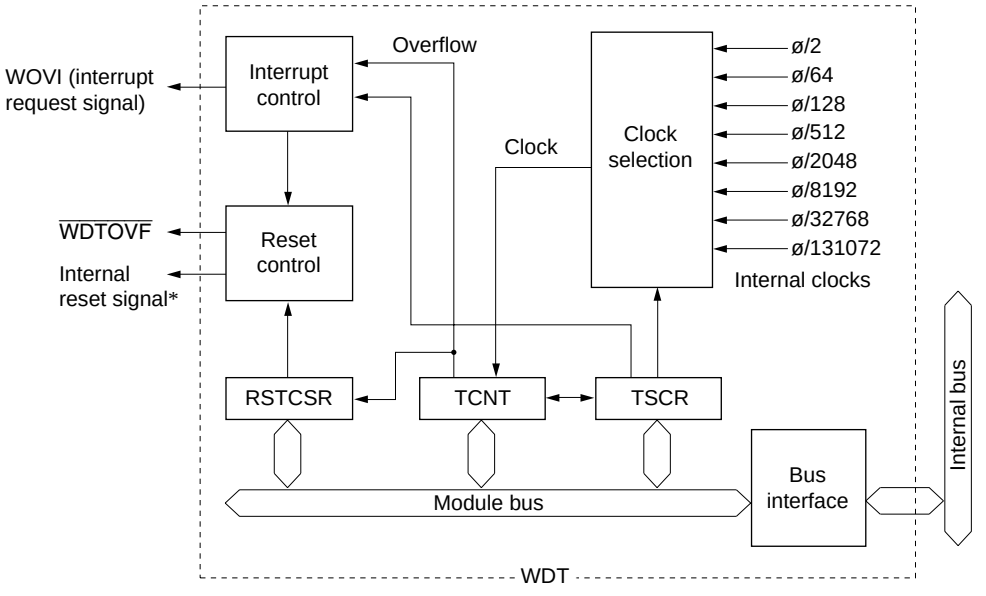
Channel	Name	Symbol	I/O	Function
0	Timer output pin 0	TMO_0	Output	Compare match output
	Timer clock input pin 0	$TMCI_0$	Input	Counter external clock input
	Timer reset input pin 0	$TMRI_0$	Input	Counter external reset input
1	Timer output pin 1	TMO_1	Output	Compare match output
	Timer clock input pin 1	$TMCI_1$	Input	Counter external clock input
	Timer reset input pin 1	$TMRI_1$	Input	Counter external reset input

6.7 Watchdog Timer

6.7.1 Features

- Switchable between watchdog timer mode and interval timer mode
- $\overline{\text{WDTOVF}}$ output in watchdog timer mode
- Interrupt generation when counter overflows in interval timer mode
- Selection of eight counter input clocks

6.7.2 Block Diagram



Legend
TCSR: Timer control/status register
TCNT: Timer counter
RSTCSR: Reset control/status register

Note: * The internal reset signal can be generated by means of a register setting.

Figure 6.7 Block Diagram of WDT

6.7.3 Pins

Table 6.6 WDT Pin

Name	Symbol	I/O	Function
Watchdog timer overflow	$\overline{\text{WDTOVF}}$	Output	Outputs counter overflow signal in watchdog timer mode

6.8 Serial Communication Interface

6.8.1 Features

- Three independent on-chip channels in the H8S/2339 and H8S/2338 Series
- Selection of synchronous or asynchronous serial communication mode
- Full-duplex communication capability
- Selection of LSB-first or MSB-first transfer
- Built-in baud rate generator allows any bit rate to be selected
- Selection of transmit/receive clock source
- DTC and DMAC can be activated by 4 interrupts (ERI, RXI, TXI, and TEI)
- Module stop mode can be set

6.8.2 Block Diagram

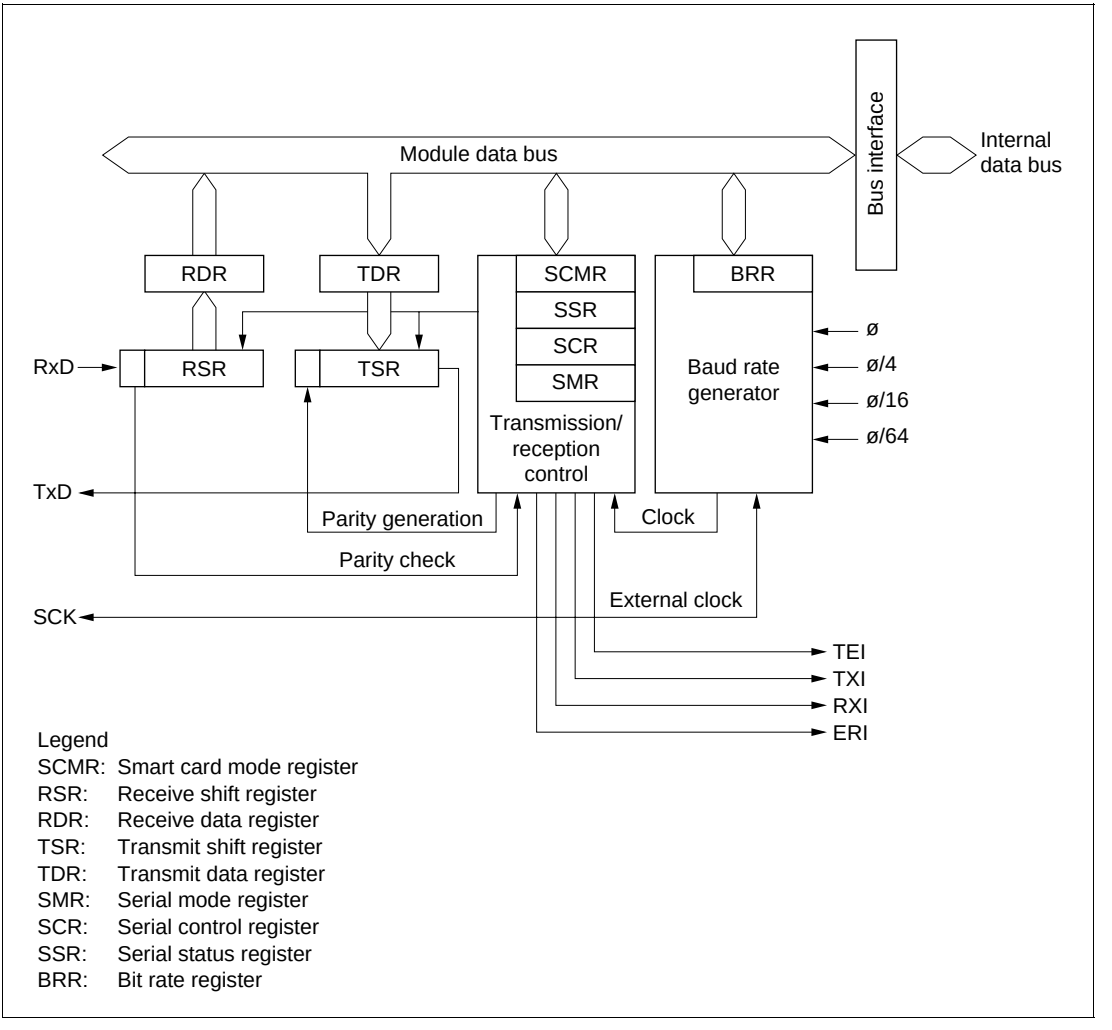


Figure 6.8 Block Diagram of SCI

6.8.3 Pins

Table 6.7 SCI Pins

Channel	Name	Symbol	I/O	Function
0	Serial clock pin	SCK_0	I/O	SCI0 clock input/output
	Receive data pin	RxD_0	Input	SCI0 receive data input
	Transmit data pin	TxD_0	Output	SCI0 transmit data output
1	Serial clock pin	SCK_1	I/O	SCI1 clock input/output
	Receive data pin	RxD_1	Input	SCI1 receive data input
	Transmit data pin	TxD_1	Output	SCI1 transmit data output
2	Serial clock pin	SCK_2	I/O	SCI2 clock input/output
	Receive data pin	RxD_2	Input	SCI2 receive data input
	Transmit data pin	TxD_2	Output	SCI2 transmit data output

6.9 Smart Card Interface

6.9.1 Features

- IC card interface conforming to ISO/IEC7816-3 supported as SCI extension function
- Switching between normal SCI and smart card interface by means of register setting
- Built-in baud rate generator allows any bit rate to be selected
- DTC and DMAC can be activated by 3 interrupts (TXI, RXI, and ERI)

6.9.2 Block Diagram

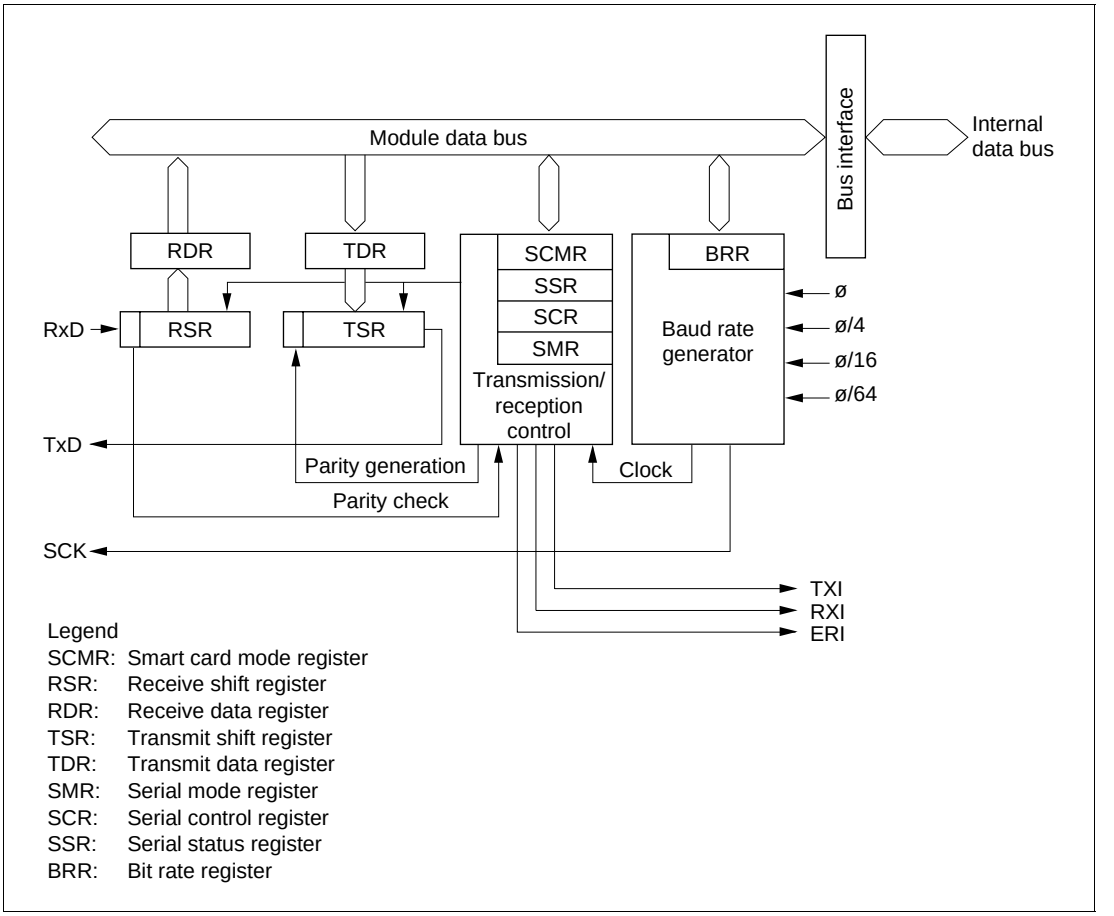


Figure 6.9 Block Diagram of Smart Card Interface

6.9.3 Pins

Table 6.8 Smart Card Interface Pins

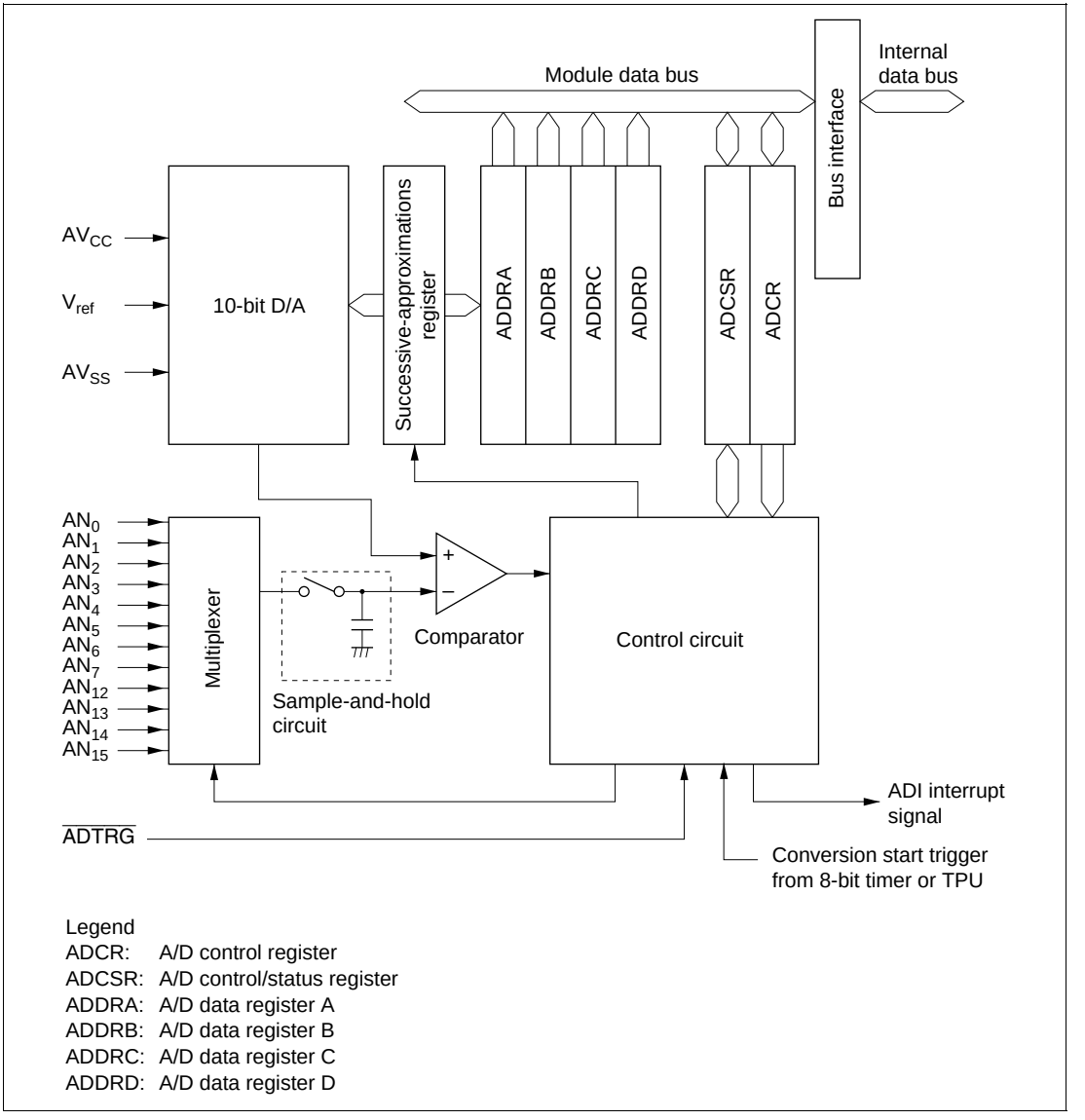
Channel	Name	Symbol	I/O	Function
0	Serial clock pin	SCK_0	I/O	SCI0 clock input/output
	Receive data pin	RxD_0	Input	SCI0 receive data input
	Transmit data pin	TxD_0	Output	SCI0 transmit data output
1	Serial clock pin	SCK_1	I/O	SCI1 clock input/output
	Receive data pin	RxD_1	Input	SCI1 receive data input
	Transmit data pin	TxD_1	Output	SCI1 transmit data output
2	Serial clock pin	SCK_2	I/O	SCI2 clock input/output
	Receive data pin	RxD_2	Input	SCI2 receive data input
	Transmit data pin	TxD_2	Output	SCI2 transmit data output

6.10 A/D Converter

6.10.1 Features

- 10-bit resolution
- 12 input channels
- Settable analog conversion voltage range
- Conversion time: 6.7 µs per channel (at 20 MHz operation)
- Selection of single mode or scan mode as operating mode
- Four data registers
- Sample-and-hold function
- Three kinds of conversion start (software, timer conversion start trigger, or $\overline{\text{ADTRG}}$ pin)
- A/D conversion end interrupt request generation
- Module stop mode can be set

6.10.2 Block Diagram



Legend
ADCR: A/D control register
ADCSR: A/D control/status register
ADDRA: A/D data register A
ADDRB: A/D data register B
ADDRC: A/D data register C
ADDRD: A/D data register D

Figure 6.10 Block Diagram of A/D Converter

6.10.3 Pins

Table 6.9 A/D Converter Pins

Name	Symbol	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog circuit power supply
Analog ground pin	AV_{SS}	Input	Analog circuit ground and reference voltage
Reference voltage pin	V_{ref}	Input	A/D conversion reference voltage
Analog input pin 0	AN_0	Input	Channel set 0 (CH3 = 1) group 0 analog input
Analog input pin 1	AN_1	Input	
Analog input pin 2	AN_2	Input	
Analog input pin 3	AN_3	Input	
Analog input pin 4	AN_4	Input	Channel set 1 (CH3 = 0) group 1 analog input
Analog input pin 5	AN_5	Input	
Analog input pin 6	AN_6	Input	
Analog input pin 7	AN_7	Input	
Analog input pin 12	AN_{12}	Input	Channel set 1 (CH3 = 0) group 1 analog input
Analog input pin 13	AN_{13}	Input	
Analog input pin 14	AN_{14}	Input	
Analog input pin 15	AN_{15}	Input	
A/D external trigger input pin	$\overline{ADTRG}$	Input	External trigger for starting A/D conversion

6.11 D/A Converter

6.11.1 Features

- 8-bit resolution
- Four output channels
- Maximum conversion time of 10 µs (with 20 pF capacitive load)
- Output voltage of 0 V to Vref
- D/A output hold function in software standby mode
- Module stop mode can be set

6.11.2 Block Diagram

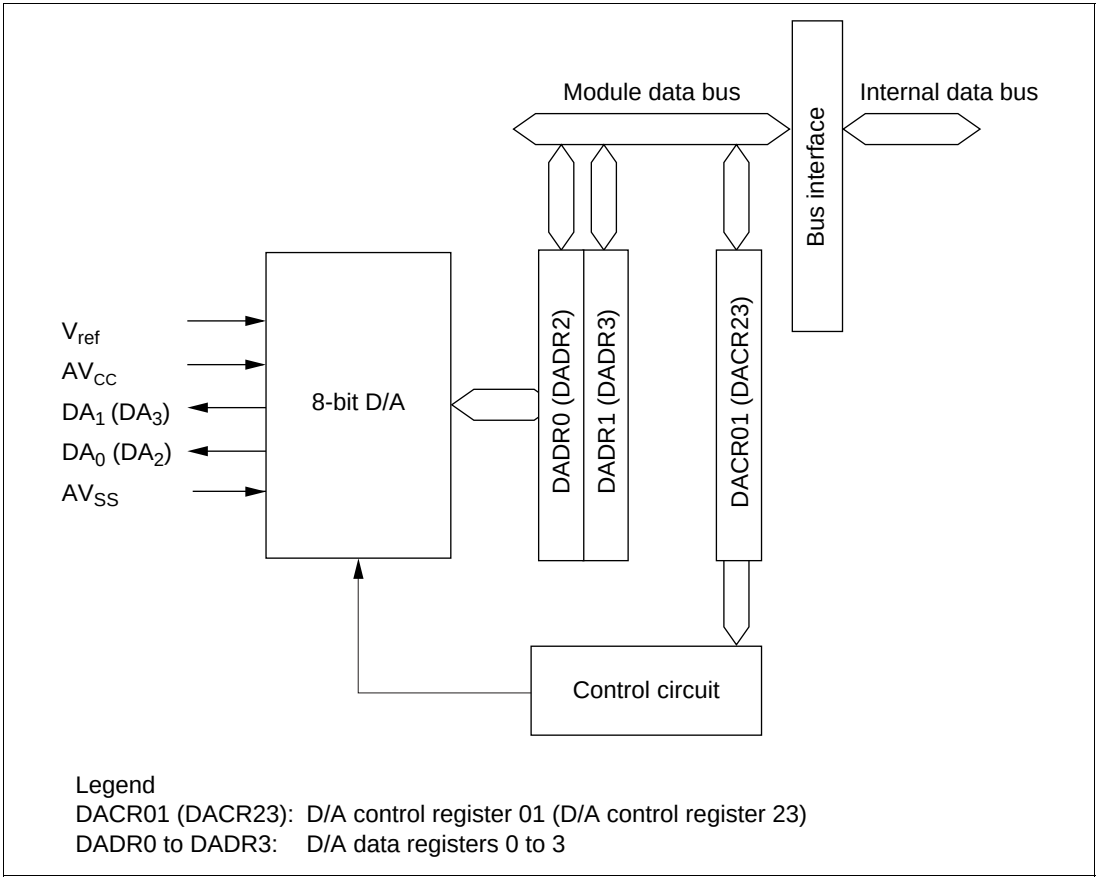


Figure 6.11 Block Diagram of D/A Converter

6.11.3 Pins

Table 6.10 D/A Converter Pins

Name	Symbol	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog circuit power supply
Analog ground pin	AV_{SS}	Input	Analog circuit ground and reference voltage
Analog output pin 0	DA_0	Output	Channel 0 analog output
Analog output pin 1	DA_1	Output	Channel 1 analog output
Analog output pin 2	DA_2	Output	Channel 2 analog output
Analog output pin 3	DA_3	Output	Channel 3 analog output
Reference voltage pin	V_{ref}	Input	Analog circuit reference voltage

6.12 RAM (H8S/2339)

6.12.1 Features

- 32 kbytes of on-chip high-speed static RAM
- Connected to the CPU by a 16-bit data bus, enabling one-state access to both byte data and word data
- Can be enabled or disabled by means of the RAM enable bit (RAME) in the system control register (SYSCR)

6.12.2 Block Diagram

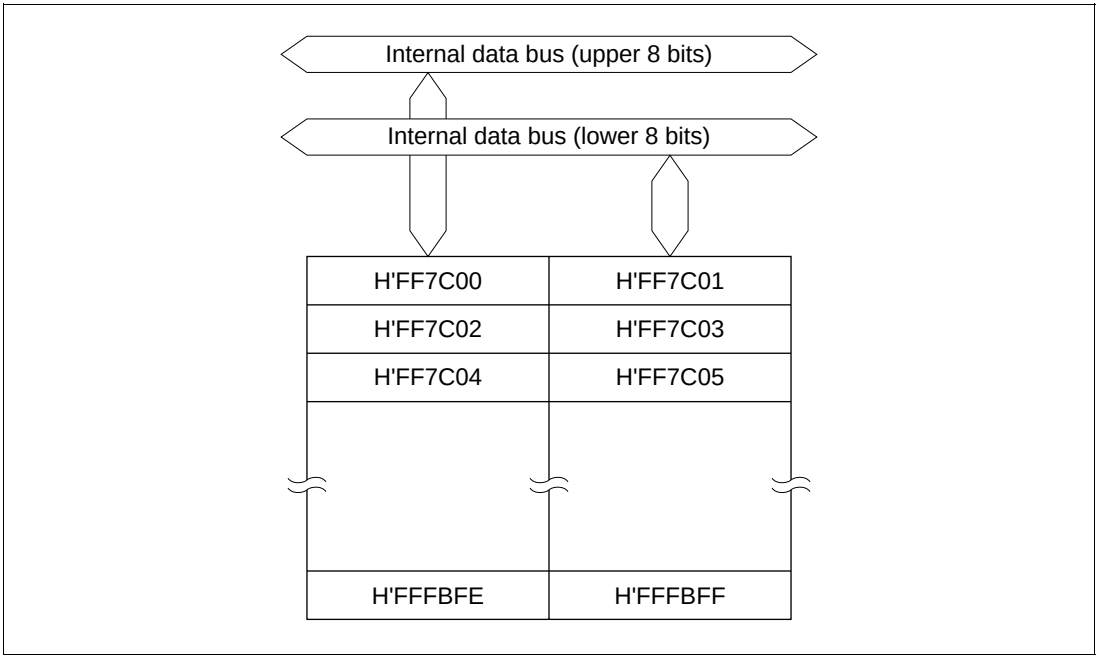


Figure 6.12 Block Diagram of RAM (32 kbytes)

6.13 RAM (H8S/2338, H8S/2337, H8S/2332)

6.13.1 Features

- Eight kbytes of on-chip high-speed static RAM
- Connected to the CPU by a 16-bit data bus, enabling one-state access to both byte data and word data
- Can be enabled or disabled by means of the RAM enable bit (RAME) in the system control register (SYSCR)

6.13.2 Block Diagram

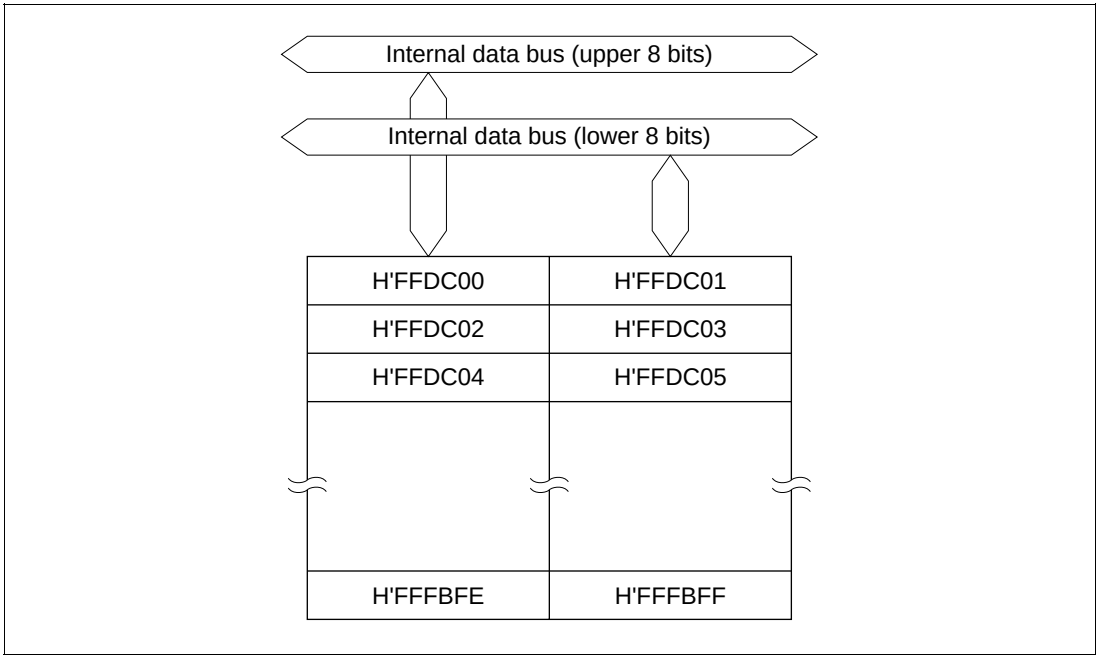


Figure 6.13 Block Diagram of RAM (8 kbytes)

6.14 ROM (H8S/2339)

6.14.1 Features

- Connected to the bus master by a 16-bit data bus, enabling one-state access to both byte data and word data
- The flash memory version (H8S/2339 F-ZTAT™) can be erased and programmed with a PROM programmer, as well as on-board

6.14.2 Block Diagrams

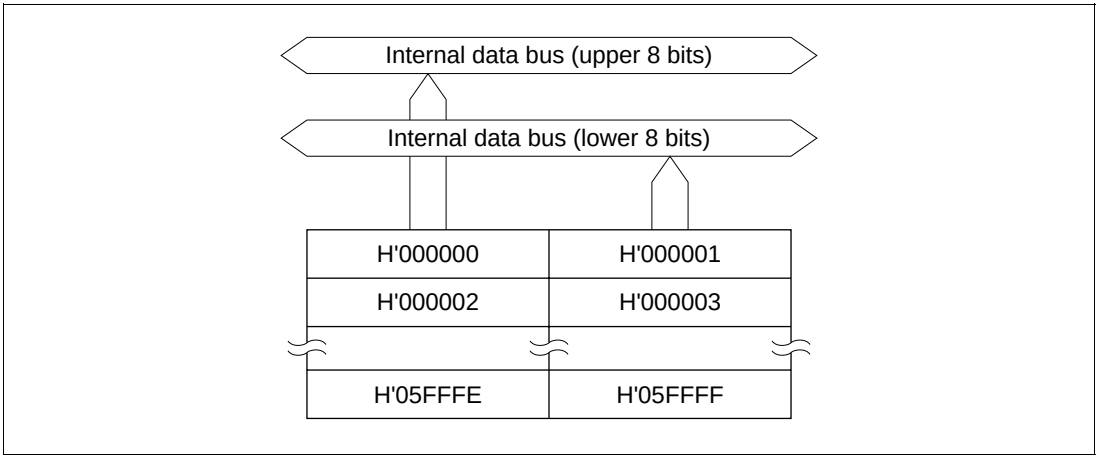
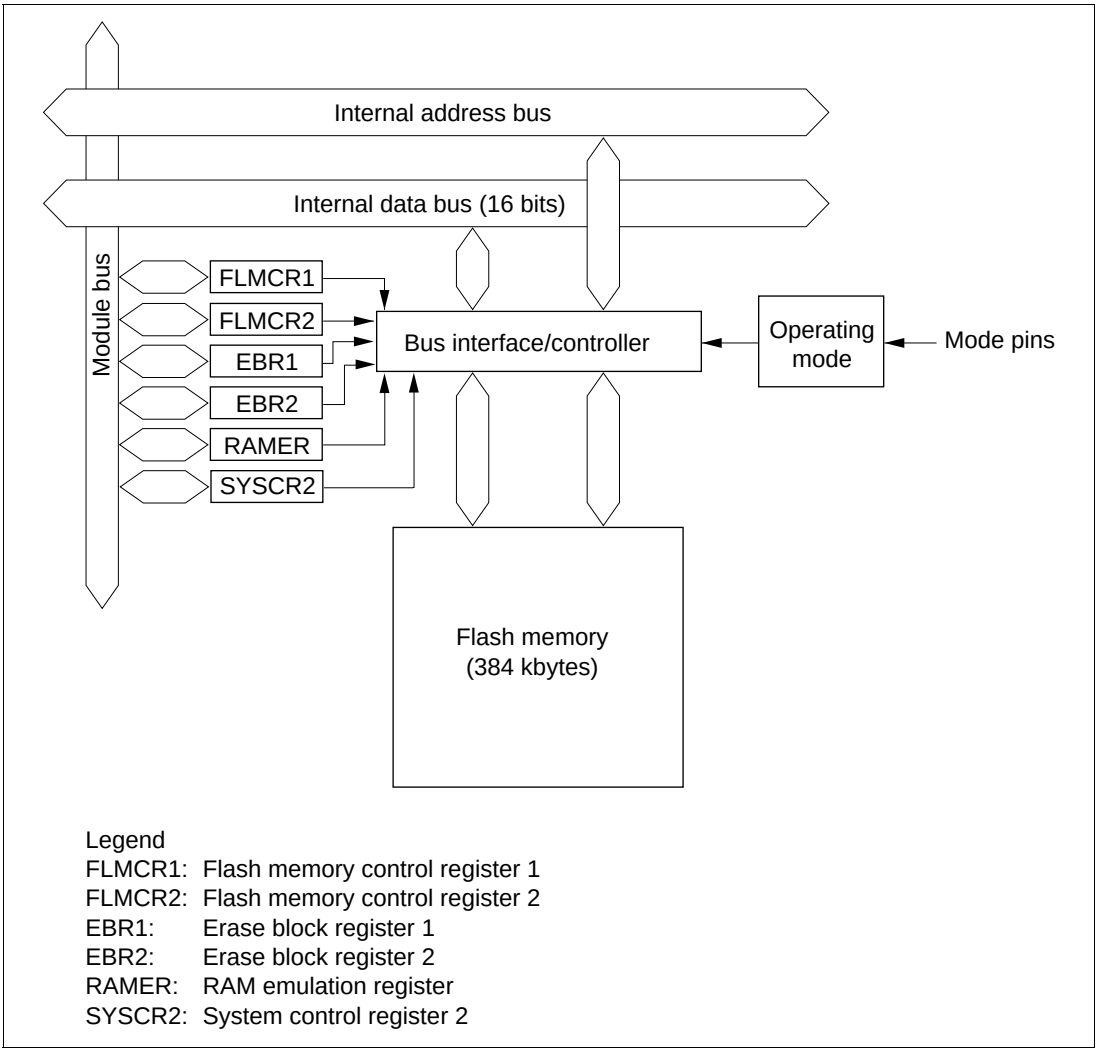


Figure 6.14 Block Diagram of Flash Memory (384 kbytes)



Legend
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2
RAMER: RAM emulation register
SYSCR2: System control register 2

Figure 6.15 Block Diagram of Flash Memory

6.15 ROM (H8S/2338, H8S/2337)

6.15.1 Features

- Connected to the bus master by a 16-bit data bus, enabling one-state access to both byte data and word data
- The flash memory version (H8S/2338 F-ZTAT™) can be erased and programmed with a PROM programmer, as well as on-board
- The H8S/2338 has 256 kbytes, and the H8S/2337 has 128 kbytes, of on-chip mask ROM

6.15.2 Block Diagrams

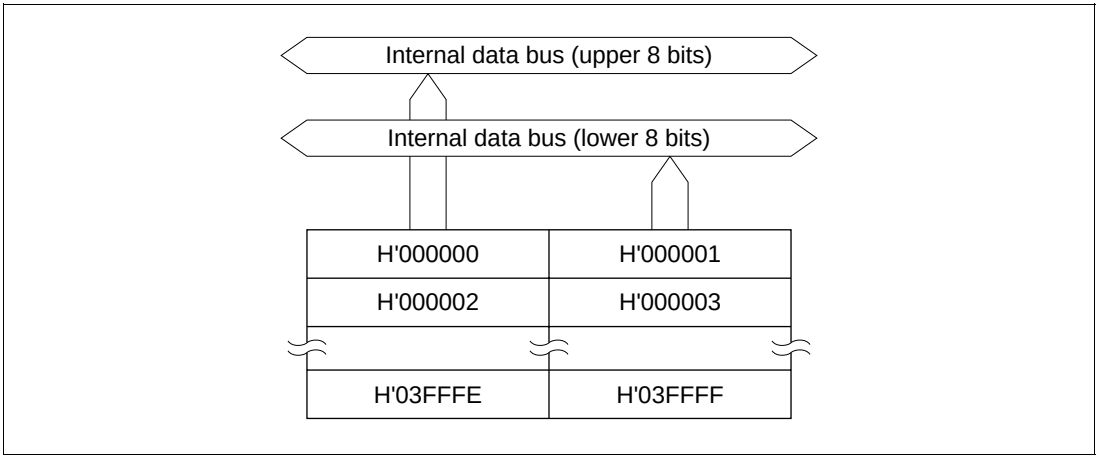
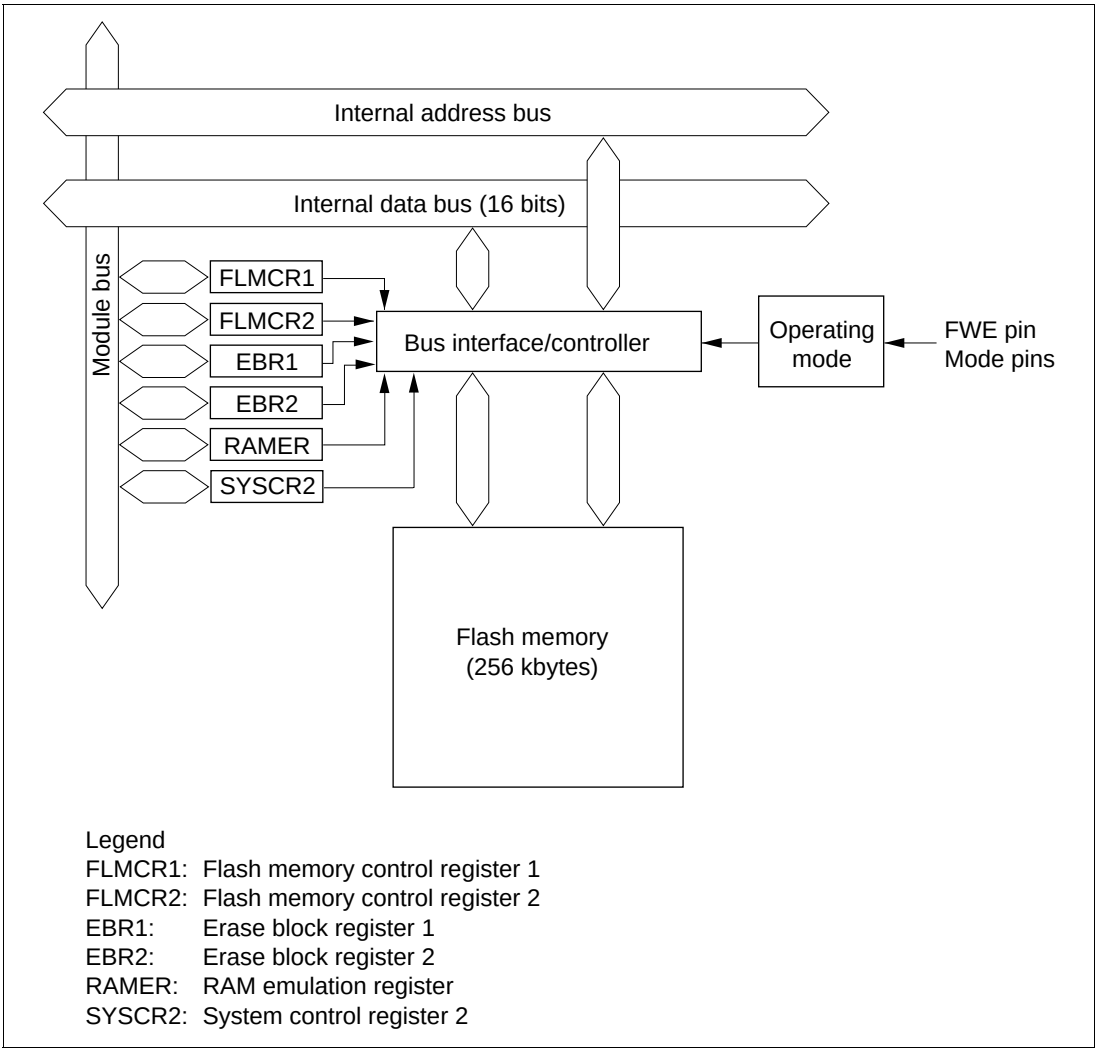


Figure 6.16 Block Diagram of Flash Memory (256 kbytes)



Legend
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2
RAMER: RAM emulation register
SYSCR2: System control register 2

Figure 6.17 Block Diagram of Flash Memory

6.16 Clock Pulse Generator

6.16.1 Features

- Comprises an oscillator, duty correction circuit, medium-speed clock divider, and bus master clock selection circuit
- Generates system clock (ø), bus master clock, and internal clock
- Allows switching between medium-speed mode and variable clock division function

6.16.2 Block Diagram

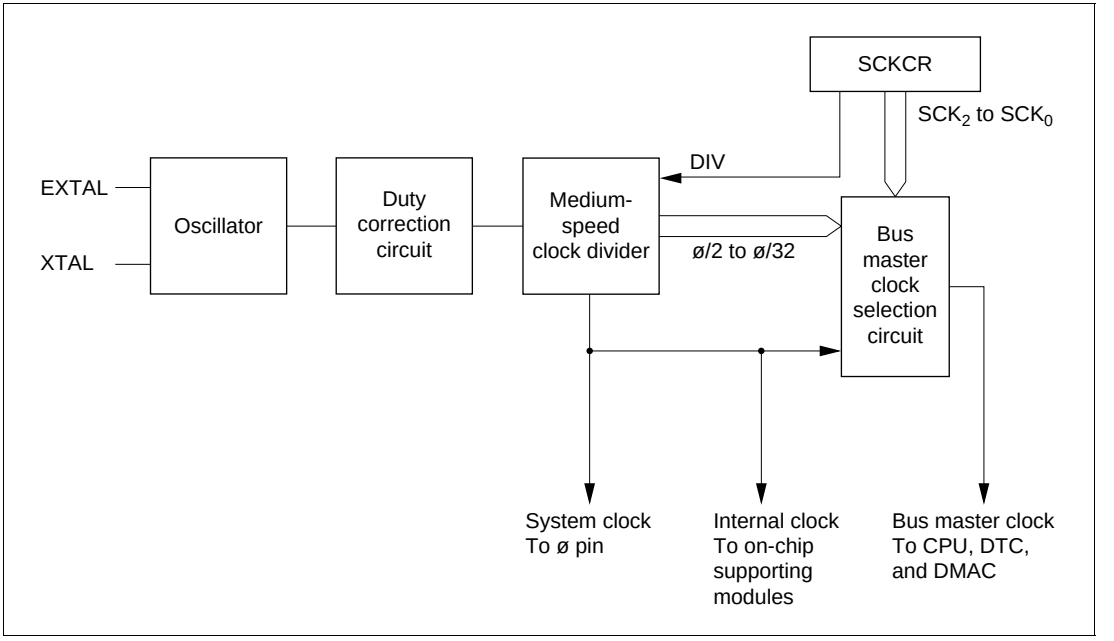


Figure 6.18 Block Diagram of Clock Pulse Generator

Section 7 Electrical Characteristics

For electrical characteristics of the H8S/2339 F-ZTAT version, please contact Hitachi's sales office.

7.1 Electrical Characteristics of Mask ROM Version (H8S/2338, H8S/2337) and ROMless Version (H8S/2332)

7.1.1 Absolute Maximum Ratings

Table 7.1 lists the absolute maximum ratings.

Table 7.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.6	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.6	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

7.1.2 DC Characteristics

Table 7.2 DC Characteristics

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, 7, 9	VT^-	$V_{CC} \times 0.2$	—	—	V	
	$P5_0$ to $P5_3$, $P6_4$ to $P6_7$	VT^+	—	—	$V_{CC} \times 0.7$	V	
	PA_4 to PA_7	$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, 8, B to G, $P5_4$ to $P5_7$, $P6_0$ to $P6_3$, PA_0 to PA_3		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 03	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, 8, B to G, $P5_4$ to $P5_7$, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD_2 to MD_0		—	—	1	µA	
	Port 4 $P5_4$ to $P5_7$		—	—	1	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Ports 1, 2, 3, 5, 6, 7 Ports 8, 9, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{in} = 0V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*2	Normal operation	I_{CC}*4	—	43 (3.0 V)	84	mA	f = 20 MHz
				58 (3.3 V)	105	mA	f = 25 MHz
	Sleep mode		—	34 (3.0 V)	66	mA	f = 20 MHz
				4.6 (3.3 V)	82	mA	f = 25 MHz
	Standby mode*3		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	2.4 (3.0 V)	6.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref},** and AV_{SS} pins open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.5$ V and $V_{IL\ max} = 0.5$ V with all output pins unloaded and all MOS input pull-ups in the off state.

3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.

4. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} max = 1.0 (mA) + 1.15 (mA/(MHz × V)) × V_{CC} × f (normal operation)

   I_{CC} max = 1.0 (mA) + 0.90 (mA/(MHz × V)) × V_{CC} × f (sleep mode)

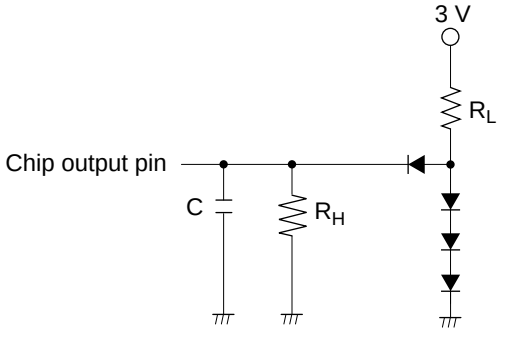
Table 7.3 Permissible Output Currents

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.3.

7.1.3 AC Characteristics



C = 50 pF: ports 1, A to F
C = 30 pF: ports 2, 3, 5 to 9, G

Input/output timing measurement level:
1.5 V (V_{CC} = 2.7 V to 3.6 V)

Figure 7.1 Output Load Circuit

(1) Clock Timing

Table 7.4 Clock Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}	50	500	40	500	ns	Figure 7.2
Clock pulse high width	t_{CH}	20	—	15	—	ns	
Clock pulse low width	t_{CL}	20	—	15	—	ns	
Clock rise time	t_{Cr}	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	5	—	5	ns	
Reset oscillation stabilization time (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 7.3
Software standby oscillation stabilization time (crystal)	t_{OSC2}	10	—	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	Figure 7.3

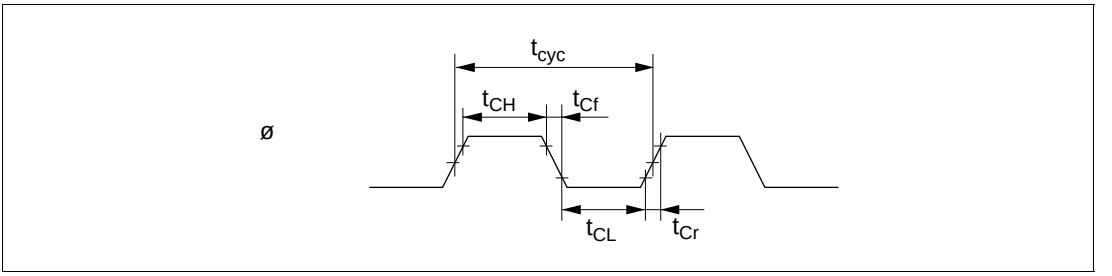


Figure 7.2 System Clock Timing

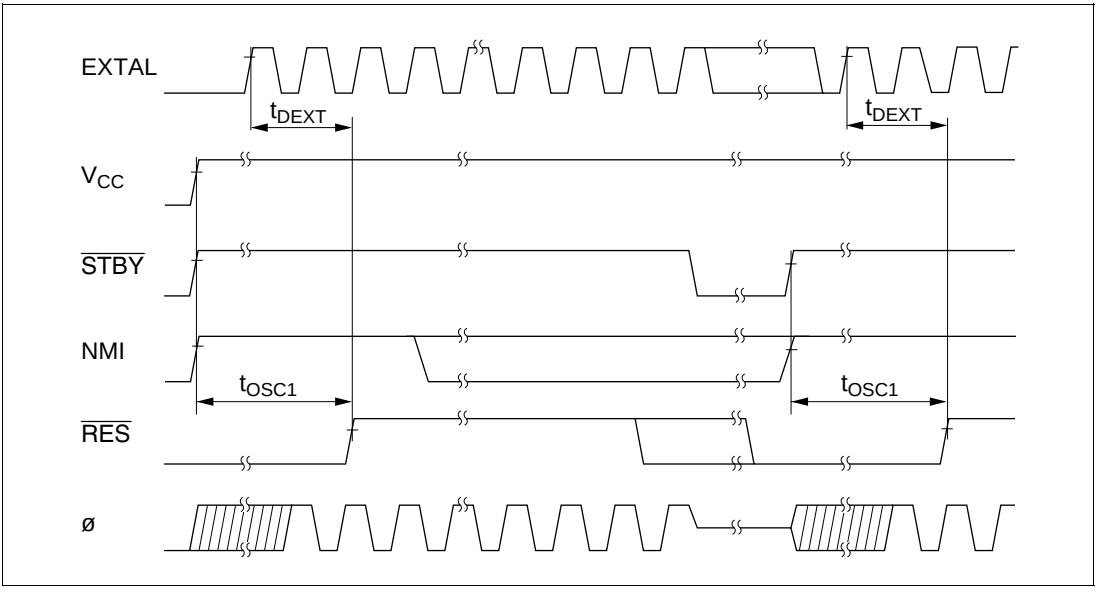


Figure 7.3 Oscillation Stabilization Timing

(2) Control Signal Timing

Table 7.5 Control Signal Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 7.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

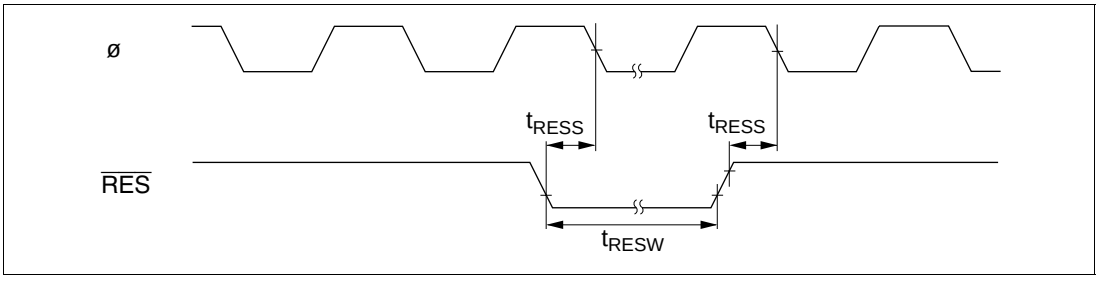


Figure 7.4 Reset Input Timing

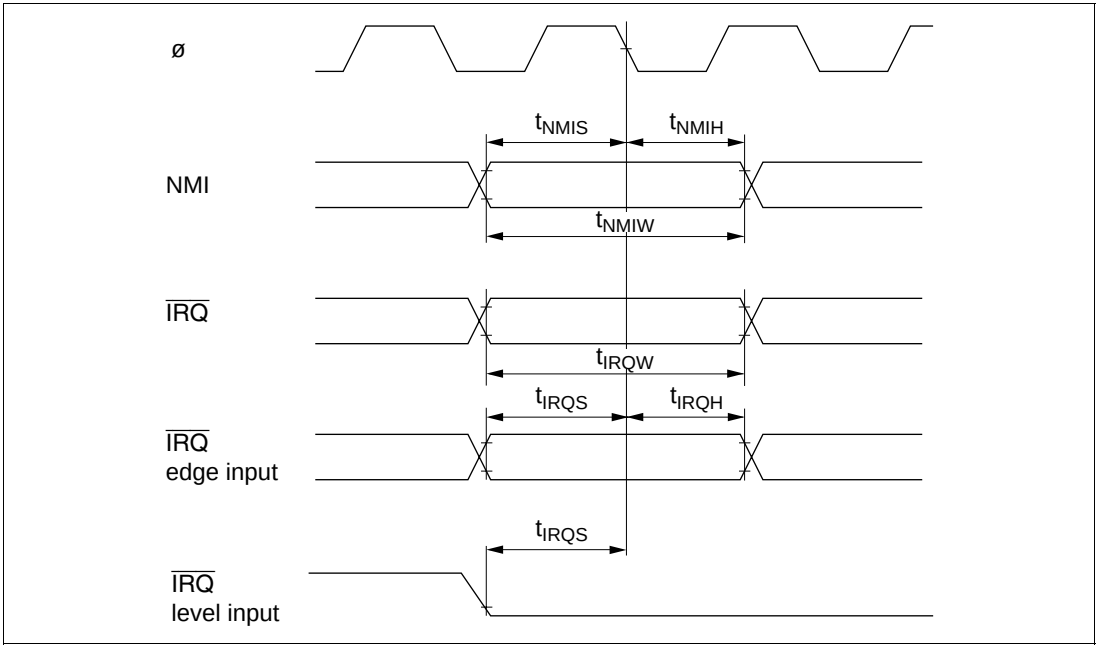


Figure 7.5 Interrupt Input Timing

(3) Bus Timing

Table 7.6 Bus Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figures 7.6 to 7.13
Address setup time	t_{AS}	0.5 × t_{cyc} – 15	—	0.5 × t_{cyc} – 15	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	
Precharge time	t_{PCH}	1.5 × t_{cyc} – 20	—	1.5 × t_{cyc} – 15	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	—	15	ns	
$\overline{CS}$ delay time 3	t_{CSD3}	—	25	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
$\overline{CAS}$ delay time	t_{CASD}	—	20	—	15	ns	
Read data setup time	t_{RDS}	15	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} – 25	—	1.5 × t_{cyc} – 20	ns	
Read data access time 3	t_{ACC3}	—	2.0 × t_{cyc} – 25	—	2.0 × t_{cyc} – 20	ns	
Read data access time 4	t_{ACC4}	—	2.5 × t_{cyc} – 25	—	2.5 × t_{cyc} – 20	ns	
Read data access time 5	t_{ACC5}	—	3.0 × t_{cyc} – 25	—	3.0 × t_{cyc} – 20	ns	
Read data access time 6	t_{ACC6}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	—	15	ns	Figures 7.6 to 7.13
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	1.0 × t_{cyc} – 20	—	1.0 × t_{cyc} – 15	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	1.5 × t_{cyc} – 20	—	1.5 × t_{cyc} – 15	—	ns	
Write data delay time	t_{WDD}	—	30	—	20	ns	
Write data setup time	t_{WDS}	0.5 × t_{cyc} – 20	—	0.5 × t_{cyc} – 15	—	ns	
Write data hold time	t_{WDH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	
$\overline{WR}$ setup time	t_{WCS}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 10	—	ns	
$\overline{WR}$ hold time	t_{WCH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 10	—	ns	
$\overline{CAS}$ setup time	t_{CSR}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	Figure 7.10
$\overline{WAIT}$ setup time	t_{WTS}	30	—	25	—	ns	Figure 7.8
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	30	—	ns	Figure 7.14
$\overline{BACK}$ delay time	t_{BACD}	—	15	—	15	ns	
Bus floating time	t_{BZD}	—	50	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	—	25	ns	Figure 7.15

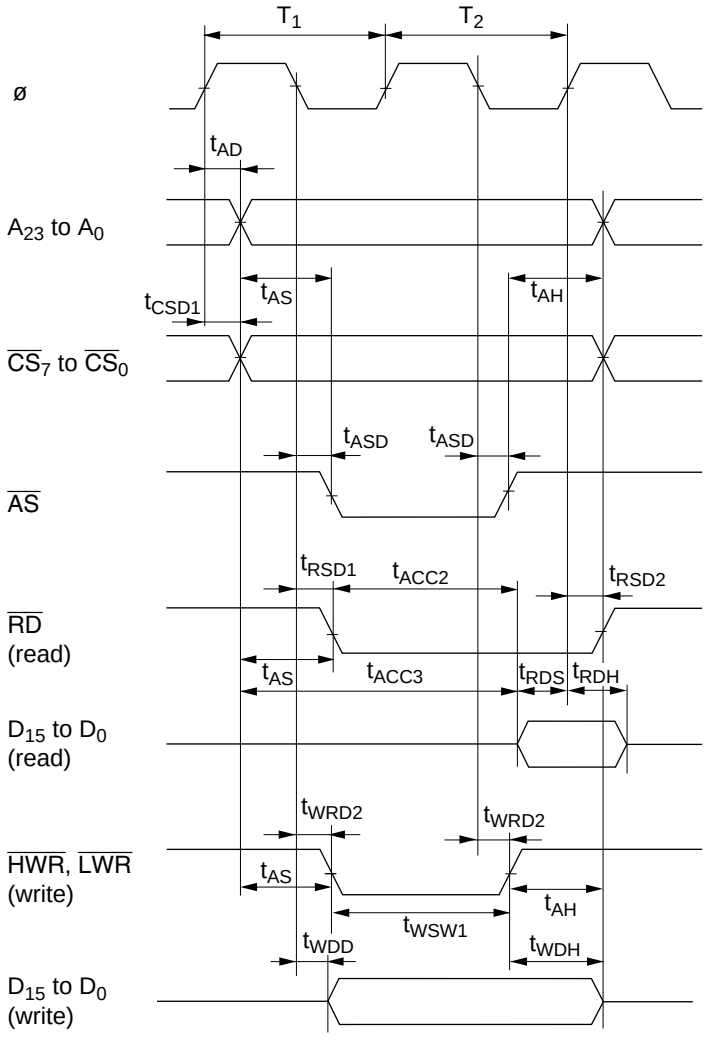


Figure 7.6 Basic Bus Timing (2-State Access)

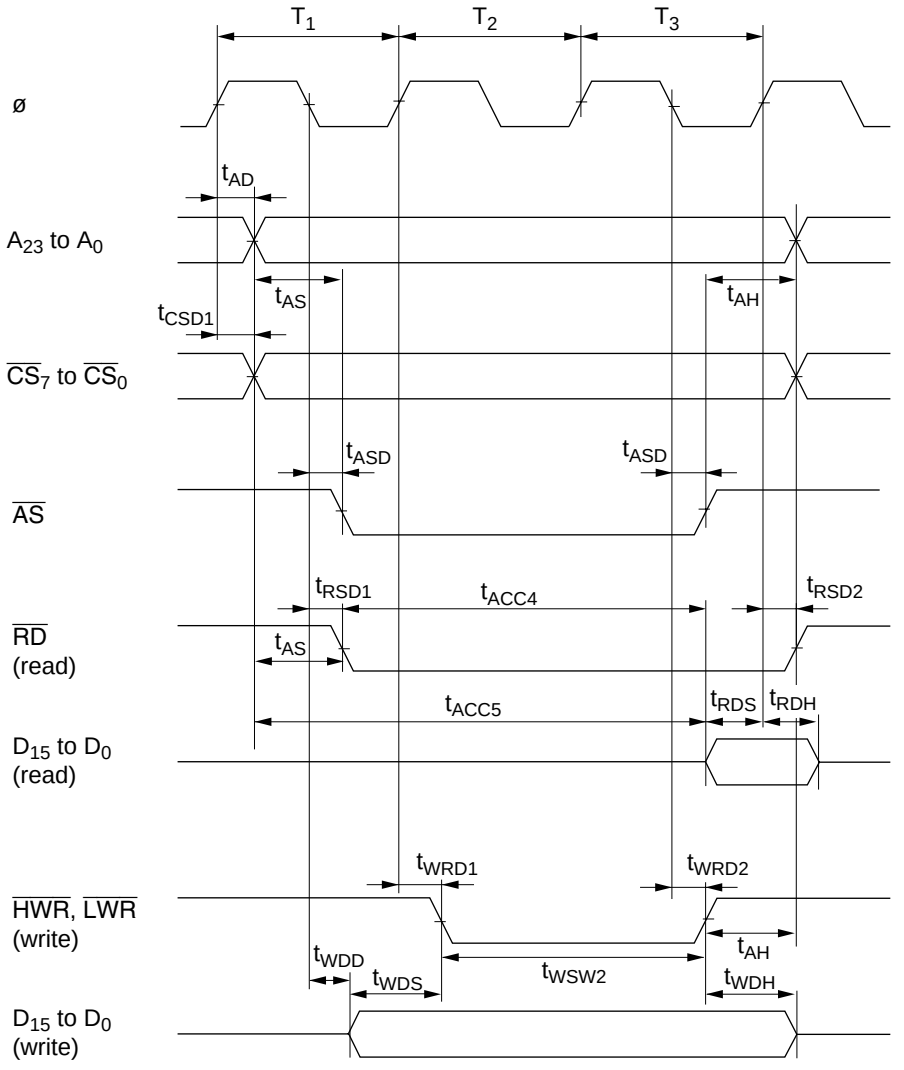


Figure 7.7 Basic Bus Timing (3-State Access)

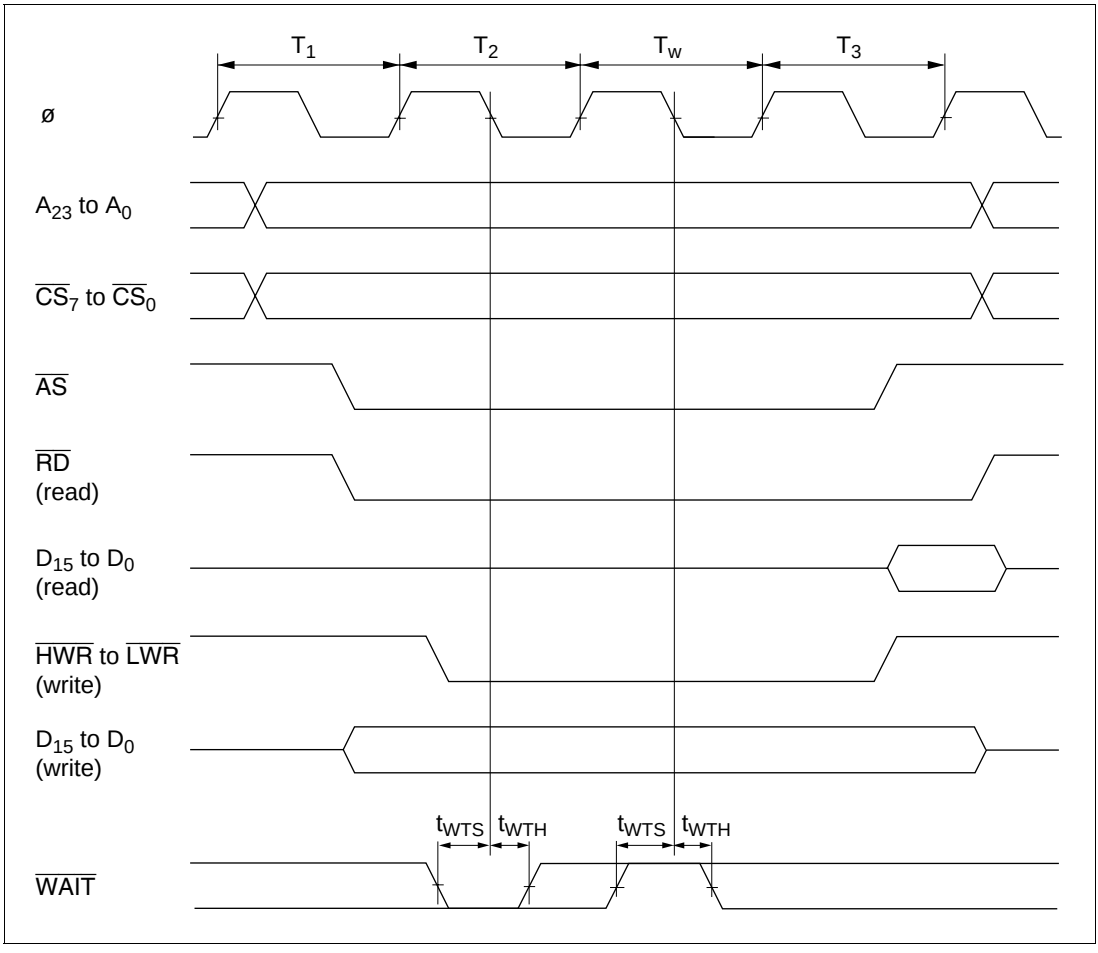


Figure 7.8 Basic Bus Timing (3-State Access, 1 Wait)

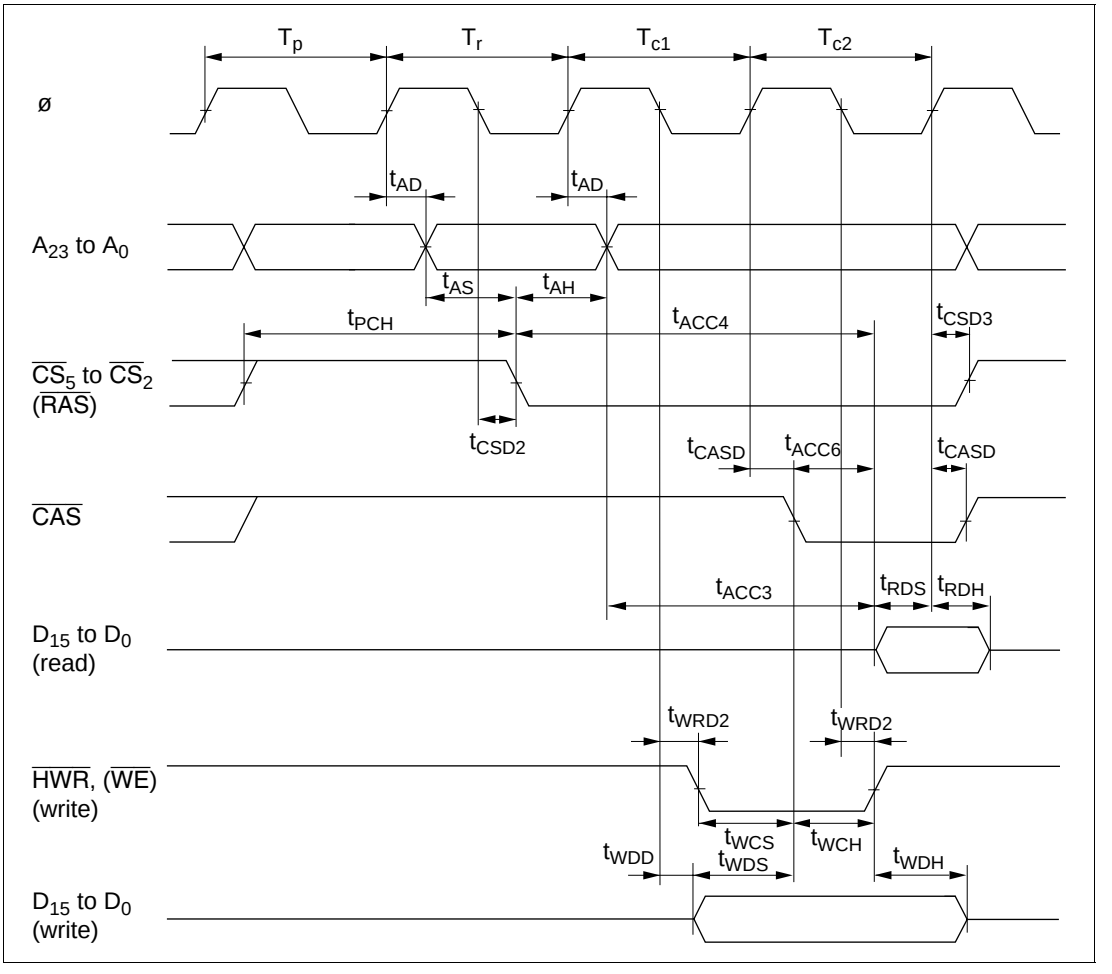


Figure 7.9 DRAM Bus Timing

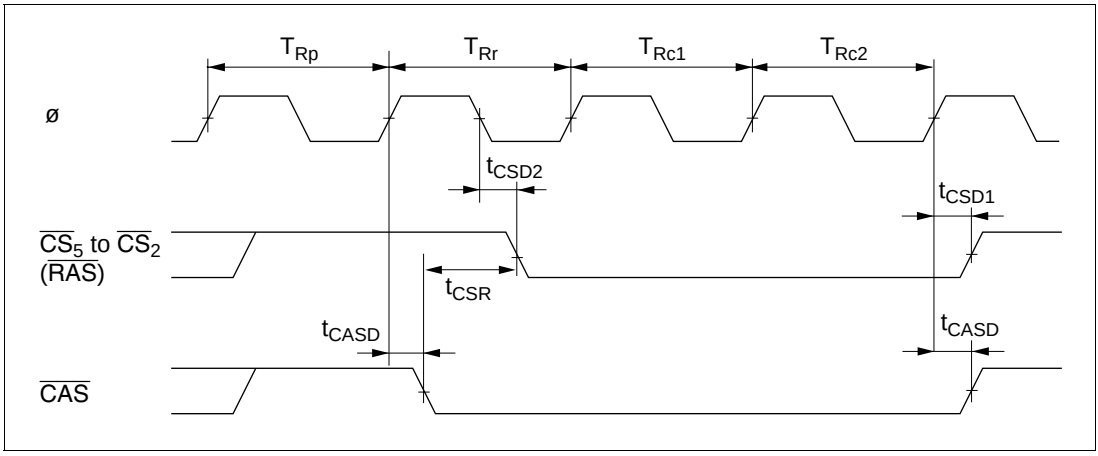


Figure 7.10 CAS-Before-RAS Refresh Timing

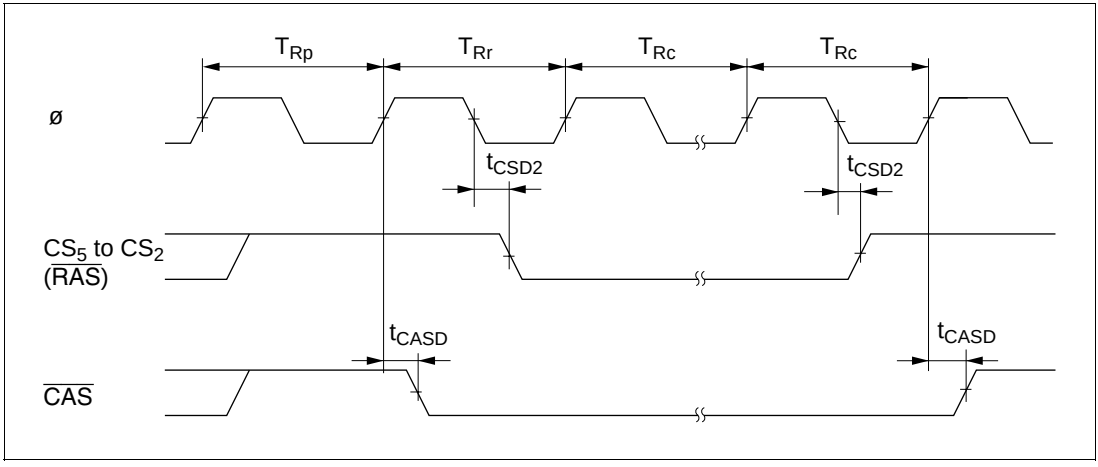


Figure 7.11 Self-Refresh Timing

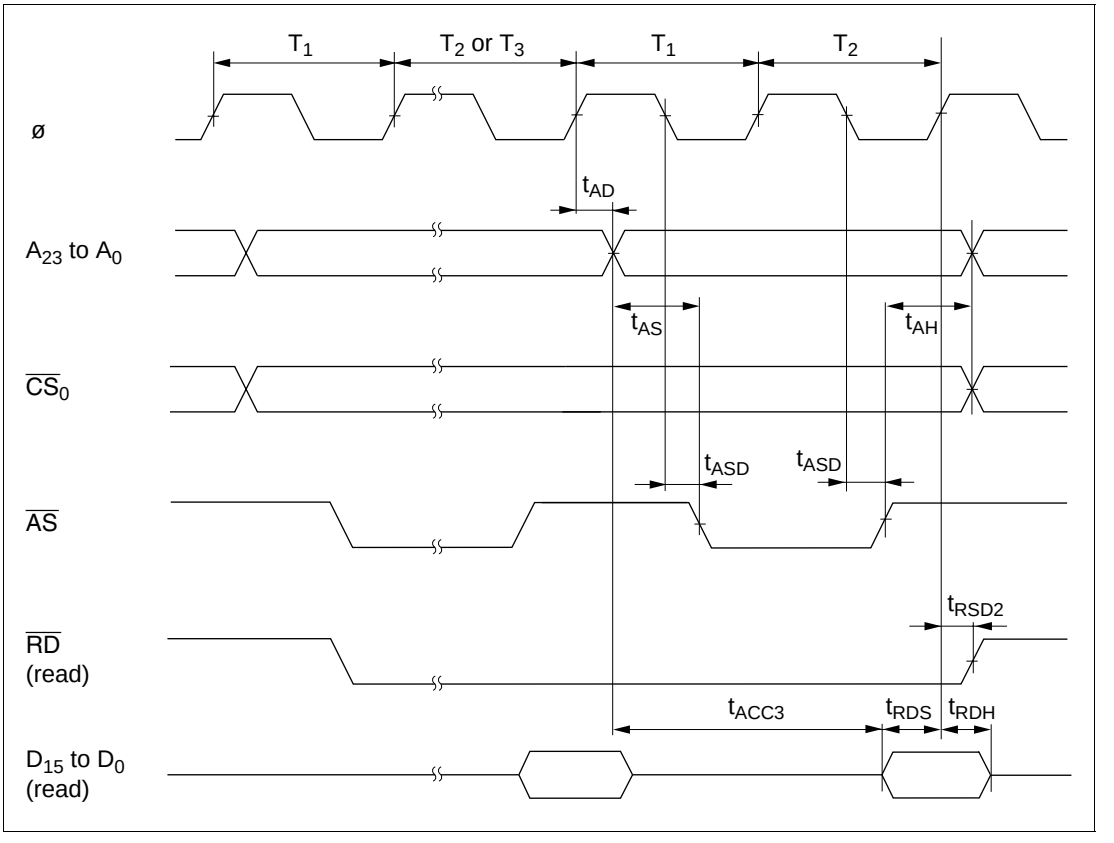


Figure 7.12 Burst ROM Access Timing (2-State Access)

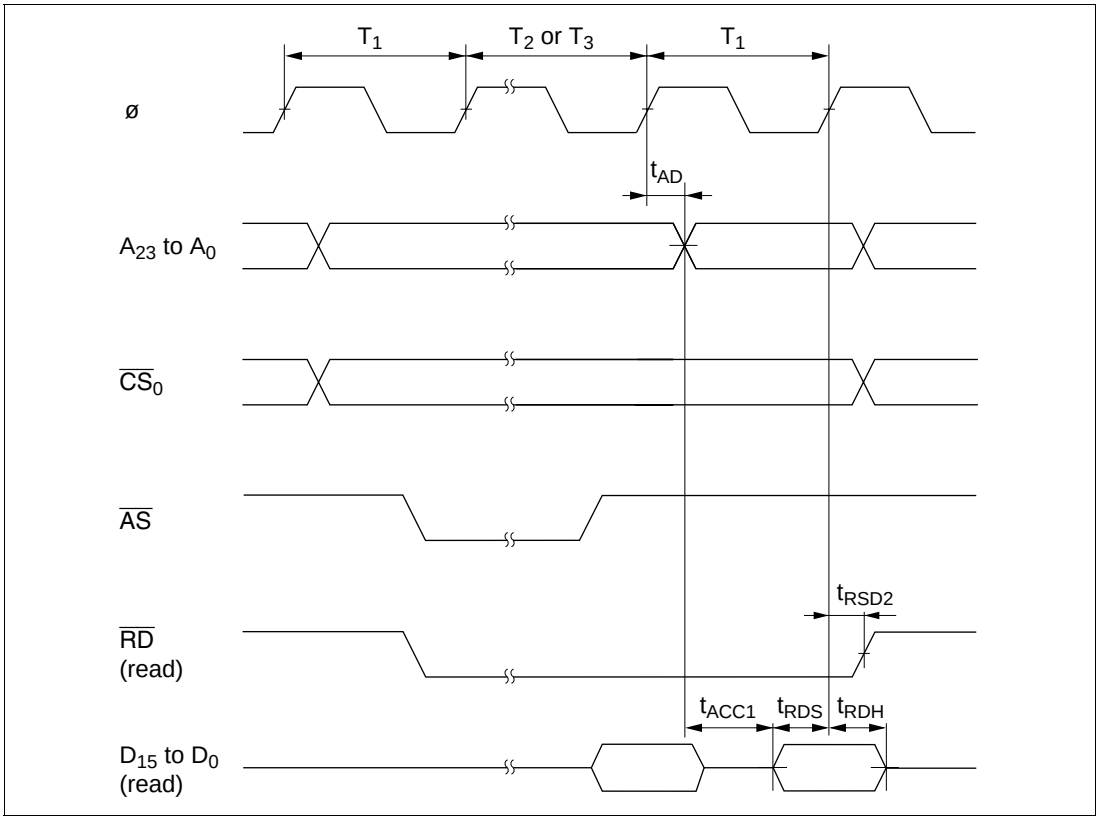


Figure 7.13 Burst ROM Access Timing (1-State Access)

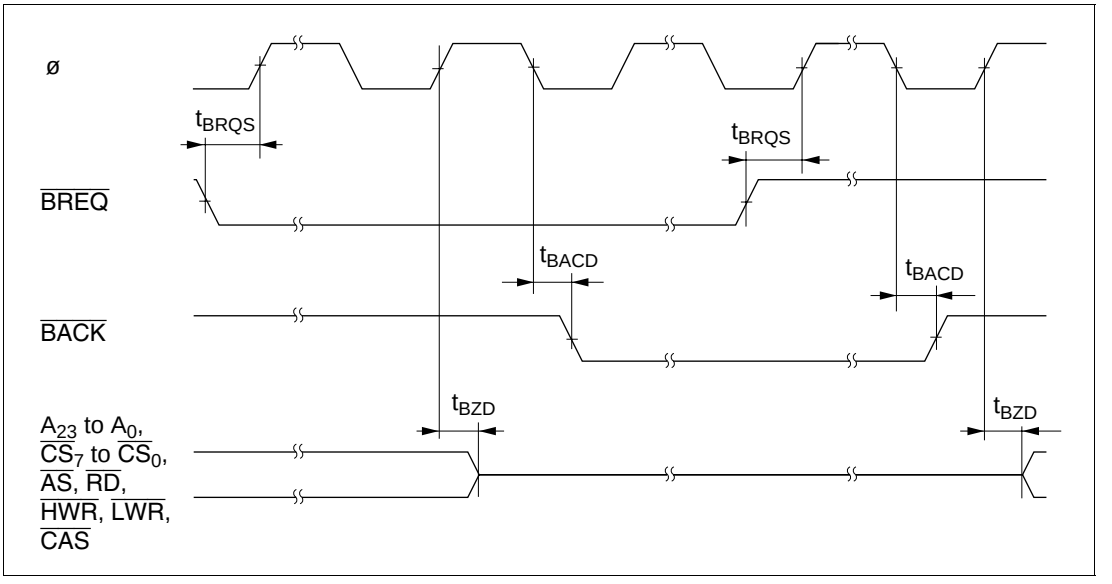


Figure 7.14 External Bus Release Timing

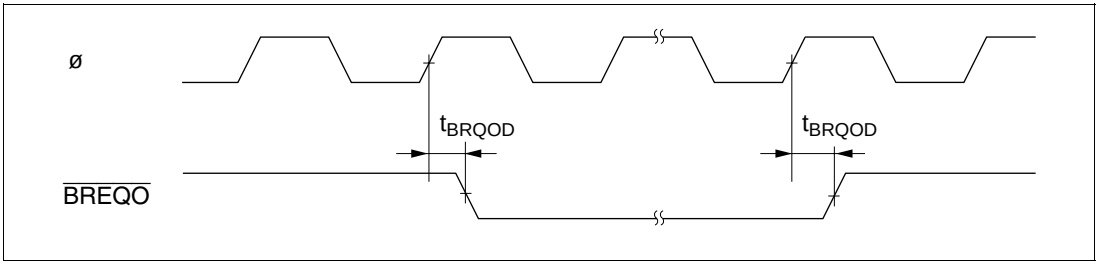


Figure 7.15 External Bus Request Output Timing

(4) DMAC Timing

Table 7.7 DMAC Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	30	—	25	—	ns	Figure 7.19
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	20	—	18		Figure 7.18
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	20	—	18	ns	Figures 7.16 and 7.17
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	20	—	18		

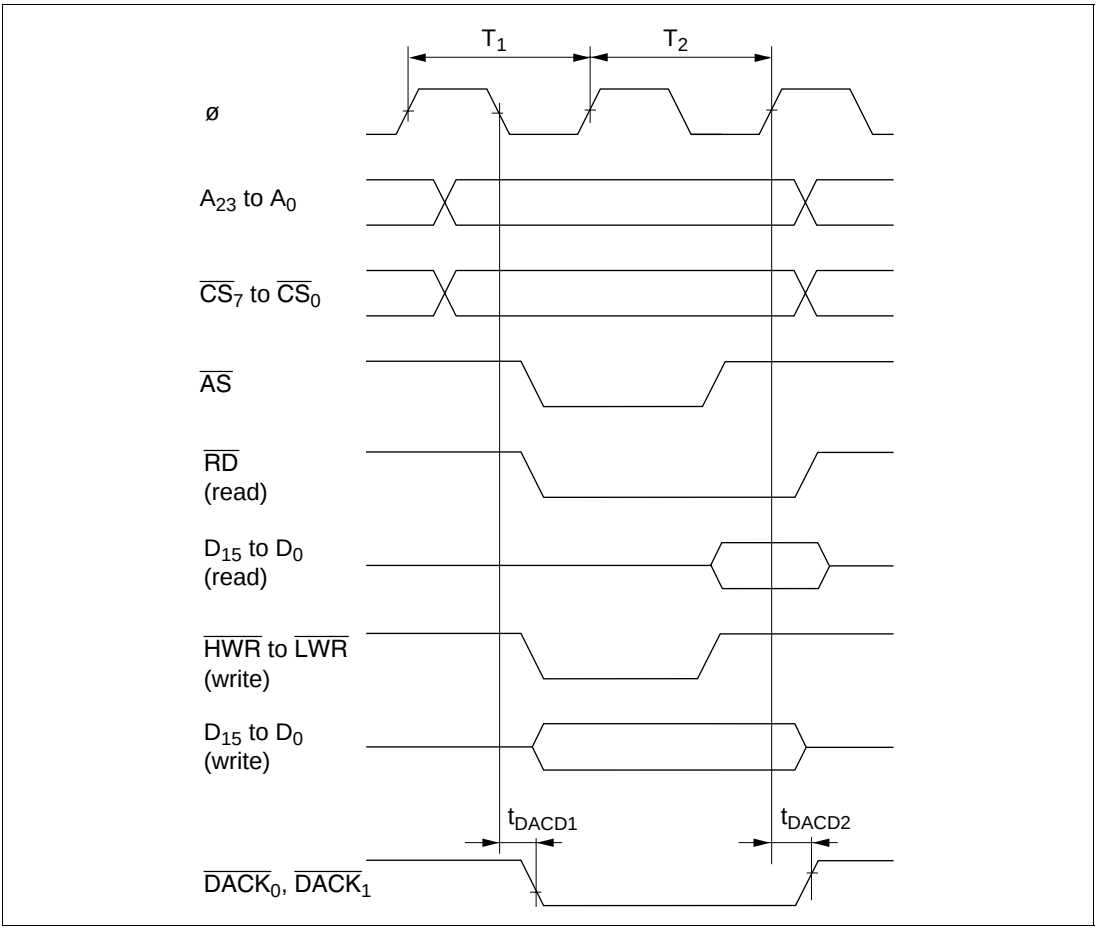


Figure 7.16 DMAC Single Address Transfer Timing (2-State Access)

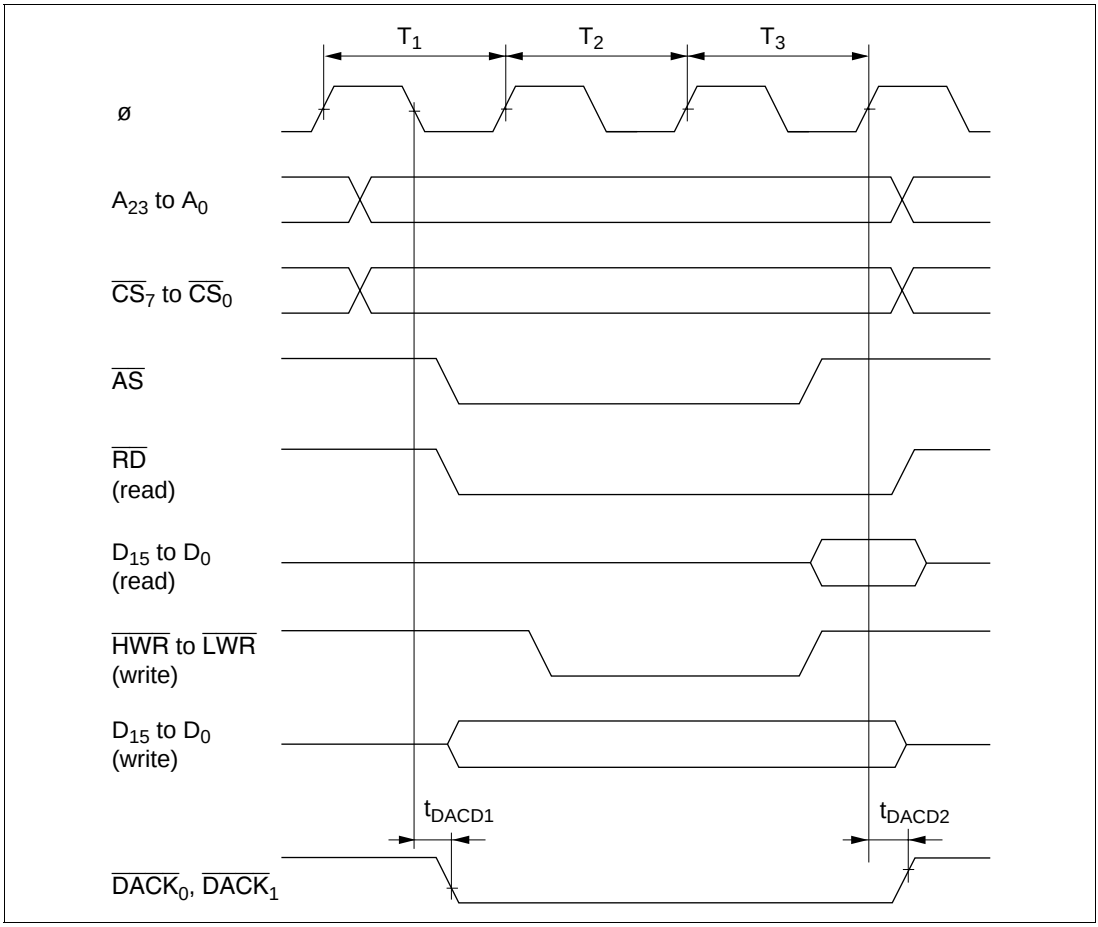


Figure 7.17 DMAC Single Address Transfer Timing (3-State Access)

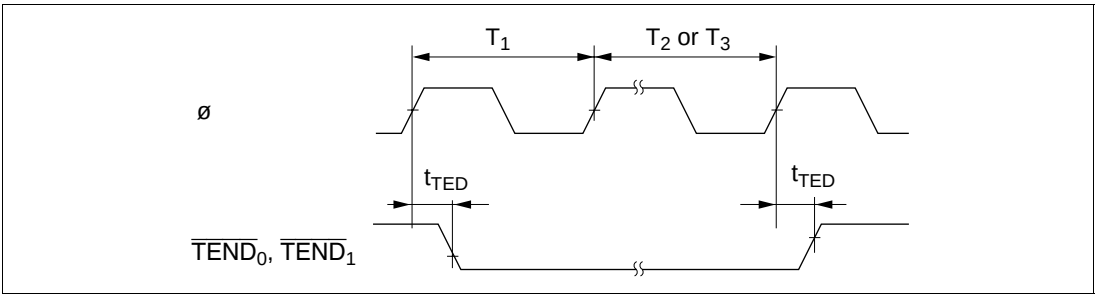


Figure 7.18 DMAC $\overline{\text{TEND}}$ Output Timing

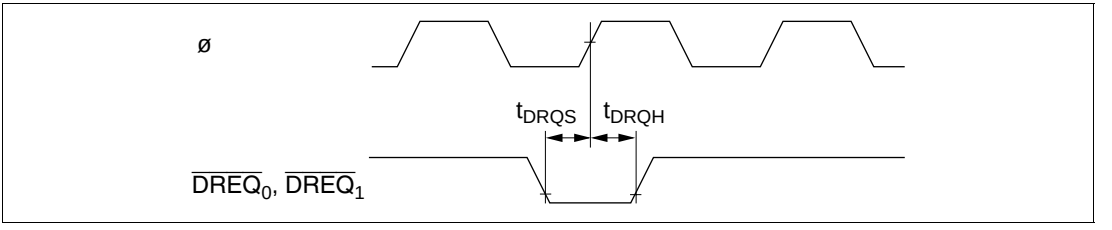


Figure 7.19 DMAC $\overline{\text{DREQ}}$ Input Timing

(5) Timing of On-Chip Supporting Modules

Table 7.8 Timing of On-Chip Supporting Modules

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

				Condition A		Condition B			Test
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
I/O ports	Output data delay time		t_{PWD}	—	50	—	40	ns	Figure 7.20
	Input data setup time		t_{PRS}	30	—	25	—		
	Input data hold time		t_{PRH}	30	—	25	—		
	Pulse output delay time		t_{POD}	—	50	—	40	ns	Figure 7.21
	Timer output delay time		t_{TOCD}	—	50	—	40	ns	Figure 7.22
	Timer input setup time		t_{TICS}	30	—	25	—		
	Timer clock input setup time		t_{TCKS}	30	—	25	—	ns	Figure 7.23
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TCKWL}	2.5	—	2.5	—		
8-bit timer	Timer output delay time		t_{TMOD}	—	50	—	40	ns	Figure 7.24
	Timer reset input setup time		t_{TMRS}	30	—	25	—	ns	Figure 7.26
	Timer clock input setup time		t_{TMCS}	30	—	25	—	ns	Figure 7.25
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—	2.5	—		
WDT	Overflow output delay time		t_{WOVD}	—	50	—	40	ns	Figure 7.27

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 7.28
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure 7.29
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 7.30

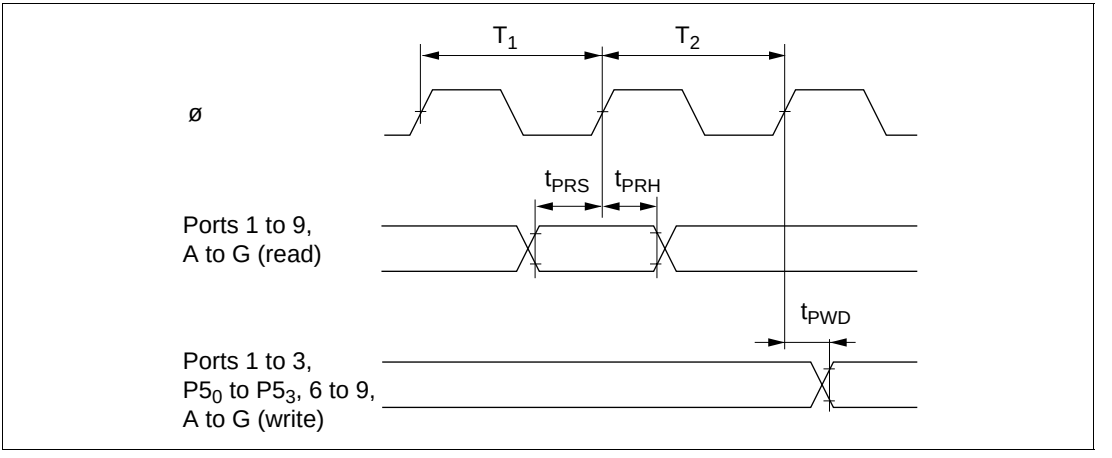


Figure 7.20 I/O Port Input/Output Timing

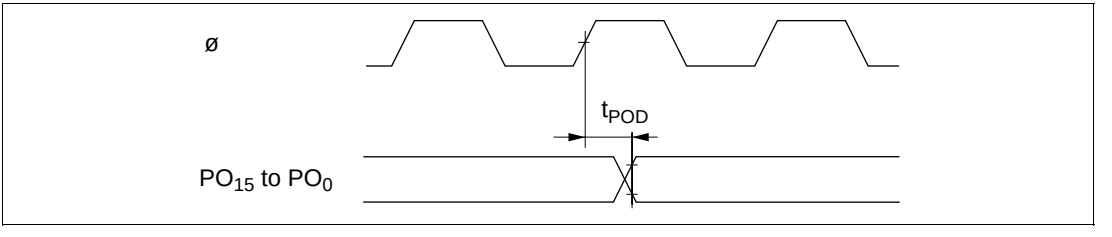


Figure 7.21 PPG Output Timing

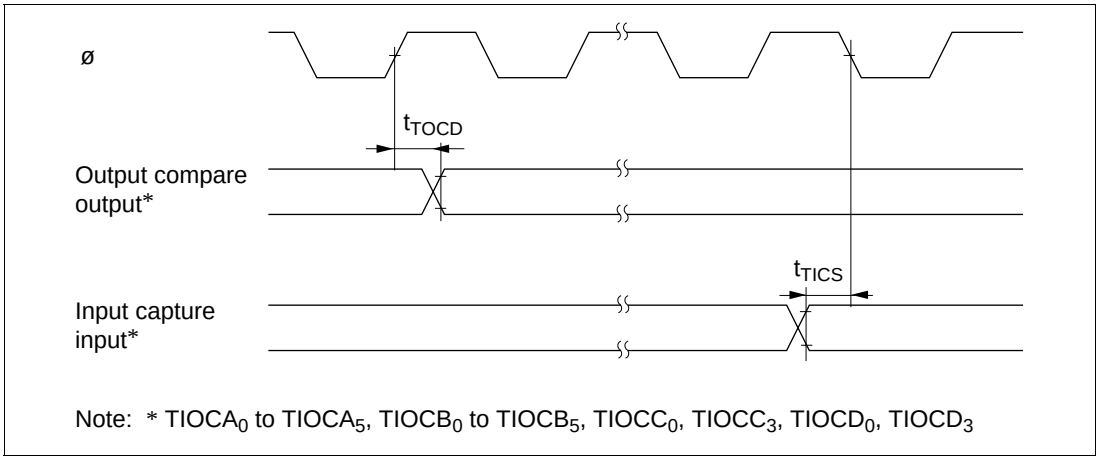


Figure 7.22 TPU Input/Output Timing

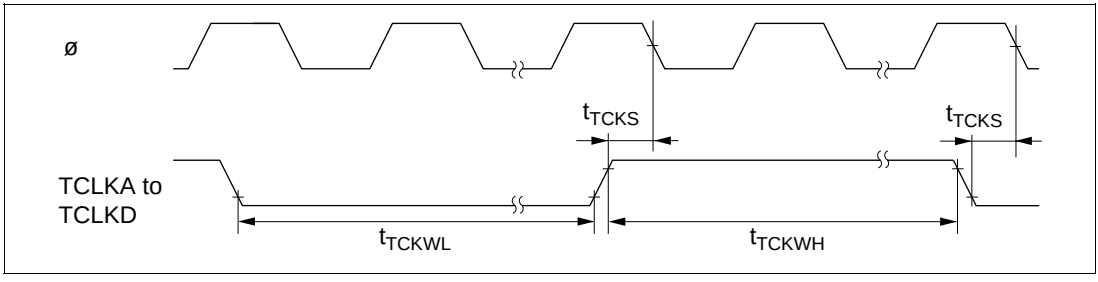


Figure 7.23 TPU Clock Input Timing

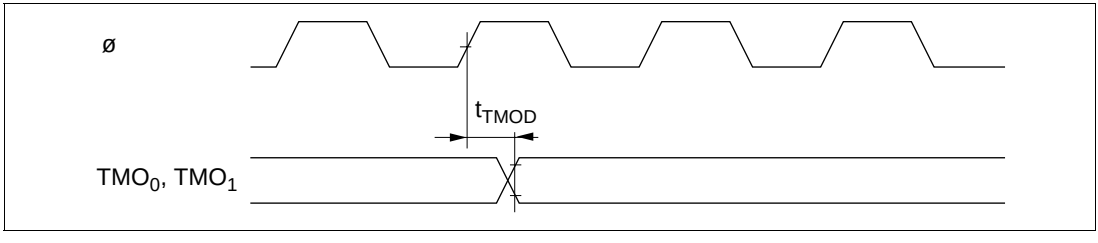


Figure 7.24 8-Bit Timer Output Timing

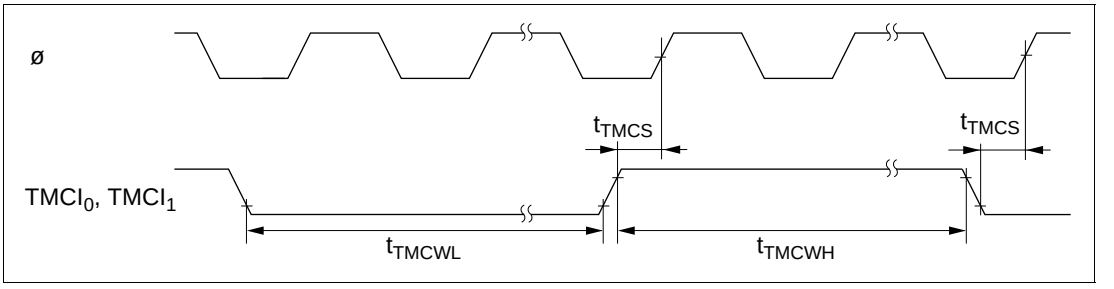


Figure 7.25 8-Bit Timer Clock Input Timing

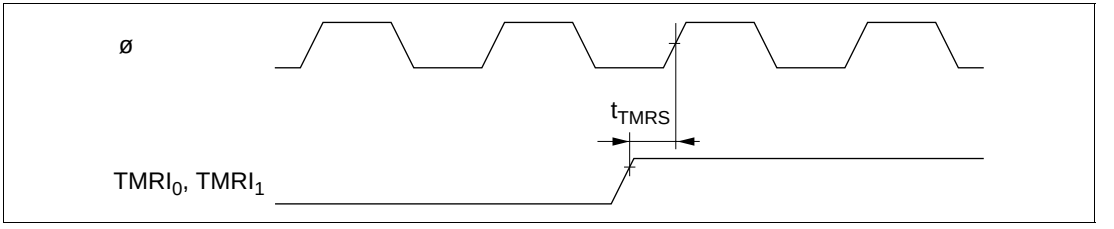


Figure 7.26 8-Bit Timer Reset Input Timing

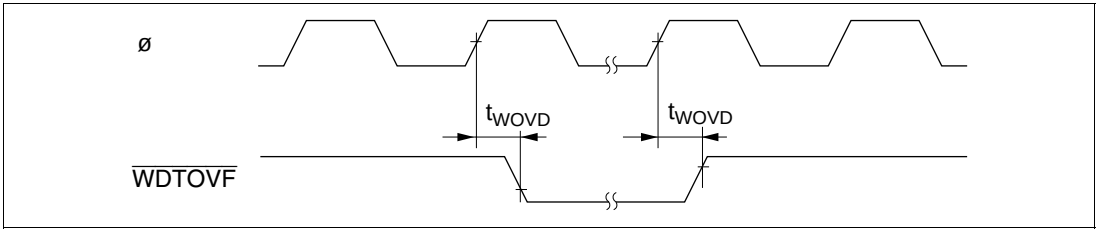


Figure 7.27 WDT Output Timing

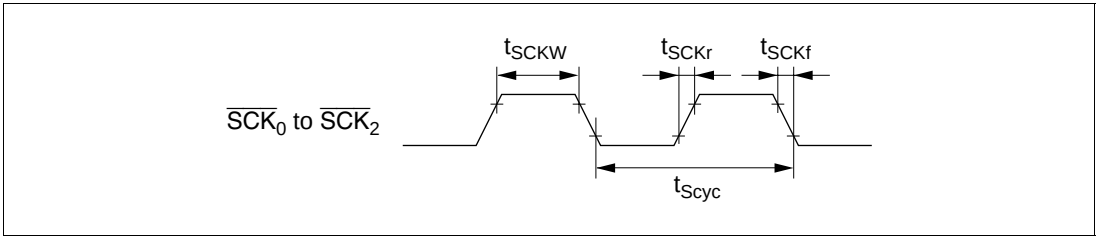


Figure 7.28 SCK Clock Input Timing

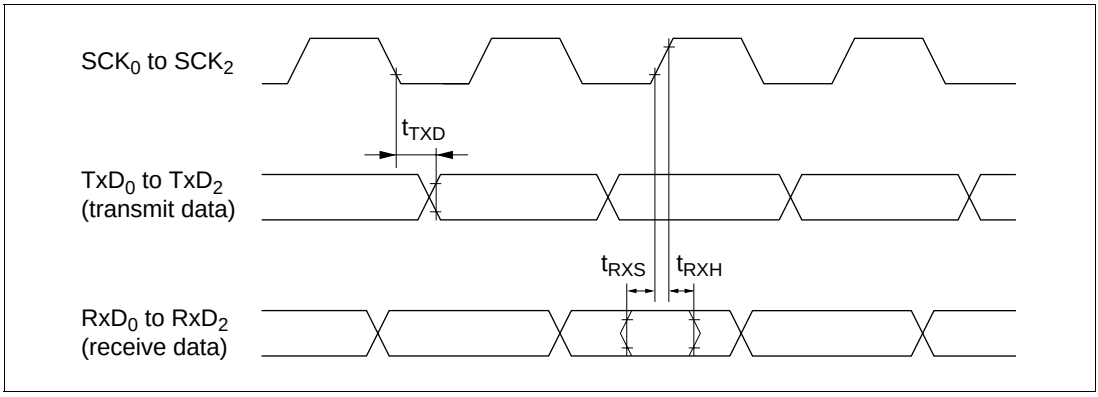


Figure 7.29 SCI Input/Output Timing (Synchronous Mode)

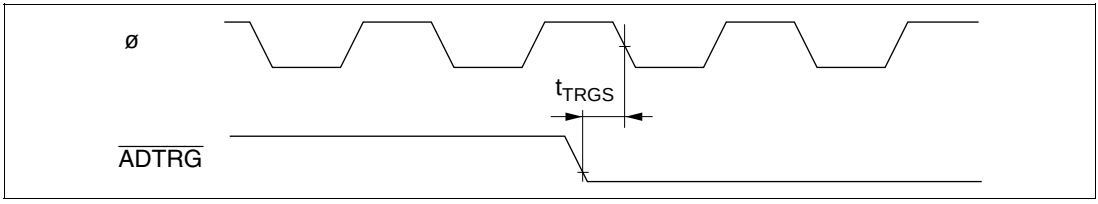


Figure 7.30 A/D Converter External Trigger Input Timing

7.1.4 A/D Conversion Characteristics

Table 7.9 A/D Conversion Characteristics

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bits
Conversion time	6.7	—	—	10.6	—	—	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±5.5	—	—	±5.5	LSB
Offset error	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	±0.5	—	—	±0.5	—	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

7.1.5 D/A Conversion Characteristics

Table 7.10 D/A Conversion Characteristics

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition A			Condition B				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 M resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 M resistive load

7.2 Electrical Characteristics of F-ZTAT Version (H8S/2338)

7.2.1 Absolute Maximum Ratings

Table 7.11 Absolute Maximum Ratings — Preliminary —

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.3	V
Input voltage (FWE)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (except port 4)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * The operating temperature ranges for flash memory programming/erasing are as follows: T_a = 0°C to +75°C (regular specifications), T_a = 0°C to +85°C (wide-range specifications).

7.2.2 DC Characteristics

Table 7.12 DC Characteristics — Preliminary —

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, 7, 9	VT^-	$V_{CC} \times 0.2$	—	—	V	
	$P5_0$ to $P5_3$ $P6_4$ to $P6_7$	VT^+	—	—	$V_{CC} \times 0.7$	V	
	PA_4 to PA_7	$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0, FWE	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, 8, B to G, $P5_4$ to $P5_7$, $P6_0$ to $P6_3$, PA_0 to PA_3		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 03	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0, FWE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, 8 B to G, $P5_4$ to $P5_7$, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD_2 to MD_0, FWE		—	—	1.0	µA	
	Port 4, $P5_4$ to $P5_7$		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Ports 1, 2, 3, 5, 6, 7, 8, 9 Ports A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{CC} = 3.0 V to 3.6 V, V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*[2]	Normal operation	I_{CC}*[4]	—	TBD (3.0 V)	TBD	mA	f = 20 MHz
				58 (3.3 V)	105	mA	f = 25 MHz
	Sleep mode		—	TBD (3.0 V)	TBD	mA	f = 20 MHz
				46 (3.3 V)	82	mA	f = 25 MHz
	Standby mode*[3]		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80		50°C < T_a
Analog power supply voltage	During A/D and D/A conversion	AI_{CC}	—	0.2 (3.0 V)	2.0	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply voltage	During A/D and D/A conversion	AI_{CC}	—	2.4 (3.0 V)	6.0	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. **If the A/D and D/A converters are not used, do not leave the AV_{CC},** V_{ref}, and AV_{SS} pins open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current dissipation values are for $V_{IH\ min} = V_{CC} - 0.5$ V and $V_{IL\ max} = 0.5$ V with all output pins unloaded and all MOS input pull-ups in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:

   I_{CC} max = 1.0 (mA) + 1.15 (mA/(MHz × V)) × V_{CC} × f (normal operation)

   I_{CC} max = 1.0 (mA) + 0.09 (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Table 7.13 Permissible Output Currents **— Preliminary —**

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	$\sum I_{OL}$	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 7.13.

7.2.3 AC Characteristics

(1) Clock Timing

Table 7.14 Clock Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}	50	500	40	500	ns	Figure 7.2
Clock pulse high width	t_{CH}	20	—	15	—	ns	
Clock pulse low width	t_{CL}	20	—	15	—	ns	
Clock rise time	t_{Cr}	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	5	—	5	ns	
Reset oscillation stabilization time (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 7.3
Software standby oscillation stabilization time (crystal)	t_{OSC2}	10	—	10	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	Figure 7.3

(2) Control Signal Timing

Table 7.15 Control Signal Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 7.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

(3) Bus Timing

Table 7.16 Bus Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figures 7.6 to 7.13
Address setup time	t_{AS}	0.5 × t_{cyc} – 15	—	0.5 × t_{cyc} – 15	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	
Precharge time	t_{PCH}	1.5 × t_{cyc}– 20	—	1.5 × t_{cyc}– 15	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	—	15	ns	
$\overline{CS}$ delay time 3	t_{CSD3}	—	25	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
$\overline{CAS}$ delay time	t_{CASD}	—	20	—	15	ns	
Read data setup time	t_{RDS}	15	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} – 25	—	1.5 × t_{cyc} – 20	ns	
Read data access time 3	t_{ACC3}	—	2.0 × t_{cyc} – 25	—	2.0 × t_{cyc} – 20	ns	
Read data access time 4	t_{ACC4}	—	2.5 × t_{cyc} – 25	—	2.5 × t_{cyc} – 20	ns	
Read data access time 5	t_{ACC5}	—	3.0 × t_{cyc} – 25	—	3.0 × t_{cyc} – 20	ns	
Read data access time 6	t_{ACC6}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	—	15	ns	Figures 7.6 to 7.13
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 15$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 15$	—	ns	
Write data delay time	t_{WDD}	—	30	—	20	ns	
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 15$	—	ns	
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
$\overline{WR}$ setup time	t_{WCS}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{WR}$ hold time	t_{WCH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ setup time	t_{CSR}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	Figure 7.10
$\overline{WAIT}$ setup time	t_{WTS}	30	—	25	—	ns	Figure 7.8
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	30	—	ns	Figure 7.14
$\overline{BACK}$ delay time	t_{BACD}	—	15	—	15	ns	
Bus floating time	t_{BZD}	—	50	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	—	25	ns	Figure 7.15

(4) DMAC Timing

Table 7.17 DMAC Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	30	—	25	—	ns	Figure 7.19
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	20	—	18		Figure 7.18
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	20	—	18	ns	Figures 7.16 and 7.17
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	20	—	18		

(5) Timing of On-Chip Supporting Modules

Table 7.18 Timing of On-Chip Supporting Modules —Preliminary—

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

* In planning stage

				Condition A		Condition B			Test
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
I/O ports	Output data delay time		t_{PWD}	—	50	—	40	ns	Figure 7.20
	Input data setup time		t_{PRS}	30	—	25	—		
	Input data hold time		t_{PRH}	30	—	25	—		
	Pulse output delay time		t_{POD}	—	50	—	40	ns	Figure 7.21
	Timer output delay time		t_{TOCD}	—	50	—	40	ns	Figure 7.22
	Timer input setup time		t_{TICS}	30	—	25	—		
	Timer clock input setup time		t_{TCKS}	30	—	25	—	ns	Figure 7.23
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TCKWL}	2.5	—	2.5	—		
8-bit timer	Timer output delay time		t_{TMOD}	—	50	—	40	ns	Figure 7.24
	Timer reset input setup time		t_{TMRS}	30	—	25	—	ns	Figure 7.26
	Timer clock input setup time		t_{TMCS}	30	—	25	—	ns	Figure 7.25
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—	2.5	—		
WDT	Overflow output delay time		t_{WOVD}	—	50	—	40	ns	Figure 7.27

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 7.28
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure 7.29
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 7.30

7.2.4 A/D Conversion Characteristics

Table 7.19 A/D Conversion Characteristics — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

* In planning stage

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bits
Conversion time	6.7	—	—	10.6	—	—	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±5.5	—	—	±5.5	LSB
Offset error	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	±0.5	—	—	±0.5	—	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

7.2.5 D/A Conversion Characteristics

Table 7.20 D/A Conversion Characteristics — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

* In planning stage

	Condition A			Condition B				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 M resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 M resistive load

7.2.6 Flash Memory Characteristics

Table 7.21 Flash Memory Characteristics — Preliminary —

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 0°C to + 75°C (program/erase operating temperature range: regular specifications), T_a = 0°C to + 85°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Programming time*1, *2, *4		t_P	—	10	200	ms/ 128 bytes	
Erase time*1, *3, *6		t_E	—	50	1000	ms/block	
Rewrite times		N_{WEC}	—	—	100	Times	
Programming	Wait time after SWE bit setting*1	x	1	—	—	µs	
	Wait time after PSU bit setting*1	y	50	—	—	µs	
	Wait time after P bit setting*1, *4	z	—	—	10	µs	Wait for additional writing
			—	—	30	µs	1 ≤ n 6
			—	—	200	µs	7 ≤ n ≤ 1000
	Wait time after P bit clearing*1	α	5	—	—	µs	
	Wait time after PSU bit clearing*1	β	5	—	—	µs	
	Wait time after PV bit setting*1	γ	4	—	—	µs	
	Wait time after H'FF dummy write*1	ε	2	—	—	µs	
	Wait time after PV bit clearing*1	η	2	—	—	µs	
	Wait time after SWE bit clearing*1	θ	100	—	—	µs	
	Maximum number of writes*1, *4	N	—	—	1000*5	Times	
Erasing	Wait time after SWE bit setting*1	x	1	—	—	µs	
	Wait time after ESU bit setting*1	y	100	—	—	µs	
	Wait time after E bit setting*1, *6	z	—	—	10	ms	Wait for erasing time
	Wait time after E bit clearing*1	α	10	—	—	µs	
	Wait time after ESU bit clearing*1	β	10	—	—	µs	
	Wait time after EV bit setting*1	γ	20	—	—	µs	
	Wait time after H'FF dummy write*1	ε	2	—	—	µs	
	Wait time after EV bit clearing*1	η	4	—	—	µs	
	Wait time after SWE bit clearing*1	θ	100	—	—	µs	
	Maximum number of erases*1, *6	N	—	—	100	Times	

Notes: 1. Follow the program/erase algorithms when making the time settings.

2. Programming time per 128 bytes. (Indicates the total time during which the P bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)

3. Time to erase one block. (Indicates the time during which the E bit is set in FLMCR1. Does not include the erase-verify time.)

4. Maximum programming time

$$t_P(\max) = \sum_{i=1}^{N} \text{wait time after P bit setting (z)}$$

5. The maximum number of writes (N) should be set as shown below according to the actual set value of z so as not to exceed the maximum programming time (t_P(max)).

   The wait time after P bit setting (z) should be changed as follows according to the number of writes (n).

   Number of writes (n)

   $1 \leq n \leq 6$ z = 30 µs

   $7 \leq n \leq 1000$ z = 200 µs

   $1 \leq n \leq 6$ z = 10 µs: For additional writing

6. For the maximum erase time (t_E(max)), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):

   t_E(max) = Wait time after E bit setting (z) × maximum number of erases (N)

7.3 Usage Note

Although both the F-ZTAT™ and mask ROM versions fully meet the electrical specifications listed in this manual, there may be differences in the actual values of the electrical characteristics, operating margins, noise margins, and so forth, due to differences in the fabrication process, the on-chip ROM, and the layout patterns.

If the F-ZTAT™ version is used to carry out system evaluation and testing, therefore, when switching to the mask ROM version the same evaluation and testing procedures should also be conducted on this version.

8.1 List of Registers (Address Order)

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'F800	MRA	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz	DTC	16/32* bits
to	SAR										
H'FBFF											
	MRB	CHNE	DISEL	CHNS	—	—	—	—	—		
	DAR										
	CRA										
	CRB										
H'FE80	TCR3	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU3	16 bits
H'FE81	TMDR3	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FE82	TIOR3H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE83	TIOR3L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FE84	TIER3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FE85	TSR3	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FE86	TCNT3										
H'FE87											
H'FE88	TGR3A										
H'FE89											
H'FE8A	TGR3B										
H'FE8B											
H'FE8C	TGR3C										
H'FE8D											
H'FE8E	TGR3D										
H'FE8F											

Note: * Located in on-chip RAM. The bus width is 32 bits when the DTC accesses this area as register information, and 16 bits otherwise.

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FE90	TCR4	—	CCLR1	CCLR0	CKEG	CKEGO	TPSC2	TPSC1	TPSC0	TPU4	16 bits
H'FE91	TMDR4	—	—	—	—	MD3	MD2	MD1	MD0		
H'FE92	TIOR4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE94	TIER4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FE95	TSR4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FE96	TCNT4										
H'FE97											
H'FE98	TGR4A										
H'FE99											
H'FE9A	TGR4B										
H'FE9B											
H'FEA0	TCR5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU5	16 bits
H'FEA1	TMDR5	—	—	—	—	MD3	MD2	MD1	MD0		
H'FEA2	TIOR5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FEA4	TIER5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FEA5	TSR5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FEA6	TCNT5										
H'FEA7											
H'FEA8	TGR5A										
H'FEA9											
H'FEAA	TGR5B										
H'FEAB											
H'FEB0	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR	Ports	8 bits
H'FEB1	P2DDR	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR		
H'FEB2	P3DDR	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR		
H'FEB4	P5DDR	—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR		
H'FEB5	P6DDR	P67DDR	P66DDR	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR		
H'FEB6	P7DDR	—	—	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR		
H'FEB7	P8DDR	—	P86DDR	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR		
H'FEB8	P9DDR	P97DDR	P96DDR	P95DDR	P94DDR	P93DDR	P92DDR	—	—		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FEB9	PADDR	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR	Ports	8 bits
H'FEBA	PBDDR	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR		
H'FEBB	PCDDR	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR		
H'FEBC	PDDDR	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR		
H'FEBD	PEDDR	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR		
H'FEBE	PFDDR	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR		
H'FEBF	PGDDR	—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR		
H'FEC4	IPRA	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	Interrupt	8 bits
H'FEC5	IPRB	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	controller	
H'FEC6	IPRC	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC7	IPRD	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC8	IPRE	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC9	IPRF	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECA	IPRG	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECB	IPRH	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECC	IPRI	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECD	IPRJ	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECE	IPRK	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FED0	ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	Bus controller	16 bits
H'FED1	ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0		
H'FED2	WCRH	W71	W70	W61	W60	W51	W50	W41	W40		
H'FED3	WCRL	W31	W30	W21	W20	W11	W10	W01	W00		
H'FED4	BCRH	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2	RMTS1	RMTS0		
H'FED5	BCRL	BRLE	BREQOE	EAE	—	DDS	—	WDBE	WAITE		
H'FED6	MCR	TPC	BE	RCDM	—	MXC1	MXC0	RLW1	RLW0		
H'FED7	DRAMCR	RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0		
H'FED8	RTCNT										
H'FED9	RTCOR										
H'FEDB	RAMER*	—	—	—	—	RAMS	RAM2	RAM1	RAM0		

Note: * Valid only in F-ZTAT version.

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FEE0	MAR0AH	—	—	—	—	—	—	—	—	DMAC	16 bits
H'FEE1											
H'FEE2	MAR0AL										
H'FEE3											
H'FEE4	IOR0A										
H'FEE5											
H'FEE6	ETCR0A										
H'FEE7											
H'FEE8	MAR0BH	—	—	—	—	—	—	—	—		
H'FEE9											
H'FEEA	MAR0BL										
H'FEEB											
H'FEEC	IOR0B										
H'FEED											
H'FEEE	ETCR0B										
H'FEEF											
H'FEF0	MAR1AH	—	—	—	—	—	—	—	—		
H'FEF1											
H'FEF2	MAR1AL										
H'FEF3											
H'FEF4	IOAR1A										
H'FEF5											
H'FEF6	ETCR1A										
H'FEF7											
H'FEF8	MAR1BH	—	—	—	—	—	—	—	—		
H'FEF9											
H'FEFA	MAR1BL										
H'FEFB											
H'FEFC	IOAR1B										
H'FEFD											
H'FEFE	ETCR1B										
H'FEFF											

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF00	DMAWER	—	—	—	—	WE1B	WE1A	WE0B	WE0A	DMAC	8 bits
H'FF01	DMATCR	—	—	TEE1	TEE0	—	—	—	—		
H'FF02	DMACR0A	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	16 bits
		DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	Full address mode	
H'FF03	DMACR0B	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	
		—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	Full address mode	
H'FF04	DMACR1A	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	
		DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	Full address mode	
H'FF05	DMACR1B	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	
		—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	Full address mode	
H'FF06	DMABCRH	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A	Short address mode	
		FAE1	FAE0	—	—	DTA1	—	DTA0	—	Full address mode	
H'FF07	DMABCRL	DTE1B	DTE1A	DTE0B	DTE0A	DTIE1B	DTIE1A	DTIE0B	DTIE0A	Short address mode	
		DTME1	DTE1	DTME0	DTE0	DTIE1B	DTIE1A	DTIE0B	DTIE0A	Full address mode	
H'FF2C	ISCRH	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA	Interrupt controller	8 bits
H'FF2D	ISCRL	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA		
H'FF2E	IER	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E		
H'FF2F	ISR	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F		
H'FF30 to H'FF35	DTCER	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0	DTC	8 bits
H'FF37	DTVECR	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0		
H'FF38	SBYCR	SSBY	STS2	STS1	STS0	OPE	—	—	IRQ37S	Power-down mode	8 bits
H'FF39	SYSCR	—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME	MCU	8 bits

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF3A	SCKCR	PSTOP	—	DIV	—	—	SCK2	SCK1	SCK0	Clock pulse generator	8 bits
H'FF3B	MDCR	—	—	—	—	—	MDS2	MDS1	MDS0	MCU	8 bits
H'FF3C	MSTPCRH	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	Power-down	8 bits
H'FF3D	MSTPCRL	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0	mode	
H'FF42	SYSCR*2	—	—	—	—	FLSHE	—	—	—	MCU	8 bits
H'FF44	Reserved	—	—	—	—	—	—	—	—	Reserved	—
H'FF45	PFCR1	—	—	—	—	A23E	A22E	A21E	A20E	Port	8 bits
H'FF46	PCR	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0	PPG	8 bits
H'FF47	PMR	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV		
H'FF48	NDERH	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8		
H'FF49	NDERL	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0		
H'FF4A	PODRH	POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8		
H'FF4B	PODRL	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0		
H'FF4C*1	NDRH	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8		
H'FF4D*1	NDRL	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0		
H'FF4E*1	NDRH	—	—	—	—	NDR11	NDR10	NDR9	NDR8		
H'FF4F*1	NDRL	—	—	—	—	NDR3	NDR2	NDR1	NDR0		
H'FF50	PORT1	P17	P16	P15	P14	P13	P12	P11	P10	Ports	8 bits
H'FF51	PORT2	P27	P26	P25	P24	P23	P22	P21	P20		
H'FF52	PORT3	—	—	P35	P34	P33	P32	P31	P30		
H'FF53	PORT4	P47	P46	P45	P44	P43	P42	P41	P40		
H'FF54	PORT5	P57	P56	P55	P54	P53	P52	P51	P50		
H'FF55	PORT6	P67	P66	P65	P64	P63	P62	P61	P60		
H'FF56	PORT7	—	—	P75	P74	P73	P72	P71	P70		
H'FF57	PORT8	—	P86	P85	P84	P83	P82	P81	P80		
H'FF58	PORT9	P97	P96	P95	P94	P93	P92	—	—		

Notes: 1. If the pulse output group 2 and pulse output group 3 output triggers are the same according to the PCR setting, the NDRH address will be H'FF4C, and if different, the address of NDRH for group 2 will be H'FF4E, and that for group 3 will be H'FF4C. Similarly, if the pulse output group 0 and pulse output group 1 output triggers are the same according to the PCR setting, the NDRL address will be H'FF4D, and if different, the address of NDRL for group 0 will be H'FF4F, and that for group 1 will be H'FF4D.

2. Valid only in F-ZTAT version

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF59	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Ports	8 bits
H'FF5A	PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0		
H'FF5B	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0		
H'FF5C	PORTD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0		
H'FF5D	PORTE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
H'FF5E	PORTF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0		
H'FF5F	PORTG	—	—	—	PG4	PG3	PG2	PG1	PG0		
H'FF60	P1DR	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR		
H'FF61	P2DR	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR		
H'FF62	P3DR	—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR		
H'FF64	P5DR	—	—	—	—	P53DR	P52DR	P51DR	P50DR		
H'FF65	P6DR	P67DR	P66DR	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR		
H'FF66	P7DR	—	—	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR		
H'FF67	P8DR	—	P86DR	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR		
H'FF68	P9DR	P97DR	P96DR	P95DR	P94DR	P93DR	P92DR	—	—		
H'FF69	PADR	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR		
H'FF6A	PBDR	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR		
H'FF6B	PCDR	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR		
H'FF6C	PDDR	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR		
H'FF6D	PEDR	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR		
H'FF6E	PFDR	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR		
H'FF6F	PGDR	—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR		
H'FF70	PAPCR	PA7PCR	PA6PCR	PA5PCR	PA4PCR	PA3PCR	PA2PCR	PA1PCR	PA0PCR		
H'FF71	PBPCR	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR		
H'FF72	PCPCR	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR		
H'FF73	PDPCR	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR		
H'FF74	PEPCR	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR		
H'FF76	P3ODR	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR		
H'FF77	PAODR	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF78	SMR0	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP0*[6]	CKS1	CKS0	SCI0, smart card interface 0	8 bits
H'FF79	BRR0										
H'FF7A	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF7B	TDR0										
H'FF7C	SSR0	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT		
H'FF7D	RDR0										
H'FF7E	SCMR0	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF80	SMR1	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP0*[6]	CKS1	CKS0	SCI1, smart card interface 1	8 bits
H'FF81	BRR1										
H'FF82	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF83	TDR1										
H'FF84	SSR1	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT		
H'FF85	RDR1										
H'FF86	SCMR1	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF88	SMR2	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP0*[6]	CKS1	CKS0	SCI2, smart card interface 2	8 bits
H'FF89	BRR2										
H'FF8A	SCR2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF8B	TDR2										
H'FF8C	SSR2	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT		
H'FF8D	RDR2										
H'FF8E	SCMR2	—	—	—	—	SDIR	SINV	—	SMIF		

Notes: 3. Functions as C/$\overline{A}$ for SCI use, and as GM for smart card interface use.
4. Functions as CHR for SCI use, and as BLK for smart card interface use.
5. Functions as STOP for SCI use, and as BCP1 for smart card interface use.
6. Functions as MP for SCI use, and as BCP0 for smart card interface use.
7. Functions as FER for SCI use, and as ERS for smart card interface use.

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FE90	ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter	8 bits
H'FE91	ADDRAL	AD1	AD0	—	—	—	—	—	—		
H'FE92	ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE93	ADDRBL	AD1	AD0	—	—	—	—	—	—		
H'FE94	ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE95	ADDRCL	AD1	AD0	—	—	—	—	—	—		
H'FE96	ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE97	ADDRDL	AD1	AD0	—	—	—	—	—	—		
H'FE98	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0		
H'FE99	ADCR	TRGS1	TRGS0	—	—	CKS1	CH3	—	—		
H'FFA4	DADR0									D/A converter	8 bits
H'FFA5	DADR1										
H'FFA6	DACR01	DAOE1	DAOE0	DAE	—	—	—	—	—		
H'FFA8	DADR2										
H'FFA9	DADR3										
H'FFAA	DACR23	DAOE1	DAOE0	DAE	—	—	—	—	—		
H'FFAC	PFCR2	WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—	Ports	8 bits
H'FFB0	TCR0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	8-bit timer	16 bits
H'FFB1	TCR1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	channel 0, 1	
H'FFB2	TCSR0	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0		
H'FFB3	TCSR1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0		
H'FFB4	TCORA0										
H'FFB5	TCORA1										
H'FFB6	TCORB0										
H'FFB7	TCORB1										
H'FFB8	TCNT0										
H'FFB9	TCNT1										
H'FFBC (Read)	TCSR	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	WDT	16 bits
H'FFBD (Read)	TCNT										
H'FFBF (Read)	RSTCSR	WOVF	RSTE	—	—	—	—	—	—		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FFC0	TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU	16 bits
H'FFC1	TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0		
H'FFC8	FLMCR1*[1]	FWE	SWE	ESU	PSU	EV	PV	E	P	Flash memory	8 bits
H'FFC9	FLMCR2*[1]	FLER	—	—	—	—	—	—	—		
H'FFCA	EBR1*[1]	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0		
H'FFCB	EBR2*[1]	—	—	EB13*[2]	EB12*[2]	EB11	EB10	EB9	EB8		
H'FFD0	TCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU0	16 bits
H'FFD1	TMDR0	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FFD2	TIOR0H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFD3	TIOR0L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FFD4	TIER0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FFD5	TSR0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FFD6	TCNT0										
H'FFD7											
H'FFD8	TGR0A										
H'FFD9											
H'FFDA	TGR0B										
H'FFDB											
H'FFDC	TGR0C										
H'FFDD											
H'FFDE	TGR0D										
H'FFDF											

Notes: 1. Valid only in F-ZTAT version
2. Valid only in H8S/2339 F-ZTAT version

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FFE0	TCR1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU1	16 bits
H'FFE1	TMDR1	—	—	—	—	MD3	MD2	MD1	MD0		
H'FFE2	TIOR1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFE4	TIER1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FFE5	TSR1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FFE6	TCNT1										
H'FFE7											
H'FFE8	TGR1A										
H'FFE9											
H'FFEA	TGR1B										
H'FFEB											
H'FFF0	TCR2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU2	16 bits
H'FFF1	TMDR2	—	—	—	—	MD3	MD2	MD1	MD0		
H'FFF2	TIOR2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFF4	TIER2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FFF5	TSR2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FFF6	TCNT2										
H'FFF7											
H'FFF8	TGR2A										
H'FFF9											
H'FFFA	TGR2B										
H'FFFB											

8.2 List of Registers (By Module)

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Interrupt controller	System control register	SYSCR	R/W	H'01	H'FF39
	IRQ sense control register H	ISCRH	R/W	H'00	H'FF2C
	IRQ sense control register L	ISCRL	R/W	H'00	H'FF2D
	IRQ enable register	IER	R/W	H'00	H'FF2E
	IRQ status register	ISR	R/(W)*[2]	H'00	H'FF2F
	Interrupt priority register A	IPRA	R/W	H'77	H'FEC4
	Interrupt priority register B	IPRB	R/W	H'77	H'FEC5
	Interrupt priority register C	IPRC	R/W	H'77	H'FEC6
	Interrupt priority register D	IPRD	R/W	H'77	H'FEC7
	Interrupt priority register E	IPRE	R/W	H'77	H'FEC8
	Interrupt priority register F	IPRF	R/W	H'77	H'FEC9
	Interrupt priority register G	IPRG	R/W	H'77	H'FECA
	Interrupt priority register H	IPRH	R/W	H'77	H'FECB
	Interrupt priority register I	IPRI	R/W	H'77	H'FECC
	Interrupt priority register J	IPRJ	R/W	H'77	H'FECD
	Interrupt priority register K	IPRK	R/W	H'77	H'FECE
Bus controller	Bus width control register	ABWCR	R/W	H'FF/H'00*[5]	H'FED0
	Access state control register	ASTCR	R/W	H'FF	H'FED1
	Wait control register H	WCRH	R/W	H'FF	H'FED2
	Wait control register L	WCRL	R/W	H'FF	H'FED3
	Bus control register H	BCRH	R/W	H'D0	H'FED4
	Bus control register L	BCRL	R/W	H'3C	H'FED5
	Memory control register	MCR	R/W	H'00	H'FED6
	DRAM control register	DRAMCR	R/W	H'00	H'FED7
	Refresh timer counter	RTCNT	R/W	H'00	H'FED8
	Refresh time constant register	RTCOR	R/W	H'FF	H'FED9

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
DTC	DTC mode register A	MRA	—*[3]	Undefined	—*[4]
	DTC mode register B	MRB	—*[3]	Undefined	—*[4]
	DTC source address register	SAR	—*[3]	Undefined	—*[4]
	DTC destination address register	DAR	—*[3]	Undefined	—*[4]
	DTC transfer count register A	CRA	—*[3]	Undefined	—*[4]
	DTC transfer count register B	CRB	—*[3]	Undefined	—*[4]
	DTC enable register	DTCER	R/W	H'00	H'FF30 to H'FF35
	DTC vector register	DTVECR	R/W	H'00	H'FF37
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
TPU0	Timer control register 0	TCR0	R/W	H'00	H'FFD0
	Timer mode register 0	TMDR0	R/W	H'C0	H'FFD1
	Timer I/O control register 0H	TIOR0H	R/W	H'00	H'FFD2
	Timer I/O control register 0L	TIOR0L	R/W	H'00	H'FFD3
	Timer interrupt enable register 0	TIER0	R/W	H'40	H'FFD4
	Timer status register 0	TSR0	R/(W)*[2]	H'C0	H'FFD5
	Timer counter 0	TCNT0	R/W	H'0000	H'FFD6
	Timer general register 0A	TGR0A	R/W	H'FFFF	H'FFD8
	Timer general register 0B	TGR0B	R/W	H'FFFF	H'FFDA
	Timer general register 0C	TGR0C	R/W	H'FFFF	H'FFDC
	Timer general register 0D	TGR0D	R/W	H'FFFF	H'FFDE
TPU1	Timer control register 1	TCR1	R/W	H'00	H'FFE0
	Timer mode register 1	TMDR1	R/W	H'C0	H'FFE1
	Timer I/O control register 1	TIOR1	R/W	H'00	H'FFE2
	Timer interrupt enable register 1	TIER1	R/W	H'40	H'FFE4
	Timer status register 1	TSR1	R/(W)*[2]	H'C0	H'FFE5
	Timer counter 1	TCNT1	R/W	H'0000	H'FFE6
	Timer general register 1A	TGR1A	R/W	H'FFFF	H'FFE8
	Timer general register 1B	TGR1B	R/W	H'FFFF	H'FFEA

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
TPU2	Timer control register 2	TCR2	R/W	H'00	H'FFF0
	Timer mode register 2	TMDR2	R/W	H'C0	H'FFF1
	Timer I/O control register 2	TIOR2	R/W	H'00	H'FFF2
	Timer interrupt enable register 2	TIER2	R/W	H'40	H'FFF4
	Timer status register 2	TSR2	R/(W)*[2]	H'C0	H'FFF5
	Timer counter 2	TCNT2	R/W	H'0000	H'FFF6
	Timer general register 2A	TGR2A	R/W	H'FFFF	H'FFF8
	Timer general register 2B	TGR2B	R/W	H'FFFF	H'FFFA
TPU3	Timer control register 3	TCR3	R/W	H'00	H'FE80
	Timer mode register 3	TMDR3	R/W	H'C0	H'FE81
	Timer I/O control register 3H	TIOR3H	R/W	H'00	H'FE82
	Timer I/O control register 3L	TIOR3L	R/W	H'00	H'FE83
	Timer interrupt enable register 3	TIER3	R/W	H'40	H'FE84
	Timer status register 3	TSR3	R/(W)*[2]	H'C0	H'FE85
	Timer counter 3	TCNT3	R/W	H'0000	H'FE86
	Timer general register 3A	TGR3A	R/W	H'FFFF	H'FE88
	Timer general register 3B	TGR3B	R/W	H'FFFF	H'FE8A
	Timer general register 3C	TGR3C	R/W	H'FFFF	H'FE8C
	Timer general register 3D	TGR3D	R/W	H'FFFF	H'FE8E
TPU4	Timer control register 4	TCR4	R/W	H'00	H'FE90
	Timer mode register 4	TMDR4	R/W	H'C0	H'FE91
	Timer I/O control register 4	TIOR4	R/W	H'00	H'FE92
	Timer interrupt enable register 4	TIER4	R/W	H'40	H'FE94
	Timer status register 4	TSR4	R/(W)*[2]	H'C0	H'FE95
	Timer counter 4	TCNT4	R/W	H'0000	H'FE96
	Timer general register 4A	TGR4A	R/W	H'FFFF	H'FE98
	Timer general register 4B	TGR4B	R/W	H'FFFF	H'FE9A

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
TPU5	Timer control register 5	TCR5	R/W	H'00	H'FEA0
	Timer mode register 5	TMDR5	R/W	H'C0	H'FEA1
	Timer I/O control register 5	TIOR5	R/W	H'00	H'FEA2
	Timer interrupt enable register 5	TIER5	R/W	H'40	H'FEA4
	Timer status register 5	TSR5	R/(W)*[2]	H'C0	H'FEA5
	Timer counter 5	TCNT5	R/W	H'0000	H'FEA6
	Timer general register 5A	TGR5A	R/W	H'FFFF	H'FEA8
	Timer general register 5B	TGR5B	R/W	H'FFFF	H'FEAA
ALL TPU channels	Timer start register	TSTR	R/W	H'00	H'FFC0
	Timer syncro register	TSYR	R/W	H'00	H'FFC1
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
PPG	PPG output control register	PCR	R/W	H'FF	H'FF46
	PPG output mode register	PMR	R/W	H'F0	H'FF47
	Next data enable register H	NDERH	R/W	H'00	H'FF48
	Next data enable register L	NDERL	R/W	H'00	H'FF49
	Output data register H	PODRH	R/(W)*[6]	H'00	H'FF4A
	Output data register L	PODRL	R/(W)*[6]	H'00	H'FF4B
	Next data register H	NDRH	R/W	H'00	H'FF4C*[7]
					H'FF4E
	Next data register L	NDRL	R/W	H'00	H'FF4D*[7]
					H'FF4F
	Port 1 data direction register	P1DDR	W	H'00	H'FEB0
	Port 2 data direction register	P2DDR	W	H'00	H'FEB1
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
8-bit timer 0	Timer control register 0	TCR0	R/W	H'00	H'FFB0
	Timer control/status register 0	TCSR0	R/(W)*[8]	H'00	H'FFB2
	Timer constant register A0	TCORA0	R/W	H'FF	H'FFB4
	Timer constant register B0	TCORB0	R/W	H'FF	H'FFB6
	Timer counter 0	TCNT0	R/W	H'00	H'FFB8
8-bit timer 1	Timer control register 1	TCR1	R/W	H'00	H'FFB1
	Timer control/status register 1	TCSR1	R/(W)*[8]	H'10	H'FFB3
	Timer constant register A1	TCORA1	R/W	H'FF	H'FFB5
	Timer constant register B1	TCORB1	R/W	H'FF	H'FFB7
	Timer counter 1	TCNT1	R/W	H'00	H'FFB9

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Both 8-bit timer channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
WDT	Timer control/status register	TCSR	R/(W)*[10]	H'18	H'FFBC: Write*[9] H'FFBC: Read
	Timer counter	TCNT	R/W	H'00	H'FFBC: Write*[6] H'FFBD: Read
	Reset control/status register	RSTCSR	R/(W)*[10]	H'1F	H'FFBE: Write*[9] H'FFBF: Read
SCI0	Serial mode register 0	SMR0	R/W	H'00	H'FF78
	Bit rate register 0	BRR0	R/W	H'FF	H'FF79
	Serial control register 0	SCR0	R/W	H'00	H'FF7A
	Transmit data register 0	TDR0	R/W	H'FF	H'FF7B
	Serial status register 0	SSR0	R/(W)*[2]	H'84	H'FF7C
	Receive data register 0	RDR0	R	H'00	H'FF7D
	Smart card mode register 0	SCMR0	R/W	H'F2	H'FF7E
SCI1	Serial mode register 1	SMR1	R/W	H'00	H'FF80
	Bit rate register 1	BRR1	R/W	H'FF	H'FF81
	Serial control register 1	SCR1	R/W	H'00	H'FF82
	Transmit data register 1	TDR1	R/W	H'FF	H'FF83
	Serial status register 1	SSR1	R/(W)*[2]	H'84	H'FF84
	Receive data register 1	RDR1	R	H'00	H'FF85
	Smart card mode register 1	SCMR1	R/W	H'F2	H'FF86
SCI2	Serial mode register 2	SMR2	R/W	H'00	H'FF88
	Bit rate register 2	BRR2	R/W	H'FF	H'FF89
	Serial control register 2	SCR2	R/W	H'00	H'FF8A
	Transmit data register 2	TDR2	R/W	H'FF	H'FF8B
	Serial status register 2	SSR2	R/(W)*[2]	H'84	H'FF8C
	Receive data register 2	RDR2	R	H'00	H'FF8D
	Smart card mode register 2	SCMR2	R/W	H'F2	H'FF8E

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
All SCI channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
SMCI0	Serial mode register 0	SMR0	R/W	H'00	H'FF78
	Bit rate register 0	BRR0	R/W	H'FF	H'FF79
	Serial control register 0	SCR0	R/W	H'00	H'FF7A
	Transmit data register 0	TDR0	R/W	H'FF	H'FF7B
	Serial status register 0	SSR0	R/(W)*[2]	H'84	H'FF7C
	Receive data register 0	RDR0	R	H'00	H'FF7D
	Smart card mode register 0	SCMR0	R/W	H'F2	H'FF7E
SMCI1	Serial mode register 1	SMR1	R/W	H'00	H'FF80
	Bit rate register 1	BRR1	R/W	H'FF	H'FF81
	Serial control register 1	SCR1	R/W	H'00	H'FF82
	Transmit data register 1	TDR1	R/W	H'FF	H'FF83
	Serial status register 1	SSR1	R/(W)*[2]	H'84	H'FF84
	Receive data register 1	RDR1	R	H'00	H'FF85
	Smart card mode register 1	SCMR1	R/W	H'F2	H'FF86
SMCI2	Serial mode register 2	SMR2	R/W	H’00	H’FF88
	Bit rate register 2	BRR2	R/W	H’FF	H’FF89
	Serial control register 2	SCR2	R/W	H’00	H’FF8A
	Transmit data register 2	TDR2	R/W	H’FF	H’FF8B
	Serial status register 2	SSR2	R/(W)*[2]	H’84	H’FF8C
	Receive data register 2	RDR2	R	H’00	H’FF8D
	Smart card mode register 2	SCMR2	R/W	H’00	H’FF8E
All SCI channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
ADC	A/D data register AH	ADDRAH	R	H'00	H'FF90
	A/D data register AL	ADDRAL	R	H'00	H'FF91
	A/D data register BH	ADDRBH	R	H'00	H'FF92
	A/D data register BL	ADDRBL	R	H'00	H'FF93
	A/D data register CH	ADDRCH	R	H'00	H'FF94
	A/D data register CL	ADDRCL	R	H'00	H'FF95
	A/D data register DH	ADDRDH	R	H'00	H'FF96

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
ADC	A/D data register DL	ADDRDL	R	H'00	H'FF97
	A/D control/status register	ADCSR	R/(W)*[10]	H'00	H'FF98
	A/D control register	ADCR	R/W	H'3F	H'FF99
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
DAC0, 1	D/A data register 0	DADR0	R/W	H'00	H'FFA4
	D/A data register 1	DADR1	R/W	H'00	H'FFA5
	D/A control register 01	DACR01	R/W	H'1F	H'FFA6
DAC2, 3	D/A data register 2	DADR2	R/W	H'00	H'FDA8
	D/A data register 3	DADR3	R/W	H'00	H'FDA9
	D/A control register 23	DACR23	R/W	H'1F	H'FDAA
All DAC channels	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
On-chip RAM	System control register	SYSCR	R/W	H'01	H'FF39
Flash memory	Flash memory control register 1	FLMCR1*[15]	R/W*[12]	H'00*[13]	H'FFC8*[11]
	Flash memory control register 2	FLMCR2*[15]	R/W*[12]	H'00*[14]	H'FFC9*[11]
	Erase block register 1	EBR1*[15]	R/W*[12]	H'00*[14]	H'FFCA*[11]
	Erase block register 2	EBR2*[15]	R/W*[12]	H'00*[14]	H'FFCB*[11]
	RAM emulation register	RAMER	R/W	H'00	H'FEDB
	System control register 2	SYSCR2*[16]	R/W	H'00	H'FF42
Clock pulse generator	System clock control register	SCKCR	R/W	H'00	H'FF3A
Power-down mode	Standby control register	SBYCR	R/W	H'08	H'FF38
	System clock control register	SCKCR	R/W	H'00	H'FF3A
	Module stop control register H	MSTPCRH	R/W	H'3F	H'FF3C
	Module stop control register L	MSTPCRL	R/W	H'FF	H'FF3D
Port 1	Port 1 data direction register	P1DDR	W	H'00	H'FEB0
	Port 1 data register	P1DR	R/W	H'00	H'FF60
	Port 1 register	PORT1	R	c	H'FF50
Port 2	Port 2 data direction register	P2DDR	W	H'00	H'FEB1
	Port 2 data register	P2DR	R/W	H'00	H'FF61
	Port 2 register	PORT2	R	Undefined	H'FF51

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Port 3	Port 3 data direction register	P3DDR	W	H'00	H'FEB2
	Port 3 data register	P3DR	R/W	H'00	H'FF62
	Port 3 register	PORT3	R	Undefined	H'FF52
	Port 3 open drain control register	P3ODR	R/W	H'00	H'FF76
Port 4	Port 4 register	PORT4	R	Undefined	H'FF53
Port 5	Port 5 data direction register	P5DDR	W	H'0*[21]	H'FEB4
	Port 5 data register	P5DR	R/W	H'0*[21]	H'FF64
	Port 5 register	PORT5	R	Undefined	H'FF54
	Port function control register 2	PFCR2	R/W	H'30	H'FFAC
	System control register	SYSCR	R/W	H'01	H'FF39
Port 6	Port 6 data direction register	P6DDR	W	H'00	H'FEB5
	Port 6 data register	P6DR	R/W	H'00	H'FF65
	Port 6 register	PORT6	R	Undefined	H'FF55
	Port function control register 2	PFCR2	R/W	H'30	H'FFAC
Port 7	Port 7 data direction register	P7DDR	W	H'00	H'FEB6
	Port 7 data register	P7DR	R/W	H'00	H'FF66
	Port 7 register	PORT7	R	Undefined	H'FF56
Port 8	Port 8 data direction register	P8DDR	W	H'00*[17]	H'FEB7
	Port 8 data register	P8DR	R/W	H'00*[17]	H'FF67
	Port 8 register	PORT8	R	Undefined*[17]	H'FF57
	Port function control register 2	PFCR2	R/W	H'30*[17]	H'FFAC
Port 9	Port 9 data direction register	P9DDR	W	H'00*[18]	H'FEB8
	Port 9 data register	P9DR	R/W	H'00*[18]	H'FF68
	Port 9 register	PORT9	R	Undefined	H'FF58
	System control register	SYSCR	R/W	H'01	H'FF39
Port A	Port A data direction register	PADDR	W	H'00	H'FEB9
	Port A data register	PADR	R/W	H'00	H'FF69
	Port A register	PORTA	R	Undefined	H'FF59
	Port A MOS pull-up control register	PAPCR	R/W	H'00	H'FF70
	Port A open drain control register	PAODR	R/W	H'00	H'FF77
	Port function control register 1	PFCR1	R/W	H'0F	H'FF45

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Port B	Port B data direction register	PBDDR	W	H'00	H'FEBA
	Port B data register	PBDR	R/W	H'00	H'FF6A
	Port B register	PORTB	R	Undefined	H'FF5A
	Port B MOS pull-up control register	PBPCR	R/W	H'00	H'FF71
Port C	Port C data direction register	PCDDR	W	H'00	H'FEBB
	Port C data register	PCDR	R/W	H'00	H'FF6B
	Port C register	PORTC	R	Undefined	H'FF5B
	Port C MOS pull-up control register	PCPCR	R/W	H'00	H'FF72
Port D	Port D data direction register	PDDDR	W	H'00	H'FEBC
	Port D data register	PDDR	R/W	H'00	H'FF6C
	Port D register	PORTD	R	Undefined	H'FF5C
	Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FF73
Port E	Port E data direction register	PEDDR	W	H'00	H'FEBD
	Port E data register	PEDR	R/W	H'00	H'FF6D
	Port E register	PORTE	R	Undefined	H'FF5D
	Port E MOS pull-up control register	PEPCR	R/W	H'00	H'FF74
Port F	Port F data direction register	PFDDR	W	H'80/H'00*[19]	H'FEBE
	Port F data register	PFDR	R/W	H'00	H'FF6E
	Port F register	PORTF	R	Undefined	H'FF5E
	Port function control register 2	PFCR2	R/W	H'30	H'FFAC
	System control register	SYSCR	R/W	H'01	H'FF39
Port G	Port G data direction register	PGDDR	W	H'10/H'00 *[19] *[20]	H'FEBF
	Port G data register	PGDR	R/W	H'00*[20]	H'FF6F
	Port G register	PORTG	R	Undefined*[20]	H'FF5F
	Port function control register 2	PFCR2	R/W	H'30	H'FFAC

Notes: 1. Lower 16 bits of the address.
2. Only 0 can be written for flag clearing.
3. Registers in the DTC cannot be read or written to directly.
4. Located as register information in on-chip RAM addresses H'EBC0 to H'EFBF. Cannot be located in external memory space. Do not clear the RAME bit in SYSCR to 0 when using the DTC.
5. Determined by the MCU operating mode.
6. Bits used for pulse output cannot be written to.

7. If the pulse output group 2 and pulse output group 3 output triggers are the same according to the PCR setting, the NDRH address will be H'FF4C, and if different, the address of NDRH for group 2 will be H'FF4E, and that for group 3 will be H'FF4C. Similarly, if the pulse output group 0 and pulse output group 1 output triggers are the same according to the PCR setting, the NDRL address will be H'FF4D, and if different, the address of NDRL for group 0 will be H'FF4F, and that for group 1 will be H'FF4D.
8. Only 0 can be written to bits 7 to 5, to clear the flags.
9. For information on writing, see section 10.2.4, Notes on Register Access, in the Hardware Manual.
10. Only 0 can be written to bit 7, to clear the flag.
11. Flash memory registers selection is performed by means of the FLSHE bit in system control register 2 (SYSCR2).
12. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid. Writes are also disabled when the FWE bit in FLMCR1 is cleared to 0.
13. When a high level is input to the FWE pin, the initial value is H'80.
14. When a low level is input to the FWE pin, or if a high level is input but the SWE bit in FLMCR1 is not set, these registers are initialized to H'00.
15. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers. Only byte access can be used on these registers, with the access requiring two states.
16. The SYSCR2 register can only be used in the F-ZTAT version. In the mask ROM version this register will return an undefined value if read, and cannot be written to.
17. Value of bits 6 to 0.
18. Value of bits 7 to 2.
19. The initial value depends on the mode.
20. Value of bits 4 to 0.
21 Value of bits 3 to 0.

8.3 Functions

MRA—DTC Mode Register A **H'F800—H'FBFF** **DTC**

Bit	7	6	5	4	3	2	1	0
	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

DTC Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

DTC Transfer Mode Select

0	Destination side is repeat area or block area
1	Source side is repeat area or block area

DTC Mode

0	0	Normal mode
	1	Repeat mode
1	0	Block transfer mode
	1	—

Destination Address Mode

0	—	DAR is fixed
1	0	DAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1)
	1	DAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)

Source Address Mode

0	—	SAR is fixed
1	0	SAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1)
	1	SAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)

Bit	7	6	5	4	3	2	1	0
	CHNE	DISEL	CHNS	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

Reserved
Only 0 should be written to these bits

DTC Chain Transfer Enable, DTC Chain Transfer Select

CHNE	CHNS	Description
0	—	No chain transfer. (At end of DTC data transfer, DTC waits for activation)
1	0	Chain transfer every time
1	1	Chain transfer only when transfer counter = 0

DTC Interrupt Select

0	After DTC data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0
1	After DTC data transfer ends, the CPU interrupt is enabled

SAR—DTC Source Address Register **H'F800—H'FBFF** **DTC**

Bit	23	22	21	20	19	- - -	4	3	2	1	0
						- - -					
Initial value	Unde-fined	Unde-fined	Unde-fined	Unde-fined	Unde-fined	- - -	Unde-fined	Unde-fined	Unde-fined	Unde-fined	Unde-fined
Read/Write	—	—	—	—	—	- - -	—	—	—	—	—

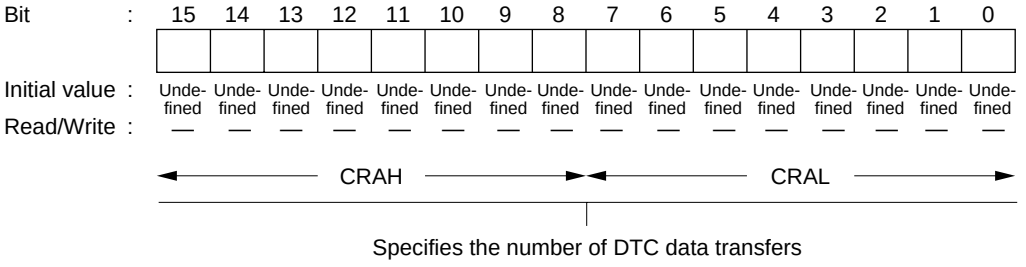
Specifies DTC transfer data source address

DAR—DTC Destination Address Register **H'F800—H'FBFF** **DTC**

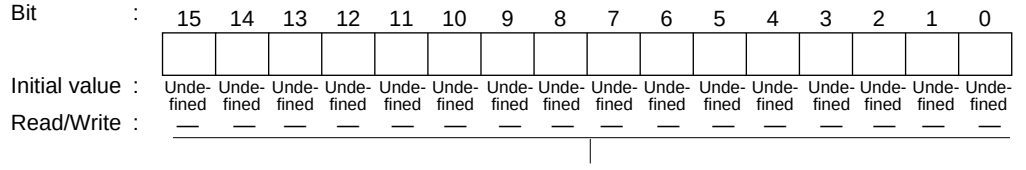
Bit	23	22	21	20	19	- - -	4	3	2	1	0
						- - -					
Initial value	Unde-fined	Unde-fined	Unde-fined	Unde-fined	Unde-fined	- - -	Unde-fined	Unde-fined	Unde-fined	Unde-fined	Unde-fined
Read/Write	—	—	—	—	—	- - -	—	—	—	—	—

Specifies DTC transfer data destination address

CRA—DTC Transfer Count Register A H'F800—H'FBFF DTC



CRB—DTC Transfer Count Register B H'F800—H'FBFF DTC



Bit :	7	6	5	4	3	2	1	0
	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Timer Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	Internal clock: counts on ø/1024
	1	0	Internal clock: counts on ø/256
		1	Internal clock: counts on ø/4096

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Counter Clear

0	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRA compare match/input capture
	1	0	TCNT cleared by TGRB compare match/input capture
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation *1
1	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRC compare match/input capture *2
	1	0	TCNT cleared by TGRD compare match/input capture *2
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation *1

Notes: 1. Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.
2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

Buffer Operation A

0	TGRA operates normally
1	TGRA and TGRC used together for buffer operation

Buffer Operation B

0	TGRB operates normally
1	TGRB and TGRD used together for buffer operation

Bit	7	6	5	4	3	2	1	0
Initial value	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR3A I/O Control

0	0	0	0	TGR3A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3A is input capture register	Capture input source is $TIOCA_3$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down

* : Don't care

TGR3B I/O Control

0	0	0	0	TGR3B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3B is input capture register	Capture input source is $TIOCB_3$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down*1

* : Don't care

Note: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000, and ø/1 is used as the TCNT4 count clock, this setting is invalid and input capture does not occur.

Bit	:	7	6	5	4	3	2	1	0
		IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR3C I/O Control

0	0	0	0	TGR3C is output compare register*1	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3C is input capture register*1	Capture input source is $TIOCC_3$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down

* : Don't care

Note: 1. When the BFA bit in TMDR3 is set to 1 and TGR3C is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

TGR3D I/O Control

0	0	0	0	TGR3D is output compare register *2	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3D is input capture register *2	Capture input source is $TIOCD_3$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down*1

* : Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000 and ø/1 is used as the TCNT4 count clock, this setting is invalid and input capture does not occur.
2. When the BFB bit in TMDR3 is set to 1 and TGR3D is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

Note: When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

Bit	7	6	5	4	3	2	1	0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

TGR Interrupt Enable C

0	Interrupt request (TGIC) by TGFC bit disabled
1	Interrupt request (TGIC) by TGFC bit enabled

TGR Interrupt Enable D

0	Interrupt request (TGID) by TGFD bit disabled
1	Interrupt request (TGID) by TGFD bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit :	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value :	1	1	0	0	0	0	0	0
Read/Write :	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT=TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Input Capture/Output Compare Flag C

0	[Clearing conditions] • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

Input Capture/Output Compare Flag D

0	[Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Note: * Can only be written with 0 for flag clearing.

TCNT3—Timer Counter 3 **H'FE86** **TPU3**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up-counter

TGR3A—Timer General Register 3A **H'FE88** **TPU3**
TGR3B—Timer General Register 3B **H'FE8A** **TPU3**
TGR3C—Timer General Register 3C **H'FE8C** **TPU3**
TGR3D—Timer General Register 3D **H'FE8E** **TPU3**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Timer Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKC pin input
	1	0	Internal clock: counts on ø/1024
		1	Counts on TCNT5 overflow/underflow

Note: This setting is ignored when channel 4 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 4 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit :	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR4A I/O Control

0	0	0	0	TGR4A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4A is input capture register	Capture input source is $TIOCA_4$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR3A compare match/ input capture	Input capture at generation of TGR3A compare match/input capture

* : Don't care

TGR4B I/O Control

0	0	0	0	TGR4B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4B is input capture register	Capture input source is $TIOCB_4$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR3C compare match/ input capture	Input capture at generation of TGR3C compare match/input capture

* : Don't care

Bit :	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value :	0	1	0	0	0	0	0	0
Read/Write :	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

TCNT4—Timer Counter 4 **H'FE96** **TPU4**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR4A—Timer General Register 4A **H'FE98** **TPU4**

TGR4B—Timer General Register 4B **H'FE9A** **TPU4**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKC pin input
	1	0	Internal clock: counts on ø/256
		1	External clock: counts on TCLKD pin input

Note: This setting is ignored when channel 5 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 5 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	:	7	6	5	4	3	2	1	0
		IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR5A I/O Control

0	0	0	0	TGR5A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR5A is input capture register	Capture input source is $TIOCA_5$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

TGR5B I/O Control

0	0	0	0	TGR5B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR5B is input capture register	Capture input source is $TIOCB_5$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

Bit :	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value :	0	1	0	0	0	0	0	0
Read/Write :	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit :	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value :	1	1	0	0	0	0	0	0
Read/Write :	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

TCNT5—Timer Counter 5 **H'FEA6** **TPU5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR5A—Timer General Register 5A **H'FEA8** **TPU5**
TGR5B—Timer General Register 5B **H'FEAA** **TPU5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1DDR—Port 1 Data Direction Register **H'FEB0** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port 1 pins

P2DDR—Port 2 Data Direction Register **H'FEB1** **Port 2**

Bit :	7	6	5	4	3	2	1	0
	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	W	W	W	W	W	W	W	W

Specify input or output for individual port 2 pins

P3DDR—Port 3 Data Direction Register **H'FEB2** **Port 3**

Bit :	7	6	5	4	3	2	1	0
	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR
Initial value :	Undefined	Undefined	0	0	0	0	0	0
Read/Write :	—	—	W	W	W	W	W	W

Specify input or output for individual port 3 pins

P5DDR—Port 5 Data Direction Register **H'FEB4** **Port 5**

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR
Initial value :	Undefined	Undefined	Undefined	Undefined	0	0	0	0
Read/Write :	—	—	—	—	W	W	W	W

Specify input or output for individual port 5 pins

P6DDR—Port 6 Data Direction Register H'FEB5 Port 6

Bit :	7	6	5	4	3	2	1	0
	P67DDR	P66DDR	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	W	W	W	W	W	W	W	W

Specify input or output for individual port 6 pins

P7DDR—Port 7 Data Direction Register H'FEB6 Port 7

Bit :	7	6	5	4	3	2	1	0
	—	—	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR
Initial value :	Undefined	Undefined	0	0	0	0	0	0
Read/Write :	—	—	W	W	W	W	W	W

Specify input or output for individual port 7 pins

P8DDR—Port 8A Data Direction Register H'FEB7 Port 8

Bit :	7	6	5	4	3	2	1	0
	—	P86DDR	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR
Initial value :	Undefined	0	0	0	0	0	0	0
Read/Write :	—	W	W	W	W	W	W	W

Specify input or output for individual port 8 pins

P9DDR—Port 9A Data Direction Register H'FEB8 Port 9

Bit	7	6	5	4	3	2	1	0
	P97DDR	P96DDR	P95DDR	P94DDR	P93DDR	P92DDR	—	—
Initial value	0	0	0	0	0	0	Undefined	Undefined
Read/Write	W	W	W	W	W	W	—	—

Specify input or output for individual port 9 pins

PADDR—Port A Data Direction Register H'FEB9 Port A

Bit	7	6	5	4	3	2	1	0
	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port A pins

PBDDR—Port B Data Direction Register H'FEBA Port B

Bit	7	6	5	4	3	2	1	0
	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port B pins

PCDDR—Port C Data Direction Register **H'FEBB** **Port C**

Bit	:	7	6	5	4	3	2	1	0
		PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port C pins

PDDDR—Port D Data Direction Register **H'FEBC** **Port D**

Bit	:	7	6	5	4	3	2	1	0
		PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port D pins

PEDDR—Port E Data Direction Register **H'FEBD** **Port E**

Bit	:	7	6	5	4	3	2	1	0
		PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port E pins

PFDDR—Port F Data Direction Register **H'FEBE** **Port F**

Bit	:	7	6	5	4	3	2	1	0
		PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 4 to 6									
Initial value	:	1	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W
Mode 7									
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port F pins

PGDDR—Port G Data Direction Register **H'FEBF** **Port G**

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 4 and 5									
Initial value	:	Undefined	Undefined	Undefined	1	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W
Modes 6 and 7									
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W

Specify input or output for individual port G pins

IPRA — Interrupt Priority Register A	**H'FEC4**	**Interrupt Controller**
IPRB — Interrupt Priority Register B	**H'FEC5**	**Interrupt Controller**
IPRC — Interrupt Priority Register C	**H'FEC6**	**Interrupt Controller**
IPRD — Interrupt Priority Register D	**H'FEC7**	**Interrupt Controller**
IPRE — Interrupt Priority Register E	**H'FEC8**	**Interrupt Controller**
IPRF — Interrupt Priority Register F	**H'FEC9**	**Interrupt Controller**
IPRG — Interrupt Priority Register G	**H'FECA**	**Interrupt Controller**
IPRH — Interrupt Priority Register H	**H'FECB**	**Interrupt Controller**
IPRI — Interrupt Priority Register I	**H'FECC**	**Interrupt Controller**
IPRJ — Interrupt Priority Register J	**H'FECD**	**Interrupt Controller**
IPRK — Interrupt Priority Register K	**H'FECE**	**Interrupt Controller**

Bit	7	6	5	4	3	2	1	0
	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0
Initial value	0	1	1	1	0	1	1	1
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Set priority (levels 7 to 0) for interrupt sources

Correspondence between Interrupt Sources and IPR Settings

Register	Bits	
	6 to 4	2 to 0
IPRA	IRQ0	IRQ1
IPRB	IRQ2	IRQ4
	IRQ3	IRQ5
IPRC	IRQ6	DTC
	IRQ7	
IPRD	WDT	Refresh timer
IPRE	—*	A/D converter
IPRF	TPU channel 0	TPU channel 1
IPRG	TPU channel 2	TPU channel 3
IPRH	TPU channel 4	TPU channel 5
IPRI	8-bit timer channel 0	8-bit timer channel 1
IPRJ	DMAC	SCI channel 0
IPRK	SCI channel 1	SCI channel 2

Note: * Reserved bits.

Bit	7	6	5	4	3	2	1	0
	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 5 to 7								
Initial value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 4								
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Bus Width Control

0	Area n is designated for 16-bit access
1	Area n is designated for 8-bit access

(n = 7 to 0)

ASTCR—Access State Control Register **H'FED1** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Access State Control

0	Area n is designated for 2-state access Wait state insertion in area n external space is disabled
1	Area n is designated for 3-state access Wait state insertion in area n external space is enabled

(n = 7 to 0)

Bit :	7	6	5	4	3	2	1	0
	W71	W70	W61	W60	W51	W50	W41	W40
Initial value :	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 4 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 5 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 6 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 7 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Bit	:	7	6	5	4	3	2	1	0
		W31	W30	W21	W20	W11	W10	W01	W00
Initial value	:	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 0 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 1 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 2 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Area 3 Wait Control

0	0	Program wait not inserted
	1	1 program wait state inserted
1	0	2 program wait states inserted
	1	3 program wait states inserted

Bit :	7	6	5	4	3	2	1	0
	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2	RMTS1	RMTS0
Initial value :	1	1	0	1	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RAM Type Select

RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	0	Normal space			
		1	Normal space			DRAM space
	1	0	Normal space		DRAM space	
		1	DRAM space			
1	—	—	—			

Note: When areas selected in DRAM space are all 8-bit space, the PF_2 pin can be used as an I/O port or $\overline{BREQO}$.

Burst Cycle Select 0

0	Max. 4 words in burst access
1	Max. 8 words in burst access

Burst Cycle Select 1

0	Burst cycle comprises 1 state
1	Burst cycle comprises 2 states

Area 0 Burst ROM Enable

0	Basic bus interface
1	Burst ROM interface

Idle Cycle Insert 0

0	Idle cycle not inserted in case of successive external read and external write cycles
1	Idle cycle inserted in case of successive external read and external write cycles

Idle Cycle Insert 1

0	Idle cycle not inserted in case of successive external read cycles in different areas
1	Idle cycle inserted in case of successive external read cycles in different areas

Bit	7	6	5	4	3	2	1	0
	BRLE	BREQOE	EAE	—	DDS	—	WDBE	WAITE
Initial value	0	0	1	0	1	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WAIT Pin Enable

0	Wait input by $\overline{\text{WAIT}}$* pin disabled
1	Wait input by $\overline{\text{WAIT}}$* pin enabled

Note: * The $\overline{\text{WAIT}}$ input pin can be switched between $P8_6$ and $P5_3$ by means of WAITPS.

Write Data Buffer Enable

0	Write data buffer function not used
1	Write data buffer function used

Reserved

DACK Timing Select

0	When DMAC single address transfer is performed in DRAM space, full access is always executed. $\overline{\text{DACK}}$ signal goes low from Tr or T1 cycle
1	Burst access is possible when DMAC single address transfer is performed in DRAM space. $\overline{\text{DACK}}$ signal goes low from Tc1 or T2 cycle

Reserved

External Address Enable

0	• In the H8S/2339 and H8S/2338, addresses H'010000 to H'03FFFF*2 are on-chip ROM • In the H8S/2337, addresses H'010000 to H'01FFFF are on-chip ROM, and addresses H'020000 to H'03FFFF are a reserved area*1 • In the H8S/2332, addresses H'010000 to H'03FFFF are a reserved area*1
1	Addresses H'010000 to H'03FFFF*2 are external addresses in external expanded mode or reserved area*1 in single-chip mode

Notes: 1. Do not access a reserved area.
2. Addresses H'010000 to H'05FFFF in the H8S/2339.

BREQO Pin Enable

0	$\overline{\text{BREQO}}$* output disabled
1	$\overline{\text{BREQO}}$* output enabled

Note: * $\overline{\text{BREQO}}$ output pin can be switched between PF_2 and $P5_3$ by means of BREQOPS.

Bus Release Enable

0	External bus release disabled
1	External bus release enabled

Bit :	7	6	5	4	3	2	1	0
	TPC	BE	RCDM	—	MXC1	MXC0	RLW1	RLW0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Refresh Cycle Wait Control

0	0	No wait state inserted
	1	1 wait state inserted
1	0	2 wait states inserted
	1	3 wait states inserted

Multiplex Shift Count

0	0	8-bit shift
	1	9-bit shift
1	0	10-bit shift
	1	—

Reserved

RAS Down Mode

0	RAS up mode selected for DRAM interface
1	RAS down mode selected for DRAM interface

Burst Access Enable

0	Burst disabled (always full access)
1	For DRAM space access, access in fast page mode

TP Cycle Control

0	1-state precharge cycle is inserted
1	2-state precharge cycle is inserted

Bit :	7	6	5	4	3	2	1	0
	RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Refresh Counter Clock Select

0	0	0	Count operation disabled
		1	Count uses ø/2
	1	0	Count uses ø/8
		1	Count uses ø/32
1	0	0	Count uses ø/128
		1	Count uses ø/512
	1	0	Count uses ø/2048
		1	Count uses ø/4096

Compare Match Interrupt Enable

0	Interrupt request (CMI) by CMF flag disabled
1	Interrupt request (CMI) by CMF flag enabled

Compare Match Flag

0	[Clearing condition] When 0 is written to CMF after reading CMF = 1
1	[Setting condition] When RTCNT = RTCOR

Refresh Mode

0	Self-refreshing is not performed in software standby mode
1	Self-refreshing is performed in software standby mode

RAS-CAS Wait

0	Wait state insertion in CAS-before-RAS refreshing disabled $\overline{RAS}$ falls in T_r cycle
1	One wait state inserted in CAS-before-RAS refreshing $\overline{RAS}$ falls in T_{c1} cycle

Refresh Control

0	Refresh control is not performed
1	Refresh control is performed

RTCNT—Refresh Timer Counter **H'FED8** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Internal clock count value

RTCOR—Refresh Time Constant Register **H'FED9** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sets the period for compare match operations with RTCNT

RAMER—RAM Emulation Register **H'FEDB** **Bus Controller (F-ZTAT version only)**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

RAM Select, Flash Memory Area Select

RAMS	RAM2	RAM1	RAM0	RAM Area	Block Name
0	*	*	*	H'FFDC00 to H'FFEBFF	RAM area, 4 kbytes
1	0	0	0	H'000000 to H'000FFF	EB0 (4 kbytes)
			1	H'001000 to H'001FFF	EB1 (4 kbytes)
		1	0	H'002000 to H'002FFF	EB2 (4 kbytes)
			1	H'003000 to H'003FFF	EB3 (4 kbytes)
	1	0	0	H'004000 to H'004FFF	EB4 (4 kbytes)
			1	H'005000 to H'005FFF	EB5 (4 kbytes)
		1	0	H'006000 to H'006FFF	EB6 (4 kbytes)
			1	H'007000 to H'007FFF	EB7 (4 kbytes)

*: Don't care

MAR0AH—Memory Address Register 0AH **H'FEE0** **DMAC**
MAR0AL—Memory Address Register 0AL **H'FEE2** **DMAC**

Bit	:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR0AH	:	—	—	—	—	—	—	—	—								
Initial value	:	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR0AL	:																
Initial value	:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Transfer destination address

IOAR0A—I/O Address Register 0A **H'FEE4** **DMAC**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR0A	:																
Initial value	:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Not used

ETCR0A—Transfer Count Register 0A **H'FEE6** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR0A																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode
Idle mode
Normal mode: Transfer counter

Repeat mode: Transfer number storage register / Transfer counter

Block transfer mode: Block size storage register / Block size counter

* : Undefined

MAR0BH—Memory Address Register 0BH **H'FEE8** **DMAC**
MAR0BL—Memory Address Register 0BL **H'FEEA** **DMAC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR0BH	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR0BL																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Transfer destination address

IOAR0B—I/O Address Register 0B **H'FEEC** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR0B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Not used

ETCR0B—Transfer Count Register 0B **H'FEEE** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR0B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode and idle mode	Transfer counter	
Repeat mode	Transfer number storage register	Transfer counter
Block transfer mode	Block transfer counter	

* : Undefined

Note: Not used in normal mode.

MAR1AH—Memory Address Register 1AH **H'FEF0** **DMAC**
MAR1AL—Memory Address Register 1AL **H'FEF2** **DMAC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR1AH	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR1AL																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Transfer destination address

IOAR1A—I/O Address Register 1A **H'FEF4** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR1A																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Not used

ETCR1A—Transfer Count Register 1A H'FEF6 DMAC

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR1A	:																
Initial value	:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode
Idle mode
Normal mode: Transfer counter

Repeat mode: Transfer number storage register; Transfer counter

Block transfer mode: Block size storage register; Block size counter

* : Undefined

MAR1BH— Memory Address Register 1BH H'FEF8 DMAC
MAR1BL — Memory Address Register 1BL H'FEFA DMAC

Bit	:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR1BH	:	—	—	—	—	—	—	—	—								
Initial value	:	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR1BL	:																
Initial value	:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Transfer destination address

IOAR1B—I/O Address Register 1B **H'FEFC** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR1B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Not used

ETCR1B—Transfer Count Register 1B **H'FEFE** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR1B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode and idle mode: Transfer counter

Repeat mode: Transfer number storage register / Transfer counter

Block transfer mode: Block transfer counter

* : Undefined

Note: Not used in normal mode.

Bit	7	6	5	4	3	2	1	0
DMAWER	—	—	—	—	WE1B	WE1A	WE0B	WE0A
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Write Enable 0A

0	Writes to all bits in DMACR0A, and bits 8, 4, and 0 in DMABCR are disabled
1	Writes to all bits in DMACR0A, and bits 8, 4, and 0 in DMABCR are enabled

Write Enable 0B

0	Writes to all bits in DMACR0B, bits 9, 5, and 1 in DMABCR, and bit 4 in DMATCR are disabled
1	Writes to all bits in DMACR0B, bits 9, 5, and 1 in DMABCR, and bit 4 in DMATCR are enabled

Write Enable 1A

0	Writes to all bits in DMACR1A, and bits 10, 6, and 2 in DMABCR are disabled
1	Writes to all bits in DMACR1A, and bits 10, 6, and 2 in DMABCR are enabled

Write Enable 1B

0	Writes to all bits in DMACR1B, bits 11, 7, and 3 in DMABCR, and bit 5 in DMATCR are disabled
1	Writes to all bits in DMACR1B, bits 11, 7, and 3 in DMABCR, and bit 5 in DMATCR are enabled

Bit :	7	6	5	4	3	2	1	0
DMATCR :	—	—	TEE1	TEE0	—	—	—	—
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	—	—	R/W	R/W	—	—	—	—

Transfer End Enable 0

0	$\overline{\text{TEND}}_0$ pin output disabled
1	$\overline{\text{TEND}}_0$ pin output enabled

Transfer End Enable 1

0	$\overline{\text{TEND}}_1$ pin output disabled
1	$\overline{\text{TEND}}_1$ pin output enabled

Full address mode

Bit :	15	14	13	12	11	10	9	8
DMACRA :	DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Block Direction/Block Enable

0	0	Transfer in normal mode
	1	Transfer in block transfer mode, destination side is block area
1	0	Transfer in normal mode
	1	Transfer in block transfer mode, source side is block area

Source Address Increment/Decrement

0	0	MARA is fixed
	1	MARA is incremented after a data transfer
1	0	MARA is fixed
	1	MARA is decremented after a data transfer

Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

Full address mode (cont)

Bit	7	6	5	4	3	2	1	0
DMACRB	—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data Transfer Factor

DTF 3	DTF 2	DTF 1	DTF 0	Block Transfer Mode	Normal Mode
0	0	0	0	—	—
			1	Activated by A/D converter conversion end interrupt	—
		1	0	Activated by $\overline{\text{DREQ}}$ pin falling edge input	Activated by $\overline{\text{DREQ}}$ pin falling edge input
			1	Activated by $\overline{\text{DREQ}}$ pin low-level input	Activated by $\overline{\text{DREQ}}$ pin low-level input
	1	0	0	Activated by SCI channel 0 transmission complete interrupt	—
			1	Activated by SCI channel 0 reception complete interrupt	—
		1	0	Activated by SCI channel 1 transmission complete interrupt	Auto-request (cycle steal)
			1	Activated by SCI channel 1 reception complete interrupt	Auto-request (burst)
1	0	0	0	Activated by TPU channel 0 compare match/input capture A interrupt	—
			1	Activated by TPU channel 1 compare match/input capture A interrupt	—
		1	0	Activated by TPU channel 2 compare match/input capture A interrupt	—
			1	Activated by TPU channel 3 compare match/input capture A interrupt	—
	1	0	0	Activated by TPU channel 4 compare match/input capture A interrupt	—
			1	Activated by TPU channel 5 compare match/input capture A interrupt	—
		1	0	—	—
			1	—	—

Destination Address Increment/Decrement

0	0	MARB is fixed
	1	MARB is incremented after a data transfer
1	0	MARB is fixed
	1	MARB is decremented after a data transfer

Short address mode

Bit	7	6	5	4	3	2	1	0
DMACR	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data Transfer Factor

				Channel A	Channel B
0	0	0	0	—	
			1	Activated by A/D converter conversion end interrupt	
		1	0	—	Activated by $\overline{\text{DREQ}}$ pin falling edge input
			1	—	Activated by $\overline{\text{DREQ}}$ pin low-level input
	1	0	0	Activated by SCI channel 0 transmission complete interrupt	
			1	Activated by SCI channel 0 reception complete interrupt	
		1	0	Activated by SCI channel 1 transmission complete interrupt	
			1	Activated by SCI channel 1 reception complete interrupt	
1	0	0	0	Activated by TPU channel 0 compare match/input capture A interrupt	
			1	Activated by TPU channel 1 compare match/input capture A interrupt	
		1	0	Activated by TPU channel 2 compare match/input capture A interrupt	
			1	Activated by TPU channel 3 compare match/input capture A interrupt	
	1	0	0	Activated by TPU channel 4 compare match/input capture A interrupt	
			1	Activated by TPU channel 5 compare match/input capture A interrupt	
		1	0	—	
			1	—	

Data Transfer Direction

0	Dual address mode: Transfer with MAR as source address and IOAR as destination address Single address mode: Transfer with MAR as source address and $\overline{\text{DACK}}$ pin as write strobe
1	Dual address mode: Transfer with IOAR as source address and MAR as destination address Single address mode: Transfer with $\overline{\text{DACK}}$ pin as read strobe and MAR as destination address

Repeat Enable

0	Transfer in sequential mode
1	Transfer in repeat mode or idle mode

Data Transfer Increment/Decrement

0	MAR is incremented after a data transfer
1	MAR is decremented after a data transfer

Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

Full address mode

Bit :	15	14	13	12	11	10	9	8
DMABCRH :	FAE1	FAE0	—	—	DTA1	—	DTA0	—
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0 Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1 Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0 Full Address Enable

0	Short address mode
1	Full address mode

Channel 1 Full Address Enable

0	Short address mode
1	Full address mode

(Continued on next page)

Full address mode (cont)

Bit	7	6	5	4	3	2	1	0
DMABCRL	DTME1	DTE1	DTME0	DTE0	DTIE1B	DTIE1A	DTIE0B	DTIE0A
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0 Data Transfer Interrupt Enable A

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 0 Data Transfer Interrupt Enable B

0	Transfer suspended interrupt disabled
1	Transfer suspended interrupt enabled

Channel 1 Data Transfer Interrupt Enable A

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 1 Data Transfer Interrupt Enable B

0	Transfer suspended interrupt disabled
1	Transfer suspended interrupt enabled

Channel 0 Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 0 Data Transfer Master Enable

0	Data transfer disabled. In burst mode, cleared to 0 by an NMI interrupt
1	Data transfer enabled

Channel 1 Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 1 Data Transfer Master Enable

0	Data transfer disabled. In burst mode, cleared to 0 by an NMI interrupt
1	Data transfer enabled

(Continued on next page)

Short address mode

Bit	:	15	14	13	12	11	10	9	8
DMABCRH	:	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0A Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0B Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1A Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1B Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0B Single Address Enable

0	Transfer in dual address mode
1	Transfer in single address mode

Channel 1B Single Address Enable

0	Transfer in dual address mode
1	Transfer in single address mode

Channel 0 Full Address Enable

0	Short address mode
1	Full address mode

Channel 1 Full Address Enable

0	Short address mode
1	Full address mode

(Continued on next page)

Short address mode (cont)

Bit	7	6	5	4	3	2	1	0
DMABCRL	DTE1B	DTE1A	DTE0B	DTE0A	DTIE1B	DTIE1A	DTIE0B	DTIE0A
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0A Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 0B Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 1A Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 1B Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 0A Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 0B Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 1A Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 1B Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

ISCRH

Bit	:	15	14	13	12	11	10	9	8
		IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ7 to IRQ4 Sense Control

ISCRL

Bit	:	7	6	5	4	3	2	1	0
		IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ3 to IRQ0 Sense Control

IRQnSCB	IRQnSCA	Interrupt Request Generation
0	0	$\overline{IRQ}_n$ input low level
	1	Falling edge of $\overline{IRQ}_n$ input
1	0	Rising edge of $\overline{IRQ}_n$ input
	1	Both falling and rising edges of $\overline{IRQ}_n$ input

(n = 7 to 0)

IER—IRQ Enable Register **H'FF2E** **Interrupt Controller**

Bit	7	6	5	4	3	2	1	0
	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQn Enable

0	IRQn interrupt disabled
1	IRQn interrupt enabled

(n = 7 to 0)

ISR—IRQ Status Register **H'FF2F** **Interrupt Controller**

Bit	7	6	5	4	3	2	1	0
	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Indicate the status of IRQ7 to IRQ0 interrupt requests

Note: * Can only be written with 0 for flag clearing.

Bit :	7	6	5	4	3	2	1	0
	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DTC Activation Enable

0	DTC activation by this interrupt is disabled [Clearing conditions] • When the DISEL bit is 1 and data transfer has ended • When the specified number of transfers have ended
1	DTC activation by this interrupt is enabled [Holding condition] When the DISEL bit is 0 and the specified number of transfers have not ended

Correspondence between Interrupt Sources and DTCER

	Bits							
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DTCERA	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7
DTCERB	—	ADI	TGI0A	TGI0B	TGI0C	TGI0D	TGI1A	TGI1B
DTCERC	TGI2A	TGI2B	TGI3A	TGI3B	TGI3C	TGI3D	TGI4A	TGI4B
DTCERD	—	—	TGI5A	TGI5B	CMIA0	CMIB0	CMIA1	CMIB1
DTCERE	DMTEND0A	DMTEND0B	DMTEND1A	DMTEND1B	RXI0	TXI0	RXI1	TXI1
DTCERF	RXI2	TXI2	—	—	—	—	—	—

Note: For DTCE bit setting, read/write operations must be performed using bit-manipulation instructions such as BSET and BCLR. For the initial setting only, however, when multiple activation sources are set at one time, it is possible to disable interrupts and write after executing a dummy read on the relevant register.

Bit :	7	6	5	4	3	2	1	0
	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Sets vector number for DTC software activation

DTC Software Activation Enable

0	DTC software activation is disabled [Clearing conditions] • When the DISEL bit is 0 and the specified number of transfers have not ended • When SWDTEND is requested to the CPU, then 0 is written to the SWDTE bit
1	DTC software activation is enabled [Holding conditions] • When the DISEL bit is 1 and data transfer has ended • When the specified number of transfers have ended • During data transfer due to software activation

Note: * DTVEC6 to DTVEC0 bits can be written to when SWDTE = 0.

Bit :	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	OPE	—	—	IRQ37S
Initial value :	0	0	0	0	1	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	—	—	R/W

IRQ37 Software Standby Clear Select

0	$\overline{IRQ}_3$ to $\overline{IRQ}_7$ cannot be used as software standby mode clearing sources
1	$\overline{IRQ}_3$ to $\overline{IRQ}_7$ can be used as software standby mode clearing sources

Output Port Enable

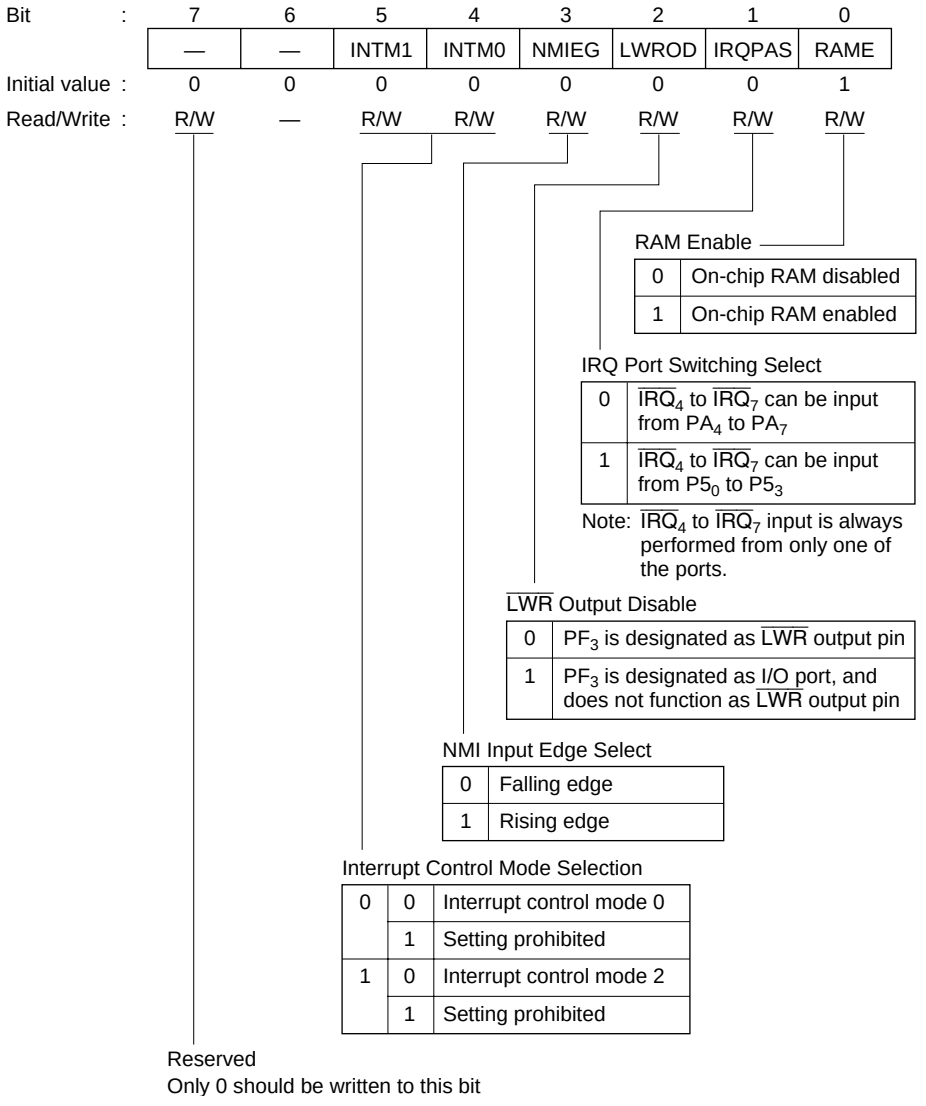
0	In software standby mode, address bus and bus control signals are high-impedance
1	In software standby mode, address bus and bus control signals retain output state

Standby Timer Select

0	0	0	Standby time = 8192 states
		1	Standby time = 16384 states
	1	0	Standby time = 32768 states
		1	Standby time = 65536 states
1	0	0	Standby time = 131072 states
		1	Standby time = 262144 states
	1	0	Reserved
		1	Standby time = 16 states

Software Standby

0	Transition to sleep mode after execution of SLEEP instruction
1	Transition to software standby mode after execution of SLEEP instruction


Bit : 7 6 5 4 3 2 1 0
— — INTM1 INTM0 NMIEG LWROD IRQPAS RAME
Initial value : 0 0 0 0 0 0 0 1
Read/Write : R/W — R/W R/W R/W R/W R/W R/W
RAM Enable
0 On-chip RAM disabled
1 On-chip RAM enabled
IRQ Port Switching Select
0 IRQ4 to IRQ7 can be input from PA4 to PA7
1 IRQ4 to IRQ7 can be input from P50 to P53
Note: IRQ4 to IRQ7 input is always performed from only one of the ports.
LWR Output Disable
0 PF3 is designated as LWR output pin
1 PF3 is designated as I/O port, and does not function as LWR output pin
NMI Input Edge Select
0 Falling edge
1 Rising edge
Interrupt Control Mode Selection
0 0 Interrupt control mode 0
1 Setting prohibited
1 0 Interrupt control mode 2
1 Setting prohibited
Reserved
Only 0 should be written to this bit

Bit	7	6	5	4	3	2	1	0
	PSTOP	—	DIV	—	—	SCK2	SCK1	SCK0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

Division Ratio Select

Reserved
Only 0 should be written to this bit

System Clock Select

			DIV = 0	DIV = 1
0	0	0	Bus master is in high-speed mode	Bus master is in high-speed mode
		1	Medium-speed clock is ø/2	Clock supplied to entire chip is ø/2
	1	0	Medium-speed clock is ø/4	Clock supplied to entire chip is ø/4
		1	Medium-speed clock is ø/8	Clock supplied to entire chip is ø/8
1	0	0	Medium-speed clock is ø/16	—
		1	Medium-speed clock is ø/32	—
	1	—	—	—

ø Clock Output Control

PSTOP	Normal Operation	Sleep Mode	Software Standby Mode	Hardware Standby Mode
0	ø output	ø output	Fixed high	High impedance
1	Fixed high	Fixed high	Fixed high	High impedance

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	1	0	0	0	0	—*	—*	—*
Read/Write	—	—	—	—	—	R	R	R

Current mode pin operating mode

Note: * Determined by pins MD_2 to MD_0

MSTPCRH — Module Stop Control Register H H'FF3C Power-Down State
MSTPCRL — Module Stop Control Register L H'FF3D Power-Down State

	MSTPCRH								MSTPCRL							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies module stop mode

0	Module stop mode cleared
1	Module stop mode set

MSTP Bits and On-Chip Supporting Modules

Register	Bits	Module
MSTPCRH	MSTP15	DMAC
	MSTP14	DTC
	MSTP13	TPU
	MSTP12	8-bit timer
	MSTP11	PPG
	MSTP10	DA0,1
	MSTP9	A/D
	MSTP8	—
MSTPCRL	MSTP7	SCI2
	MSTP6	SCI1
	MSTP5	SCI0
	MSTP4	DA2, 3
	MSTP3	-
	MSTP2	-
	MSTP1	-
	MSTP0	-

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	FLSHE	—	—	—
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	—	—	—

Flash Memory Control Register Enable

0	Flash memory control register is not selected
1	Flash memory control register is selected

Reserved Register **H'FF44**

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	—	R/W	—	—	—	—	—

Reserved
Only 0 should be written to these bits

PFCR1—Port Function Control Register 1 H'FF45

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	A23E	A22E	A21E	A20E
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address 20 Output Enable*

0	PA4DR is output when PA4DDR = 1
1	A_{20} is output when PA4DDR = 1

Address 21 Output Enable*

0	PA5DR is output when PA5DDR = 1
1	A_{21} is output when PA5DDR = 1

Address 22 Output Enable*

0	PA6DR is output when PA6DDR = 1
1	A_{22} is output when PA6DDR = 1

Address 23 Output Enable*

0	PA7DR is output when PA7DDR = 1
1	A_{23} is output when PA7DDR = 1

Note: * Valid only in modes 4 to 6.

Reserved
Only 0 should be written to these bits

Bit	7	6	5	4	3	2	1	0
	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output Trigger for Pulse Output Group 0

0	0	Compare match in TPU channel 0
	1	Compare match in TPU channel 1
1	0	Compare match in TPU channel 2
	1	Compare match in TPU channel 3

Output Trigger for Pulse Output Group 1

0	0	Compare match in TPU channel 0
	1	Compare match in TPU channel 1
1	0	Compare match in TPU channel 2
	1	Compare match in TPU channel 3

Output Trigger for Pulse Output Group 2

0	0	Compare match in TPU channel 0
	1	Compare match in TPU channel 1
1	0	Compare match in TPU channel 2
	1	Compare match in TPU channel 3

Output Trigger for Pulse Output Group 3

0	0	Compare match in TPU channel 0
	1	Compare match in TPU channel 1
1	0	Compare match in TPU channel 2
	1	Compare match in TPU channel 3

Bit :	7	6	5	4	3	2	1	0
	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV
Initial value :	1	1	1	1	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse Output Group n Normal/Non-Overlap Operation Select

0	Normal operation in pulse output group n (output values updated at compare match A in the selected TPU channel)
1	Non-overlapping operation in pulse output group n (independent 1 and 0 output at compare match A or B in the selected TPU channel)

(n = 3 to 0)

Pulse Output Group n Direct/Inverse Output

0	Inverse output for pulse output group n (low-level output at pin for a 1 in PODRH)
1	Direct output for pulse output group n (high-level output at pin for a 1 in PODRH)

(n = 3 to 0)

NDERH

Bit	7	6	5	4	3	2	1	0
	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse Output Enable/Disable

0	Pulse outputs PO_{15} to PO_8 are disabled
1	Pulse outputs PO_{15} to PO_8 are enabled

NDERL

Bit	7	6	5	4	3	2	1	0
	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse Output Enable/Disable

0	Pulse outputs PO_7 to PO_0 are disabled
1	Pulse outputs PO_7 to PO_0 are enabled

PODRH

Bit :	7	6	5	4	3	2	1	0
	POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Stores output data for use in pulse output

PODRL

Bit :	7	6	5	4	3	2	1	0
	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Stores output data for use in pulse output

Note: * A bit that has been set for pulse output by NDER is read-only.

(1) When pulse output group output triggers are the same

(a) Address: H'FF4C

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores the next data for pulse output groups 3 and 2

(b) Address: H'FF4E

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

(2) When pulse output group output triggers are different

(a) Address: H'FF4C

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Stores the next data for pulse output group 3

(b) Address: H'FF4E

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR11	NDR10	NDR9	NDR8
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Stores the next data for pulse output group 2

(1) When pulse output group output triggers are the same

(a) Address: H'FF4D

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores the next data for pulse output groups 1 and 0

(b) Address: H'FF4F

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

(2) When pulse output group output triggers are different

(a) Address: H'FF4D

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Stores the next data for pulse output group 1

(b) Address: H'FF4F

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR3	NDR2	NDR1	NDR0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Stores the next data for pulse output group 0

PORT1—Port 1 Register **H'FF50** **Port 1**

Bit :	7	6	5	4	3	2	1	0
	P17	P16	P15	P14	P13	P12	P11	P10
Initial value :	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write :	R	R	R	R	R	R	R	R

State of port 1 pins

Note: * Determined by the state of pins $P1_7$ to $P1_0$.

PORT2—Port 2 Register **H'FF51** **Port 2**

Bit :	7	6	5	4	3	2	1	0
	P27	P26	P25	P24	P23	P22	P21	P20
Initial value :	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write :	R	R	R	R	R	R	R	R

State of port 2 pins

Note: * Determined by the state of pins $P2_7$ to $P2_0$.

PORT3—Port 3 Register **H'FF52** **Port 3**

Bit :	7	6	5	4	3	2	1	0
	—	—	P35	P34	P33	P32	P31	P30
Initial value :	Undefined	Undefined	—*	—*	—*	—*	—*	—*
Read/Write :	—	—	R	R	R	R	R	R

State of port 3 pins

Note: * Determined by the state of pins $P3_5$ to $P3_0$.

PORT4—Port 4 Register **H'FF53** **Port 4**

Bit	:	7	6	5	4	3	2	1	0
		P47	P46	P45	P44	P43	P42	P41	P40
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	:	R	R	R	R	R	R	R	R

State of port 4 pins

Note: * Determined by the state of pins $P4_7$ to $P4_0$.

PORT5—Port 5 Register **H'FF54** **Port 5**

Bit	:	7	6	5	4	3	2	1	0
		P57	P56	P55	P54	P53	P52	P51	P50
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	:	R	R	R	R	R	R	R	R

State of port 5 pins

Note: * Determined by the state of pins $P5_7$ to $P5_0$.

PORT6—Port 6 Register **H'FF55** **Port 6**

Bit	:	7	6	5	4	3	2	1	0
		P67	P66	P65	P64	P63	P62	P61	P60
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	:	R	R	R	R	R	R	R	R

State of port 6 pins

Note: * Determined by the state of pins $P6_7$ to $P6_0$.

PORT7—Port 7 Register **H'FF56** **Port 7**

Bit	7	6	5	4	3	2	1	0
	—	—	P75	P74	P73	P72	P71	P70
Initial value	Undefined	Undefined	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

State of port 7 pins

Note: * Determined by the state of pins $P7_5$ to $P7_0$.

PORT8—Port 8 Register **H'FF57** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	P86	P85	P84	P83	P82	P81	P80
Initial value	Undefined	—*	—*	—*	—*	—*	—*	—*
Read/Write	—	R	R	R	R	R	R	R

State of port 8 pins

Note: * Determined by the state of pins $P8_6$ to $P8_0$.

PORT9—Port 9 Register **H'FF58** **Port 9**

Bit	7	6	5	4	3	2	1	0
	P97	P96	P95	P94	P93	P92	—	—
Initial value	—*	—*	—*	—*	—*	—*	Undefined	Undefined
Read/Write	R	R	R	R	R	R	—	—

State of port 9 pins

Note: * Determined by the state of pins $P9_7$ to $P9_2$.

PORTA—Port A Register **H'FF59** **Port A**

Bit	7	6	5	4	3	2	1	0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port A pins

Note: * Determined by the state of pins PA_7 to PA_0.

PORTB—Port B Register **H'FF5A** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port B pins

Note: * Determined by the state of pins PB_7 to PB_0.

PORTC—Port C Register **H'FF5B** **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port C pins

Note: * Determined by the state of pins PC_7 to PC_0.

PORTD—Port D Register **H'FF5C** **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port D pins

Note: * Determined by the state of pins PD_7 to PD_0.

PORTE—Port E Register **H'FF5D** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port E pins

Note: * Determined by the state of pins PE_7 to PE_0.

PORTF—Port F Register **H'FF5E** **Port F**

Bit	7	6	5	4	3	2	1	0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port F pins

Note: * Determined by the state of pins PF_7 to PF_0.

PORTG—Port G Register **H'FF5F** **Port G**

Bit	7	6	5	4	3	2	1	0
	—	—	—	PG4	PG3	PG2	PG1	PG0
Initial value	Undefined	Undefined	Undefined	—*	—*	—*	—*	—*
Read/Write	—	—	—	R	R	R	R	R

State of port G pins

Note: * Determined by the state of pins PG_4 to PG_0.

P1DR—Port 1 Data Register **H'FF60** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 1 pins ($P1_7$ to $P1_0$)

P2DR—Port 2 Data Register **H'FF61** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 2 pins ($P2_7$ to $P2_0$)

P3DR—Port 3 Data Register **H'FF62** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
Initial value	Undefined	Undefined	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 3 pins ($P3_5$ to $P3_0$)

P5DR—Port 5 Data Register **H'FF64** **Port 5**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	P53DR	P52DR	P51DR	P50DR
Initial value	Undefined	Undefined	Undefined	Undefined	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Stores output data for port 5 pins ($P5_3$ to $P5_0$)

P6DR—Port 6 Data Register **H'FF65** **Port 6**

Bit	7	6	5	4	3	2	1	0
	P67DR	P66DR	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 6 pins ($P6_7$ to $P6_0$)

P7DR—Port 7 Data Register **H'FF66** **Port 7**

Bit	7	6	5	4	3	2	1	0
	—	—	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR
Initial value	Undefined	Undefined	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 7 pins ($P7_5$ to $P7_0$)

P8DR—Port 8 Data Register **H'FF67** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	P86DR	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR
Initial value	Undefined	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 8 pins ($P8_6$ to $P8_0$)

P9DR—Port 9 Data Register **H'FF68** **Port 9**

Bit	7	6	5	4	3	2	1	0
	P97DR	P96DR	P95DR	P94DR	P93DR	P92DR	—	—
Initial value	0	0	0	0	0	0	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Stores output data for port 9 pins ($P9_7$ to $P9_2$)

PADR—Port A Data Register **H'FF69** **Port A**

Bit	7	6	5	4	3	2	1	0
	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port A pins (PA_7 to PA_0)

PBDR—Port B Data Register **H'FF6A** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port B pins (PB_7 to PB_0)

PCDR—Port C Data Register **H'FF6B** **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port C pins (PC_7 to PC_0)

PDDR—Port D Data Register **H'FF6C** **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port D pins (PD_7 to PD_0)

PEDR—Port E Data Register **H'FF6D** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port E pins (PE_7 to PE_0)

PFDR—Port F Data Register **H'FF6E** **Port F**

Bit	7	6	5	4	3	2	1	0
	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port F pins (PF_7 to PF_0)

PGDR—Port G Data Register H'FF6F Port G

Bit	7	6	5	4	3	2	1	0
	—	—	—	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR
Initial value	Undefined	Undefined	Undefined	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Stores output data for port G pins (PG_4 to PG_0)

PAPCR—Port A MOS Pull-Up Control Register H'FF70 Port A

Bit	7	6	5	4	3	2	1	0
	PA7PCR	PA6PCR	PA5PCR	PA4PCR	PA3PCR	PA2PCR	PA1PCR	PA0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port A on a bit-by-bit basis

PBPCR—Port B MOS Pull-Up Control Register H'FF71 Port B

Bit	7	6	5	4	3	2	1	0
	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port B on a bit-by-bit basis

PCPCR—Port C MOS Pull-Up Control Register H'FF72 **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port C on a bit-by-bit basis

PDPCR—Port D MOS Pull-Up Control Register H'FF73 **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port D on a bit-by-bit basis

PEPCR—Port E MOS Pull-Up Control Register H'FF74 **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the MOS input pull-up function incorporated into port E on a bit-by-bit basis

P3ODR—Port 3 Open Drain Control Register H'FF76 Port 3

Bit	7	6	5	4	3	2	1	0
	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR
Initial value	Undefined	Undefined	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Controls the PMOS on/off status for each port 3 pin ($P3_5$ to $P3_0$)

PAODR—Port A Open Drain Control Register H'FF77 Port A

Bit	7	6	5	4	3	2	1	0
	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Controls the PMOS on/off status for each port A pin (PA_7 to PA_0)

Bit :	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity
1	Odd parity

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Base Clock Pulse

BCP1	BCP0	Base Clock Pulse
0	0	32 clocks
	1	64 clocks
1	0	372 clocks
	1	256 clocks

Parity Mode

0	Even parity
1	Odd parity

Parity Enable
(Set to 1 when using the smart card interface)

0	Setting prohibited
1	Parity bit addition and checking enabled

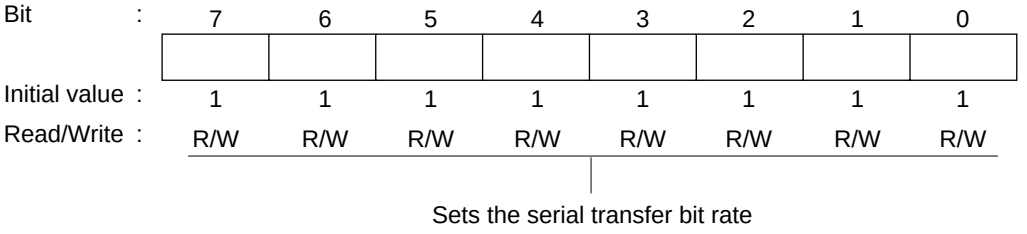
Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generated 12.5 etu (11.5 etu in block transfer mode) after beginning of start bit • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generated 11.0 etu after beginning of start bit • Fixed high/low-level control possible (set in SCR) in addition to clock output on/off control

Note: etu (Elementary Time Unit): Interval for transfer of one bit



Note: For details, see section 11.2.8, Bit Rate Register (BRR), in the Hardware Manual.

Bit	:	7	6	5	4	3	2	1	0
		TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(When bit 7 of SMR is set to 1 in smart card interface mode)

SCMR	SMR	SCR setting		SCK pin function
SMIF	C/$\overline{A}$,GM	CKE1	CKE0	
0	See SCI specification			
1	0	0	0	Operates as port I/O pin
1	0	0	1	Clock output as SCK output pin
1	1	0	0	Fixed-low output as SCK output pin
1	1	0	1	Clock output as SCK output pin
1	1	1	0	Fixed-high output as SCK output pin
1	1	1	1	Clock output as SCK output pin

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit	:	7	6	5	4	3	2	1	0
		TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(When bit 7 of SMR is set to 1 in smart card interface mode)

SCMR	SMR		SCR setting		SCK pin function
SMIF	C/$\overline{A}$,GM		CKE1	CKE0	
0	See SCI specification				
1	0		0	0	Operates as port I/O pin
1	0		0	1	Clock output as SCK output pin
1	1		0	0	Fixed-low output as SCK output pin
1	1		0	1	Clock output as SCK output pin
1	1		1	0	Fixed-high output as SCK output pin
1	1		1	1	Clock output as SCK output pin

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

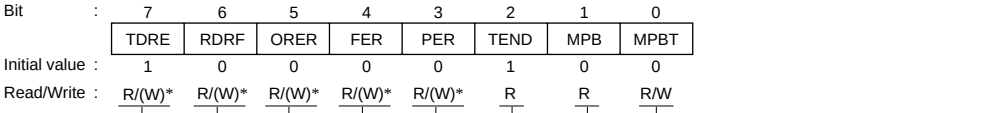
Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled


Bit :
7
6
5
4
3
2
1
0
Initial value :
1
1
1
1
1
1
1
1
Read/Write :
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
Stores data for serial transmission



Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Framing Error

0	[Clearing condition] When 0 is written to FER after reading FER = 1
1	[Setting condition] When the SCI checks the stop bit at the end of the receive data when reception ends, and the stop bit is 0

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0 for flag clearing.

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	Transmission in progress [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	Transmission has ended [Setting conditions] • On reset, or in standby mode or module stop mode • When the TE bit in SCR is 0 and the ERS bit is 0 • When TDRE = 1 and ERS = 0 (normal transmission) 2.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 1 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 1

Note: etu (Elementary Time Unit): Interval for transfer of one bit

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Error Signal Status

0	Data has been received normally, and there is no error signal [Clearing conditions] • On reset, or in standby mode or module stop mode • When 0 is written to ERS after reading ERS = 1
1	Error signal indicating detection of parity error has been sent by receiving device [Setting condition] When the error signal is sampled at the low level

Note: Clearing the TE bit in SCR to 0 does not affect the ERS flag, which retains its prior state.

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0 for flag clearing.

RDR0—Receive Data Register 0 **H'FF7D** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores received serial data

SCMR0—Smart Card Mode Register 0 **H'FF7E** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value	1	1	1	1	0	0	1	0
Read/Write	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

Bit :	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity
1	Odd parity

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Base Clock Pulse

BCP1	BCP0	Base Clock Pulse
0	0	32 clocks
	1	64 clocks
1	0	372 clocks
	1	256 clocks

Parity Mode
(Set to 1 when using the smart card interface)

0	Even parity
1	Odd parity

Parity Enable

0	Setting prohibited
1	Parity bit addition and checking enabled

Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generated 12.5 etu (11.5 etu in block transfer mode) after beginning of start bit • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generated 11.0 etu after beginning of start bit • Fixed high/low-level control possible (set in SCR) in addition to clock output on/off control

Note: etu (Elementary Time Unit): Interval for transfer of one bit

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sets the serial transfer bit rate

Note: For details, see section 11.2.8, Bit Rate Register (BRR), in the Hardware Manual.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable

0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input

Notes: 1. Outputs a clock of the same frequency as the bit rate.
2. Inputs a clock with a frequency 16 times the bit rate.

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit	:	7	6	5	4	3	2	1	0
		TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(When bit 7 of SMR is set to 1 in smart card interface mode)

SCMR	SMR	SCR setting		SCK pin function
SMIF	C/$\overline{A}$,GM	CKE1	CKE0	
0	See SCI specification			
1	0	0	0	Operates as port I/O pin
1	0	0	1	Clock output as SCK output pin
1	1	0	0	Fixed-low output as SCK output pin
1	1	0	1	Clock output as SCK output pin
1	1	1	0	Fixed-high output as SCK output pin
1	1	1	1	Clock output as SCK output pin

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled


Bit :
7
6
5
4
3
2
1
0
Initial value :
1
1
1
1
1
1
1
1
Read/Write :
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
Stores data for serial transmission

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Framing Error

0	[Clearing condition] When 0 is written to FER after reading FER = 1
1	[Setting condition] When the SCI checks the stop bit at the end of the receive data when reception ends, and the stop bit is 0

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0 for flag clearing.

Bit	:	7	6	5	4	3	2	1	0
		TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Initial value	:	1	0	0	0	0	1	0	0
Read/Write	:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	Transmission in progress [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	Transmission has ended [Setting conditions] • On reset, or in standby mode or module stop mode • When the TE bit in SCR is 0 and the ERS bit is 0 • When TDRE = 1 and ERS = 0 (normal transmission) 2.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 1 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 1

Note: etu (Elementary Time Unit): Interval for transfer of one bit

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Error Signal Status

0	Data has been received normally, and there is no error signal [Clearing conditions] • On reset, or in standby mode or module stop mode • When 0 is written to ERS after reading ERS =1
1	Error signal indicating detection of parity error has been sent by receiving device [Setting condition] When the error signal is sampled at the low level

Note: Clearing the TE bit in SCR to 0 does not affect the ERS flag, which retains its prior state.

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0 for flag clearing.

RDR1—Receive Data Register 1 **H'FF85 SCI1, Smart Card Interface 1**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores received serial data

SCMR1—Smart Card Mode Register 1 **H'FF86 SCI1, Smart Card Interface 1**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value	1	1	1	1	0	0	1	0
Read/Write	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

Bit :	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity
1	Odd parity

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Base Clock Pulse

BCP1	BCP0	Base Clock Pulse
0	0	32 clocks
	1	64 clocks
1	0	372 clocks
	1	256 clocks

Parity Mode
(Set to 1 when using the smart card interface)

0	Even parity
1	Odd parity

Parity Enable

0	Setting prohibited
1	Parity bit addition and checking enabled

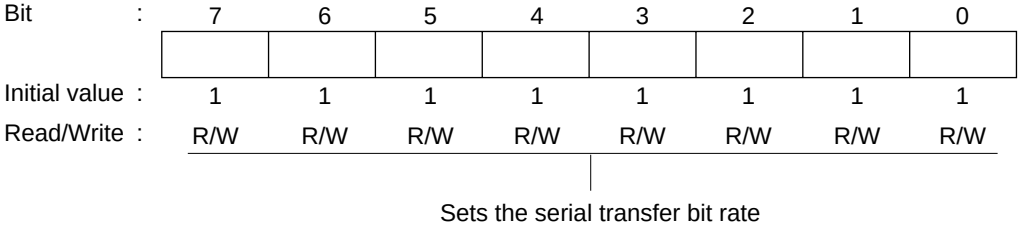
Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generated 12.5 etu (11.5 etu in block transfer mode) after beginning of start bit • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generated 11.0 etu after beginning of start bit • Fixed high/low-level control possible (set in SCR) in addition to clock output on/off control

Note: etu (Elementary Time Unit): Interval for transfer of one bit



Note: For details, see section 11.2.8, Bit Rate Register (BRR), in the Hardware Manual.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable

0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input

Notes: 1. Outputs a clock of the same frequency as the bit rate.
2. Inputs a clock with a frequency 16 times the bit rate.

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(When bit 7 of SMR is set to 1 in smart card interface mode)

SMCR	SMR	SCR setting		SCK pin function
SMIF	C/$\overline{A}$,GM	CKE1	CKE0	
0	See SCI specification			
1	0	0	0	Operates as port I/O pin
1	0	0	1	Clock output as SCK output pin
1	1	0	0	Fixed-low output as SCK output pin
1	1	0	1	Clock output as SCK output pin
1	1	1	0	Fixed-high output as SCK output pin
1	1	1	1	Clock output as SCK output pin

Transmit End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

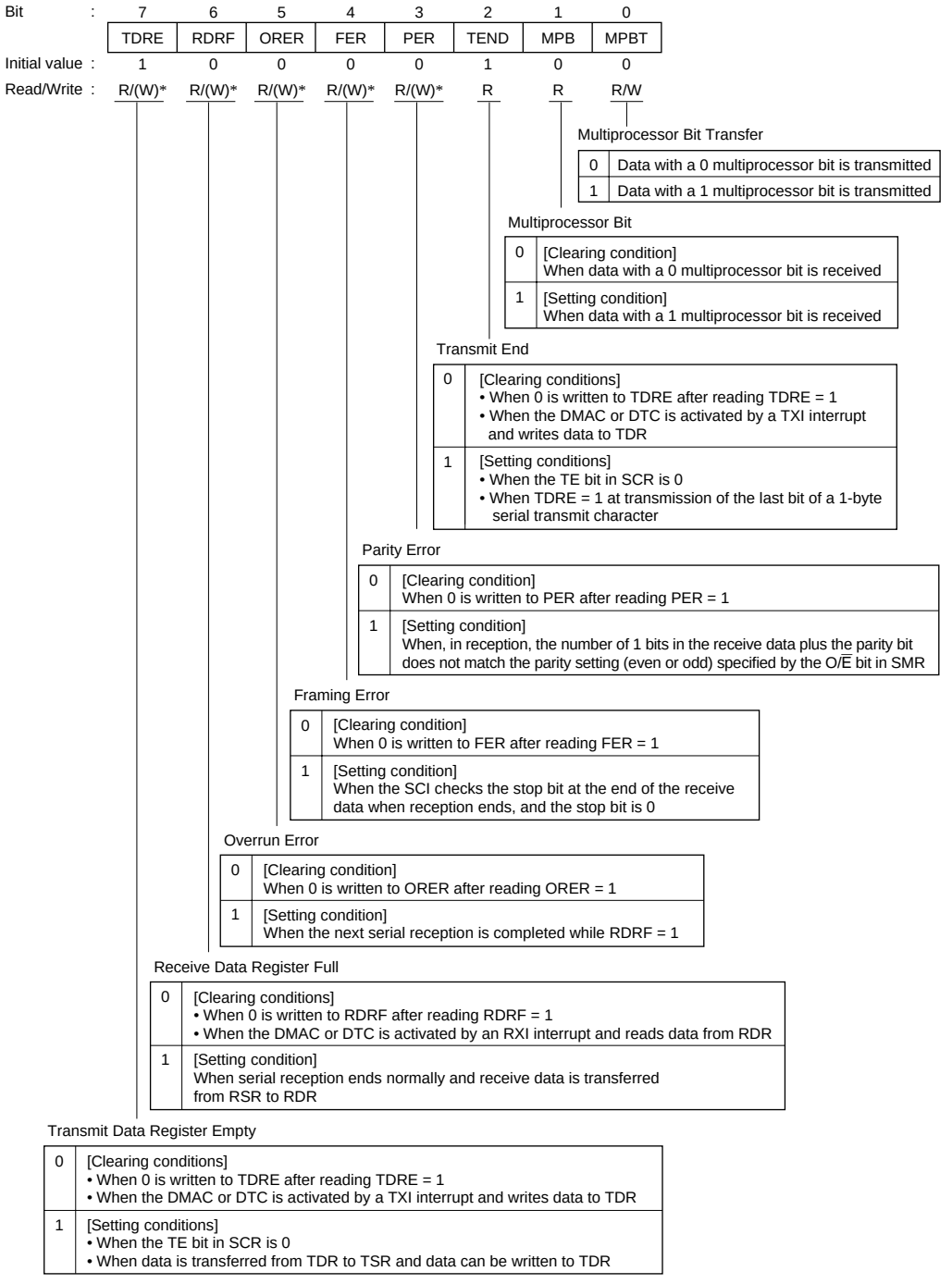
Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled


Bit :
7
6
5
4
3
2
1
0
Initial value :
1
1
1
1
1
1
1
1
Read/Write :
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
Stores data for serial transmission



Note: * Can only be written with 0 for flag clearing.

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	Transmission in progress [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	Transmission has ended [Setting conditions] • On reset, or in standby mode or module stop mode • When the TE bit in SCR is 0 and the ERS bit is 0 • When TDRE = 1 and ERS = 0 (normal transmission) 2.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 1 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 0 • When TDRE = 1 and ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 1

Note: etu (Elementary Time Unit): Interval for transfer of one bit

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Error Signal Status

0	Data has been received normally, and there is no error signal [Clearing conditions] • On reset, or in standby mode or module stop mode • When 0 is written to ERS after reading ERS =1
1	Error signal indicating detection of parity error has been sent by receiving device [Setting condition] When the error signal is sampled at the low level

Note: Clearing the TE bit in SCR to 0 does not affect the ERS flag, which retains its prior state.

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

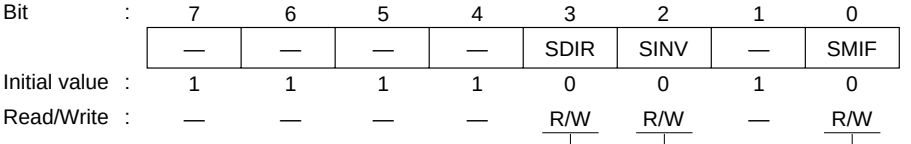
Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0 for flag clearing.

RDR2—Receive Data Register 2 **H'FF8D SCI2, Smart Card Interface 2**

SCMR2—Smart Card Mode Register 2 **H'FF8E SCI2, Smart Card Interface 2**



Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

ADDRAH	**—**	**A/D Data Register AH**	**H'FF90**	**A/D Converter**
ADDRAL	**—**	**A/D Data Register AL**	**H'FF91**	**A/D Converter**
ADDRBH	**—**	**A/D Data Register BH**	**H'FF92**	**A/D Converter**
ADDRBL	**—**	**A/D Data Register BL**	**H'FF93**	**A/D Converter**
ADDRCH	**—**	**A/D Data Register CH**	**H'FF94**	**A/D Converter**
ADDRCL	**—**	**A/D Data Register CL**	**H'FF95**	**A/D Converter**
ADDRDH	**—**	**A/D Data Register DH**	**H'FF96**	**A/D Converter**
ADDRDL	**—**	**A/D Data Register DL**	**H'FF97**	**A/D Converter**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Stores the results of A/D conversion

Analog Input Channel				A/D Data Register
Channel Set 0 (CH3 = 1)		Channel Set 1 (CH3 = 0)		
Group 0	Group 1	Group 0	Group 1	
AN0	AN4	Setting prohibited	AN12	ADDRA
AN1	AN5	Setting prohibited	AN13	ADDRB
AN2	AN6	Setting prohibited	AN14	ADDRC
AN3	AN7	Setting prohibited	AN15	ADDRD

Bit	:	7	6	5	4	3	2	1	0
		ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel Select
Note: CH2, CH1, and CH0 are used in combination with bit 2 (CH3) of ADCR.
See ADCR—A/D Control Register H'FF99 A/D Converter.

Clock Select
Note: CKS is used in combination with bit 3 (CKS1) of ADCR.
See ADCR—A/D Control Register H'FF99 A/D Converter.

Scan Mode

0	Single mode
1	Scan mode

A/D Start

0	A/D conversion stopped
1	• Single mode: A/D conversion is started. Cleared to 0 automatically when conversion ends • Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or transition to standby mode or module stop mode

A/D Interrupt Enable

0	A/D conversion end interrupt request disabled
1	A/D conversion end interrupt request enabled

A/D End Flag

0	[Clearing conditions] • When 0 is written to the ADF flag after reading ADF = 1 • When the DMAC or DTC is activated by an ADI interrupt, and ADDR is read
1	[Setting conditions] • Single mode: When A/D conversion ends • Scan mode: When A/D conversion ends on all specified channels

Note: * Can only be written with 0 for flag clearing.

Bit	7	6	5	4	3	2	1	0
	TRGS1	TRGS0	—	—	CKS1	CH3	—	—
Initial value	0	0	1	1	1	1	1	1
Read/Write	R/W	R/W	—	—	R/W	R/W	—	—

Channel Select

Selects the analog input channels. Ensure that conversion is halted (ADST = 0) before making a channel selection.

Channel Selection				Description	
CH3	CH2*	CH1*	CH0*	Single Mode	Scan Mode
1	0	0	0	AN0 (Initial value)	AN_0
			1	AN_1	AN_0, AN_1
		1	0	AN_2	AN_0 to AN_2
			1	AN_3	AN_0 to AN_3
	1	0	0	AN_4	AN_4
			1	AN_5	AN_4, AN_5
		1	0	AN_6	AN_4 to AN_6
			1	AN_7	AN_4 to AN_7
0	0	0	0	Setting prohibited	Setting prohibited
			1	Setting prohibited	Setting prohibited
		1	0	Setting prohibited	Setting prohibited
			1	Setting prohibited	Setting prohibited
	1	0	0	AN_{12}	AN_{12}
			1	AN_{13}	AN_{12}, AN_{13}
		1	0	AN_{14}	AN_{12} to AN_{14}
			1	AN_{15}	AN_{12} to AN_{15}

Note: * CH2, CH1, and CH0 are bits in ADCSR.

Clock Select

Bit 3	ADCSR Bit 3	Description
CKS1	CKS	
0	0	Conversion time = 530 states (max.)
	1	Conversion time = 68 states (max.)
1	0	Conversion time = 266 states (max.) (Initial value)
	1	Conversion time = 134 states (max.)

Timer Trigger Select

TRGS1	TRGS1	Description
0	0	A/D conversion start by external trigger is disabled
	1	A/D conversion start by external trigger (TPU) is enabled
1	0	A/D conversion start by external trigger (8-bit timer) is enabled
	1	A/D conversion start by external trigger pin ($\overline{ADTRG}$) is enabled

DADR0—D/A Data Register 0 **H'FFA4** **D/A Converter**
DADR1—D/A Data Register 1 **H'FFA5** **D/A Converter**

Bit	:	7	6	5	4	3	2	1	0
		DAOE1	DAOE0	DAE	—	—	—	—	—
Initial value	:	0	0	0	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	—	—	—	—	—

D/A Output Enable 0

0	Analog output DA_0 is disabled
1	Channel 0 D/A conversion is enabled Analog output DA_0 is enabled

D/A Output Enable 1

0	Analog output DA_1 is disabled
1	Channel 1 D/A conversion is enabled Analog output DA_1 is enabled

D/A Conversion Control

DAOE1	DAOE0	DAE	Description
0	0	*	Channel 0 and 1 D/A conversion disabled
	1	0	Channel 0 D/A conversion enabled
			Channel 1 D/A conversion disabled
		1	Channel 0 and 1 D/A conversion enabled
1	0	0	Channel 0 D/A conversion disabled
			Channel 1 D/A conversion enabled
		1	Channel 0 and 1 D/A conversion enabled
	1	*	Channel 0 and 1 D/A conversion enabled

* : Don't care


Bit : 7 6 5 4 3 2 1 0
Initial value : 0 0 0 0 0 0 0 0
Read/Write : R/W R/W R/W R/W R/W R/W R/W R/W
Stores data for D/A conversion

Bit :	7	6	5	4	3	2	1	0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Initial value :	0	0	0	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	—	—	—	—	—

D/A Output Enable 0

0	Analog output DA_2 is disabled
1	Channel 2 D/A conversion is enabled Analog output DA_2 is enabled

D/A Output Enable 1

0	Analog output DA_3 is disabled
1	Channel 3 D/A conversion is enabled Analog output DA_3 is enabled

D/A Conversion Control

DAOE1	DAOE0	DAE	Description
0	0	*	Channel 2 and 3 D/A conversion disabled
	1	0	Channel 2 D/A conversion enabled
			Channel 3 D/A conversion disabled
		1	Channel 2 and 3 D/A conversion enabled
1	0	0	Channel 2 D/A conversion disabled
			Channel 3 D/A conversion enabled
		1	Channel 2 and 3 D/A conversion enabled
	1	*	Channel 2 and 3 D/A conversion enabled

* : Don't care

Bit	7	6	5	4	3	2	1	0
	WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R

AS Output Disable

0	PF_6 is designated as $\overline{AS}$ output pin
1	PF_6 is designated as I/O port, and does not function as $\overline{AS}$ output pin

Note: This bit is valid in modes 4 to 6.

CS25 Enable

0	$\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$, and $\overline{CS}_5$ output disabled (can be used as I/O ports)
1	$\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$, and $\overline{CS}_5$ output enabled

Note: Clear the DDR bits to 0 before changing the CS25E setting.

CS167 Enable

0	$\overline{CS}_1$, $\overline{CS}_6$, and $\overline{CS}_7$ output disabled (can be used as I/O ports)
1	$\overline{CS}_1$, $\overline{CS}_6$, and $\overline{CS}_7$ output enabled

Note: Clear the DDR bits to 0 before changing the CS167E setting.

BREQO Pin Select

0	$\overline{BREQO}$ output is PF_2 pin
1	$\overline{BREQO}$ output is $P5_3$ pin

Note: Set BREQOPS before setting the BREQOE bit in BCRL to 1.

WAIT Pin Select

0	$\overline{WAIT}$ input is $P8_6$ pin
1	$\overline{WAIT}$ input is $P5_3$ pin

Note: Set WAITPS before setting the WAITE bit in BCRL to 1.

Bit :	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	0	Clock input disabled
		1	Internal clock: counted at falling edge of ø/8
	1	0	Internal clock: counted at falling edge of ø/64
		1	Internal clock: counted at falling edge of ø/8192
1	0	0	For channel 0: Count at TCNT1 overflow signal* For channel 1: Count at TCNT0 compare match A*
		1	External clock: counted at rising edge
	1	0	External clock: counted at falling edge
		1	External clock: counted at both rising and falling edges

Note: * If the count input of channel 0 is the TCNT1 overflow signal and that of channel 1 is the TCNT0 compare match signal, no incrementing clock is generated. Do not use this setting.

Counter Clear

0	0	Clear is disabled
	1	Clear by compare match A
1	0	Clear by compare match B
	1	Clear by rising edge of external reset input

Timer Overflow Interrupt Enable

0	OVF interrupt requests (OVI) are disabled
1	OVF interrupt requests (OVI) are enabled

Compare Match Interrupt Enable A

0	CMFA interrupt requests (CMIA) are disabled
1	CMFA interrupt requests (CMIA) are enabled

Compare Match Interrupt Enable B

0	CMFB interrupt requests (CMIB) are disabled
1	CMFB interrupt requests (CMIB) are enabled

TCSR0

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W	R/W

TCSR1

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	—	R/W	R/W	R/W	R/W

Output Select

0	0	No change when compare match A occurs
	1	0 is output when compare match A occurs
1	0	1 is output when compare match A occurs
	1	Output is inverted when compare match A occurs (toggle output)

Output Select

0	0	No change when compare match B occurs
	1	0 is output when compare match B occurs
1	0	1 is output when compare match B occurs
	1	Output is inverted when compare match B occurs (toggle output)

A/D Trigger Enable (TCSR0 only)

0	A/D converter start requests by compare match A are disabled
1	A/D converter start requests by compare match A are enabled

Timer Overflow Flag

0	[Clearing condition] When 0 is written to OVF after reading OVF = 1
1	[Setting condition] When TCNT overflows (changes from H'FF to H'00)

Compare Match Flag A

0	[Clearing conditions] • When 0 is written to CMFA after reading CMFA = 1 • When the DTC is activated by a CMIA interrupt, while the DISEL bit of MRB in DTC is 0
1	[Setting condition] When TCNT matches TCORA

Compare Match Flag B

0	[Clearing conditions] • When 0 is written to CMFB after reading CMFB = 1 • When the DTC is activated by a CMIB interrupt, while the DISEL bit of MRB in DTC is 0
1	[Setting condition] When TCNT matches TCORB

Note: * Only 0 can be written to bits 7 to 5, to clear these flags.

TCORA0—Time Constant Register A0 **H'FFB4** **8-Bit Timer Channel 0**
TCORA1—Time Constant Register A1 **H'FFB5** **8-Bit Timer Channel 1**

	TCORA0								TCORA1							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCORB0—Time Constant Register B0 **H'FFB6** **8-Bit Timer Channel 0**
TCORB1—Time Constant Register B1 **H'FFB7** **8-Bit Timer Channel 1**

	TCORB0								TCORB1							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNT0—Timer Counter 0 **H'FFB8** **8-Bit Timer Channel 0**
TCNT1—Timer Counter 1 **H'FFB9** **8-Bit Timer Channel 1**

	TCNT0								TCNT1							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/(W)*1	R/W	R/W	—	—	R/W	R/W	R/W

Clock Select

CKS2	CKS1	CKS0	Clock	Overflow period* (when ø = 20 MHz)
0	0	0	ø/2 (Initial value)	25.6µs
		1	ø/64	819.2µs
	1	0	ø/128	1.6ms
		1	ø/512	6.6ms
1	0	0	ø/2048	26.2ms
		1	ø/8192	104.9ms
	1	0	ø/32768	419.4ms
		1	ø/131072	1.68s

Note: * The overflow period is the time from when TCNT starts counting up from H'00 until overflow occurs.

Timer Enable

0	TCNT is initialized to H'00 and halted
1	TCNT counts

Timer Mode Select

0	Interval timer mode: Sends the CPU an interval timer interrupt request (WOVI) when TCNT overflows
1	Watchdog timer mode: Generates the $\overline{WDTOVF}$ signal when TCNT overflows

Overflow Flag

0	[Clearing condition] When 0 is written to OVF after reading OVF = 1
1	[Setting condition] When TCNT overflows from H'FF to H'00 in interval timer mode

The method for writing to TCSR is different from that for general registers to prevent accidental overwriting. For details, see section 10.2.4, Notes on Register Access, in the Hardware Manual.

Note: * Can only be written with 0 for flag clearing.

TCNT—Timer Counter **H'FFBC (W) H'FFBD (R)** **WDT**

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RSTCSR—Reset Control/Status Register **H'FFBE (W) H'FFBF (R)** **WDT**

Bit	:	7	6	5	4	3	2	1	0
		WOVF	RSTE	—	—	—	—	—	—
Initial value	:	0	0	0	1	1	1	1	1
Read/Write	:	R/(W)*	R/W	R/W	—	—	—	—	—

Reserved
This bit cannot be modified

Reset Enable

0	Reset signal is not generated if TCNT overflows*
1	Reset signal is generated if TCNT overflows

Note: * The modules in the H8S/2338 Series are not reset, but TCNT and TCSR in WDT are reset.

Watchdog Timer Overflow Flag

0	[Clearing condition] When 0 is written to WOVF after reading WOVF = 1
1	[Setting condition] When TCNT overflows (changes from H'FF to H'00) during watchdog timer operation

Note: * Can only be written with 0 for flag clearing.

The method for writing to RSTCSR is different from that for general registers to prevent accidental overwriting. For details, see section 10.2.4, Notes on Register Access, in the Hardware Manual.

Bit	7	6	5	4	3	2	1	0
	—	—	CST5	CST4	CST3	CST2	CST1	CST0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Counter Start

0	TCNTn count operation is stopped
1	TCNTn performs count operation

(n = 5 to 0)

Note: If 0 is written to the CST bit during operation with the TIOC pin designated for output, the counter stops but the TIOC pin output compare output level is retained. If TIOR is written to when the CST bit is cleared to 0, the pin output level will be changed to the set initial output value.

Bit	7	6	5	4	3	2	1	0
	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Timer Synchronization

0	TCNTn operates independently (TCNT presetting/ clearing is unrelated to other channels)
1	TCNTn performs synchronous operation TCNT synchronous presetting/synchronous clearing is possible

(n = 5 to 0)

Notes: 1. To set synchronous operation, the SYNC bits for at least two channels must be set to 1.
2. To set synchronous clearing, in addition to the SYNC bit , the TCNT clearing source must also be set by means of bits CCLR2 to CCLR0 in TCR.

Bit	7	6	5	4	3	2	1	0
	FWE	SWE	ESU	PSU	EV	PV	E	P
Initial value	—*	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Program

0	Program mode cleared
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1

Erase

0	Erase mode cleared
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1

Program-Verify

0	Program-verify mode cleared
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE = 1

Erase-Verify

0	Erase-verify mode cleared
1	Transition to erase-verify mode [Setting condition] When FWE = 1 and SWE = 1

Program Setup

0	Program setup cleared
1	Program setup [Setting condition] When FWE = 1 and SWE = 1

Software Write Enable

0	Writes disabled
1	Writes enabled [Setting condition] When FWE = 1

Erase Setup

0	Erase setup cleared
1	Erase setup [Setting condition] When FWE = 1 and SWE = 1

Flash Write Enable

0	When a low level is input to the FWE pin (hardware-protected state)
1	When a high level is input to the FWE pin

Note: * Determined by the state of the FWE pin (H8S/2338 F-ZTAT version).
The FWE pin is fixed to 1 in the H8S/2339 F-ZTAT version.

Bit :	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	—	—
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R	—	—	—	—	—	—	—

Flash Memory Error

0	Flash memory is operating normally Flash memory program/erase protection (error protection) is disabled [Clearing condition] Reset or hardware standby mode
1	An error has occurred during flash memory programming/erasing Flash memory program/erase protection (error protection) is enabled [Setting condition] See section 17.8.3, Error Protection, in the Hardware Manual.

Bit :	7	6	5	4	3	2	1	0
EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit :	7	6	5	4	3	2	1	0
EBR2	—	—	EB13*	EB12*	EB11	EB10	EB9	EB8
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	—	—	—	—	R/W	R/W	R/W	R/W

Note: * Valid only in H8S/2339 F-ZTAT version.

Bit :	7	6	5	4	3	2	1	0
	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKB pin input
	1	0	External clock: counts on TCLKC pin input
		1	External clock: counts on TCLKD pin input

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Counter Clear

0	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRA compare match/input capture
	1	0	TCNT cleared by TGRB compare match/input capture
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1
1	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRC compare match/input capture*2
	1	0	TCNT cleared by TGRD compare match/input capture*2
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1

Notes: 1. Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.
2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

TGRA Buffer Operation

0	TGRA operates normally
1	TGRA and TGRC used together for buffer operation

TGRB Buffer Operation

0	TGRB operates normally
1	TGRB and TGRD used together for buffer operation

Bit :	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR0A I/O Control

0	0	0	0	TGR0A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0A is input capture register	Capture input source is $TIOCA_0$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down

* : Don't care

TGR0B I/O Control

0	0	0	0	TGR0B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0B is input capture register	Capture input source is $TIOCB_0$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down*[1]

* : Don't care

Note: 1. When bits TPSC2 to TPSC0 in TCR1 are set to B'000, and ø/1 is used as the TCNT1 count clock, this setting is invalid and input capture does not occur.

Bit	:	7	6	5	4	3	2	1	0
	:	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR0C I/O Control

0	0	0	0	TGR0C is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0C is input capture register	Capture input source is $TIOCC_0$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down

* : Don't care

Note: When the BFA bit in TMDR0 is set to 1 and TGR0C is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

TGR0D I/O Control

0	0	0	0	TGR0D is output compare register *2	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0D is input capture register *2	Capture input source is $TIOCD_0$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down*1

* : Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR1 are set to B'000, and ø/1 is used as the TCNT1 count clock, this setting is invalid and input capture does not occur.
2. When the BFB bit in TMDR0 is set to 1 and TGR0D is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

Note: When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

Bit	7	6	5	4	3	2	1	0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

TGR Interrupt Enable C

0	Interrupt request (TGIC) by TGFC bit disabled
1	Interrupt request (TGIC) by TGFC bit enabled

TGR Interrupt Enable D

0	Interrupt request (TGID) by TGFD bit disabled
1	Interrupt request (TGID) by TGFD bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Input Capture/Output Compare Flag C

0	[Clearing conditions] • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

Input Capture/Output Compare Flag D

0	[Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Note: * Can only be written with 0 for flag clearing.

TCNT0—Timer Counter 0 **H'FFD6** **TPU0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up-counter

TGR0A—Timer General Register 0A **H'FFD8** **TPU0**
TGR0B—Timer General Register 0B **H'FFDA** **TPU0**
TGR0C—Timer General Register 0C **H'FFDC** **TPU0**
TGR0D—Timer General Register 0D **H'FFDE** **TPU0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKB pin input
	1	0	Internal clock: counts on ø/256
		1	Counts on TCNT2 overflow/underflow

Note: This setting is ignored when channel 1 is in phase counting mode.

Clock Edge*

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 1 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	:	7	6	5	4	3	2	1	0
		IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR1A I/O Control

0	0	0	0	TGR1A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR1A is input capture register	Capture input source is $TIOCA_1$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR0A compare match/ input capture	Input capture at generation of channel 0/TGR0A compare match/ input capture

* : Don't care

TGR1B I/O Control

0	0	0	0	TGR1B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR1B is input capture register	Capture input source is $TIOCB_1$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR0C compare match/ input capture	Input capture at generation of TGR0C compare match/input capture

* : Don't care

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

TCNT1—Timer Counter 1 **H'FFE6** **TPU1**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR1A—Timer General Register 1A **H'FFE8** **TPU1**
TGR1B—Timer General Register 1B **H'FFEA** **TPU1**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	:	7	6	5	4	3	2	1	0
		—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: counts on ø/1
		1	Internal clock: counts on ø/4
	1	0	Internal clock: counts on ø/16
		1	Internal clock: counts on ø/64
1	0	0	External clock: counts on TCLKA pin input
		1	External clock: counts on TCLKB pin input
	1	0	External clock: counts on TCLKC pin input
		1	Internal clock: counts on ø/1024

Note: This setting is ignored when channel 2 is in phase counting mode.

Clock Edge*

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is ignored when channel 2 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation setting is performed by setting the SYNC bit in TSYR to 1.

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit :	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR2A I/O Control

0	0	0	0	TGR2A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR2A is input capture register	Capture input source is $TIOCA_2$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

TGR2B I/O Control

0	0	0	0	TGR2B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR2B is input capture register	Capture input source is $TIOCB_2$ pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

* : Don't care

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR2A—Timer General Register 2A **H'FFF8** **TPU2**
TGR2B—Timer General Register 2B **H'FFFA** **TPU2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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