Hitachi Single-Chip Microcomputer

H8S/2138 Series
H8S/2134 Series

Hardware Manual
Supplementary Edition

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Section 24   Electrical Characteristics

24.1   Absolute Maximum Ratings

Table 24.1 lists the absolute maximum ratings.

Table 24.1   Absolute Maximum Ratings   **– Preliminary –**

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage (except ports 6 and 7)	V_{in}	−0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port 6)	V_{in}	−0.3 to V_{CC} +0.3	V
Input voltage (CIN input selected for port 6)	V_{in}	Lower voltage of −0.3 to V_{CC} +0.3 and AV_{CC} +0.3	V
Input voltage (port 7)	V_{in}	−0.3 to AV_{CC} + 0.3	V
Analog power supply voltage	AV_{CC}	−0.3 to +7.0	V
Analog input voltage	V_{AN}	−0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: −20 to +75*	°C
		Wide-range specifications: −40 to +85*	°C
Storage temperature	T_{stg}	−55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

      * A range of 0 to +75°C must be observed for flash memory programming/erasing in the F-ZTAT version.

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24.2   DC Characteristics

Table 24.2 lists the DC characteristics. Table 24.3 lists the permissible output currents.

Table 24.2   DC Characteristics — Preliminary —

Conditions: $V_{CC} = 5.0$ V $\pm$ 10%, AV_{CC}[*1] $= 5.0$ V $\pm$ 10%, $V_{SS} = AV_{SS}$[*1] $= 0$ V, $T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60[*2, *6], IRQ2 to IRQ0[*3], IRQ5 to IRQ3	(1)	V_T^-	1.0	—	—	V	
			V_T^+	—	—	$V_{CC} \times 0.7$	V	
			$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	RES, STBY, NMI, MD1, MD0	(2)	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} +0.3$	V	
	EXTAL			$V_{CC} \times 0.7$	—	$V_{CC} +0.3$	V	
	Port 7			2.0	—	$AV_{CC} +0.3$	V	
	Input pins except (1) and (2) above[*6]			2.0	—	$V_{CC} +0.3$	V	
Input low voltage	RES, STBY, MD1, MD0	(3)	V_{IL}	−0.3	—	0.5	V	
	NMI, EXTAL, input pins except (1) and (3) above			−0.3	—	0.8	V	
Output high voltage	All output pins (except P97, and P52)[*5]		V_{OH}	$V_{CC} -0.5$	—	—	V	$I_{OH} = -200$ μA
				3.5	—	—	V	$I_{OH} = -1$ mA
	P97, P52[*4]			2.5	—	—	V	$I_{OH} = -1$ mA
Output low voltage	All output pins[*5]		V_{OL}	—	—	0.4	V	$I_{OL} = 1.6$ mA
	Ports 1 to 3			—	—	1.0	V	$I_{OL} = 10$ mA

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Table 24.2   DC Characteristics (cont)   **– Preliminary –**

Conditions: $V_{CC} = 5.0\ V \pm 10\%$, $AV_{CC}*^1 = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS}*^1 = 0\ V$, $T_a = -20$ to $+75°C$
(regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{\text{RES}}$		$|I_{in}|$	—	—	10.0	µA	$V_{in} = 0.5$ to $V_{CC} - 0.5\ V$
	$\overline{\text{STBY}}$, NMI, MD1, MD0			—	—	1.0	µA	
	Port 7			—	—	1.0	µA	$V_{in} = 0.5$ to $AV_{CC} - 0.5\ V$
Three-state leakage current (off state)	Ports 1 to 6 Ports 8, 9		$|I_{TSI}|$	—	—	1.0	µA	$V_{in} = 0.5$ to $V_{CC} - 0.5\ V$
Input pull-up MOS current	Ports 1 to 3		$-I_P$	50	—	300	µA	$V_{in} = 0\ V$
	Port 6			60	—	500	µA	
Input capacitance	$\overline{\text{RES}}$	(4)	C_{in}	—	—	80	pF	$V_{in} = 0\ V$ $f = 1$ MHz
	NMI			—	—	50	pF	$T_a = 25°C$
	P52, P97, P42, P86			—	—	20	pF	
	Input pins except (4) above			—	—	15	pF	
Current dissipation*[7]	Normal operation		I_{CC}	—	75	100	mA	$f = 20$ MHz, H8S/2134 Series
					85	120	mA	$f = 20$ MHz, H8S/2138 Series
	Sleep mode			—	60	85	mA	$f = 20$ MHz, H8S/2134 Series
					70	100	mA	$f = 20$ MHz, H8S/2138 Series
	Standby mode*[8]			—	0.01	5.0	µA	$T_a \le 50°C$
				—	—	20.0	µA	$50°C < T_a$
Analog power supply current	During A/D, D/A conversion		AI_{CC}	—	3.2	7.0	mA	
	Idle			—	0.01	5.0	µA	$AV_{CC} =$ 2.0 V to 5.5 V

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Table 24.2 DC Characteristics (cont) **– Preliminary –**

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC}*^1 = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS}*^1 = 0 \text{ V}$, $T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply voltage*[1]	AV_{CC}	4.5	—	5.5	V	Operating
		2.0	—	5.5	V	Idle/not used
RAM standby voltage	V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AVCC, and AVSS pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a value in the range 2.0 V to 5.5 V to AVCC by connection to the power supply (V_{CC}), or some other method.

2. P67 to P60 include supporting module inputs multiplexed on those pins.

3. $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

4. P52/SCK0/SCL0 and P97/SDA0 are NMOS push-pull outputs.

An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).

P52/SCK0 and P97 (ICE = 0) high levels are driven by NMOS.

5. When ICE = 0. Low-level output when the bus drive function is selected is determined separately.

6. The upper limit of the port 6 applied voltage is $V_{CC} + 0.3$ V when CIN input is not selected, and the lower of $V_{CC} + 0.3$ V and $AV_{CC} + 0.3$ V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

7. Current dissipation values are for V_{IH} min = $V_{CC} - 0.5$ V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

8. The values are for $V_{RAM} \leq V_{CC} < 4.5V$, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.

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Table 24.2   DC Characteristics (cont)   **– Preliminary –**

Conditions: V_{CC} = 4.0 V to 5.5 V[7], AV_{CC}[1] = 4.0 V to 5.5 V, V_{SS} = AV_{SS}[1] = 0 V, T_a = –20 to +75°C[7] (regular specifications), T_a = –40 to +85°C[7] (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60[2, 6], $\overline{IRQ2}$ to $\overline{IRQ0}$[3], $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	1.0	—	—	V	V_{CC}= 4.5 V to 5.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$	V	
			$V_T^+ - V_T^-$	0.4	—	—	V	
			V_T^-	0.8	—	—	V	V_{CC} < 4.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$	V	
			$V_T^+ - V_T^-$	0.3	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	V_{CC} – 0.7	—	V_{CC} +0.3	V	
	EXTAL			$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port 7			2.0	—	AV_{CC} +0.3	V	
	Input pins except (1) and (2) above[6]			2.0	—	V_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD1, MD0	(3)	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, input pins except (1) and (3) above			–0.3	—	0.8	V	
Output high voltage	All output pins (except P97, and P52)[5]		V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
				3.5	—	—	V	I_{OH} = –1 mA, V_{CC}= 4.5 V to 5.5 V
				3.0	—	—	V	I_{OH} = –1 mA, V_{CC} < 4.5 V
	P97, P52[4]			2.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins[5]		V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 to 3			—	—	1.0	V	I_{OL} = 10 mA

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Table 24.2 DC Characteristics (cont)   **– Preliminary –**

Conditions: V_{CC} = 4.0 V to 5.5 V*[7], AV_{CC}*[1] = 4.0 V to 5.5 V, V_{SS} = AV_{SS}*[1] = 0 V, T_a = –20 to +75°C*[7] (regular specifications), T_a = –40 to +85°C*[7] (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{RES}$		$|I_{in}|$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD1, MD0			—	—	1.0	µA	
	Port 7			—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1 to 6 Ports 8, 9		$|I_{TSI}|$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up current	Ports 1 to 3		$-I_P$	50	—	300	µA	V_{in} = 0 V, V_{CC} = 4.5 V to 5.5 V
	Port 6			60	—	500	µA	
	Ports 1 to 3			30	—	200	µA	V_{in} = 0 V, V_{CC} < 4.5 V
	Port 6			40	—	400	µA	
Input capacitance	$\overline{RES}$	(4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI			—	—	50	pF	
	P52, P97, P42, P86			—	—	20	pF	
	Input pins except (4) above			—	—	15	pF	
Current dissipation*[8]	Normal operation		I_{CC}	—	65	85	mA	f = 16 MHz, H8S/2134 Series
				—	70	100	mA	f = 16 MHz, H8S/2138 Series
	Sleep mode			—	50	70	mA	f = 16 MHz, H8S/2134 Series
				—	60	85	mA	f = 16 MHz, H8S/2138 Series
	Standby mode*[9]			—	0.01	5.0	µA	T_a ≤ 50°C
				—	—	20.0	µA	50°C < T_a

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Table 24.2 DC Characteristics (cont) — Preliminary –

Conditions: V_{CC} = 4.0 V to 5.5 V[7], AV_{CC}[1] = 4.0 V to 5.5 V, V_{SS} = AV_{SS}[1] = 0 V, T_a = –20 to +75°C[7] (regular specifications), T_a = –40 to +85°C[7] (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D, D/A conversion	AI_{CC}	—	3.2	7.0	mA	
	Idle		—	0.01	5.0	μA	AV_{CC} = 2.0 V to 5.5 V
Analog power supply voltage[1]		AV_{CC}	4.0	—	5.5	V	Operating
			2.0	—	5.5	V	Idle/not used
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AVCC, and AVSS pins open even if the A/D converter and D/A converter are not used.

   Even if the A/D converter and D/A converter are not used, apply a value in the range 2.0 V to 5.5 V to AVCC by connection to the power supply (V_{CC}), or some other method.

2. P67 to P60 include supporting module inputs multiplexed on those pins.

3. $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

4. P52/SCK0/SCL0 and P97/SDA0 are NMOS push-pull outputs.

   An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).

   P52/SCK0 and P97 (ICE = 0) high levels are driven by NMOS.

5. When ICE = 0. Low-level output when the bus drive function is selected is determined separately.

6. The upper limit of the port 6 applied voltage is V_{CC} + 0.3 V when CIN input is not selected, and the lower of V_{CC} + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

7. Ranges of V_{CC} = 4.5 to 5.5 V and T_a = 0 to +75°C must be observed for flash memory programming/erasing.

8. Current dissipation values are for V_{IH} min = V_{CC} – 0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

9. The values are for $V_{RAM} \leq V_{CC}$ < 4.5 V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.

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Conditions[7]: V_{CC} = 2.7 V to 5.5 V, AV_{CC}[1] = 2.7 V to 5.5 V, V_{SS} = AV_{SS}[1] = 0 V, T_a = –20 to +75°C (regular specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60[2, 6], $\overline{IRQ2}$ to $\overline{IRQ0}$[3], $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	$V_{CC} \times 0.2$	—	—	V	
			V_T^+	—	—	$V_{CC} \times 0.7$	V	
			$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} +0.3	V	
	EXTAL			$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port 7			$V_{CC} \times 0.7$	—	AV_{CC} +0.3	V	
	Input pins except (1) and (2) above[6]			$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, FWE, MD1, MD0	(3)	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, input pins except (1) and (3) above			–0.3	—	$V_{CC} \times 0.2$	V	V_{CC} < 4.0 V
						0.8	V	V_{CC} = 4.0 V to 5.5 V
Output high voltage	All output pins (except P97, and P52)[5]		V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
				V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA (V_{CC} < 4.0 V)
	P97, P52[4]			1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins[5]		V_{OL}	—	—	0.4	V	I_{OL} = 0.8 mA
	Ports 1 to 3			—	—	1.0	V	I_{OL} = 5 mA (V_{CC} < 4.0 V), I_{OL} = 10 mA (4.0 V ≤ V_{CC} ≤ 5.5 V)

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Table 24.2 DC Characteristics (cont) — Preliminary —

Conditions[7]: $V_{CC} = 2.7$ V to 5.5 V, AV_{CC}[1] $= 2.7$ V to 5.5 V, $V_{SS} = AV_{SS}$[1] $= 0$ V,
$T_a = -20$ to $+75°C$ (regular specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{\text{RES}}$		$|I_{in}|$	—	—	10.0	µA	$V_{in} = 0.5$ to $V_{CC} - 0.5$ V
	$\overline{\text{STBY}}$, NMI, MD1, MD0			—	—	1.0	µA	
	Port 7			—	—	1.0	µA	$V_{in} = 0.5$ to $AV_{CC} - 0.5$ V
Three-state leakage current (off state)	Ports 1 to 6 Ports 8, 9		$|I_{TSI}|$	—	—	1.0	µA	$V_{in} = 0.5$ to $V_{CC} - 0.5$ V
Input pull-up MOS current	Ports 1 to 3		$-I_P$	10	—	150	µA	$V_{in} = 0$ V, $V_{CC} = 2.7$ V to 3.6 V
	Port 6			30	—	250	µA	
Input capacitance	$\overline{\text{RES}}$	(4)	C_{in}	—	—	80	pF	$V_{in} = 0$ V, $f = 1$ MHz, $T_a = 25°C$
	NMI			—	—	50	pF	
	P52, P97, P42, P86			—	—	20	pF	
	Input pins except (4) above			—	—	15	pF	
Current dissipation[8]	Normal operation		I_{CC}	—	45	60	mA	$f = 10$ MHz, H8S/2134 Series
				—	50	70	mA	$f = 10$ MHz, H8S/2138 Series
	Sleep mode			—	35	50	mA	$f = 10$ MHz, H8S/2134 Series
				—	40	60	mA	$f = 10$ MHz, H8S/2138 Series
	Standby mode[9]			—	0.01	5.0	µA	$T_a \leq 50°C$
				—	—	20.0	µA	$50°C < T_a$
Analog power supply current	During A/D, D/A conversion		AI_{CC}	—	3.2	7.0	mA	
	Idle			—	0.01	5.0	µA	$AV_{CC} = 2.0$ V to 5.5 V

Table 24.2 DC Characteristics (cont) – Preliminary –

Conditions[7]: V_{CC} = 2.7 V to 5.5 V, AV_{CC}[1] = 2.7 V to 5.5 V, V_{SS} = AV_{SS}[1] = 0 V,
T_a = –20 to +75°C (regular specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply voltage[1]	AV_{CC}	2.7	—	5.5	V	Operating
		2.0	—	5.5	V	Idle/not used
RAM standby voltage	V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AVCC, and AVSS pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a value in the range 2.0 V to 5.5 V to AVCC by connection to the power supply (V_{CC}), or some other method.

2. P67 to P60 include supporting module inputs multiplexed on those pins.

3. $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

4. P52/SCK0/SCL0 and P97/SDA0 are NMOS push-pull outputs.

An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).

P52/SCK0 and P97 (ICE = 0) high levels are driven by NMOS.

5. When ICE = 0. Low-level output when the bus drive function is selected is determined separately.

6. The upper limit of the port 6 applied voltage is V_{CC} + 0.3 V when CIN input is not selected, and the lower of V_{CC} + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

7. The operating supply voltage range specification for the F-ZTAT (low-voltage) version is under investigation. Ranges of V_{CC} = 3.0 to 3.6 V and T_a = 0 to +75°C are planned for flash memory programming/erasing.

8. Current dissipation values are for V_{IH} min = V_{CC} – 0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

9. The values are for $V_{RAM} \leq V_{CC}$ < 2.7 V, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.

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Table 24.3   Permissible Output Currents

Conditions: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

| Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	SCL1, SCL0, SDA1, SDA0	I_{OL}	—	—	20	mA
	Ports 1, 2, 3		—	—	10	mA
	Other output pins		—	—	2	mA
Permissible output low current (total)	Total of ports 1, 2, and 3	$\Sigma\, I_{OL}$	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\Sigma\, -I_{OH}$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 24.3.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 24.1 and 24.2.


Table 24.3   Permissible Output Currents (cont)

Conditions: V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, T_a = –20 to +75°C (regular specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	SCL1, SCL0, SDA1, SDA0	I_{OL}	—	—	10	mA
	Ports 1, 2, 3		—	—	2	mA
	Other output pins		—	—	1	mA
Permissible output low current (total)	Total of ports 1, 2, and 3	$\Sigma\, I_{OL}$	—	—	40	mA
	Total of all output pins, including the above		—	—	60	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\Sigma\, -I_{OH}$	—	—	30	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 24.3.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 24.1 and 24.2.

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Table 24.4   Bus Drive Characteristics   **– Preliminary –**

Conditions: $V_{CC} = 2.7$ V to 5.5 V, $V_{SS} = 0$ V, Ta $= -20$ to $+75°C$

Applicable Pins: SCL1, SCL0, SDA1, SDA0 (bus drive function selected)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	V_T^-	$V_{CC} \times 0.3$	—	—	V	$V_{CC} = 2.7$ V to 5.5 V
	V_T^+	—	—	$V_{CC} \times 0.7$		$V_{CC} = 2.7$ V to 5.5 V
	$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—		$V_{CC} = 2.7$ V to 5.5 V
Input high voltage	V_{IH}	$V_{CC} \times 0.7$	—	$V_{CC} + 0.5$	V	$V_{CC} = 2.7$ V to 5.5 V
Input low voltage	V_{IL}	-0.5	—	$V_{CC} \times 0.3$		$V_{CC} = 2.7$ V to 5.5 V
Output low voltage	V_{OL}	—	—	0.8	V	$I_{OL} = 16$ mA, $V_{CC} = 4.5$ V to 5.5 V
		—	—	0.5		$I_{OL} = 8$ mA
		—	—	0.4		$I_{OL} = 3$ mA
Input capacitance	C_{in}	—	—	20	pF	$V_{in} = 0$ V, f $= 1$ MHz, $T_a = 25°C$
Three-state leakage current (off state)	$|I_{TSI}|$	—	—	1.0	µA	$V_{in} = 0.5$ to $V_{CC} - 0.5$ V
SCL, SDA output fall time	t_{Of}	$20 + 0.1Cb$	—	250	ns	$V_{CC} = 2.7$ V to 5.5 V
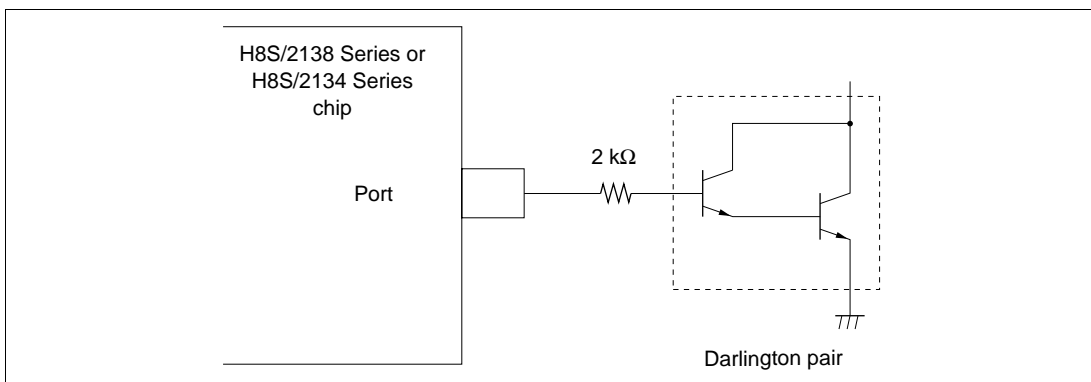
Figure 24.1   Darlington Pair Drive Circuit (Example)

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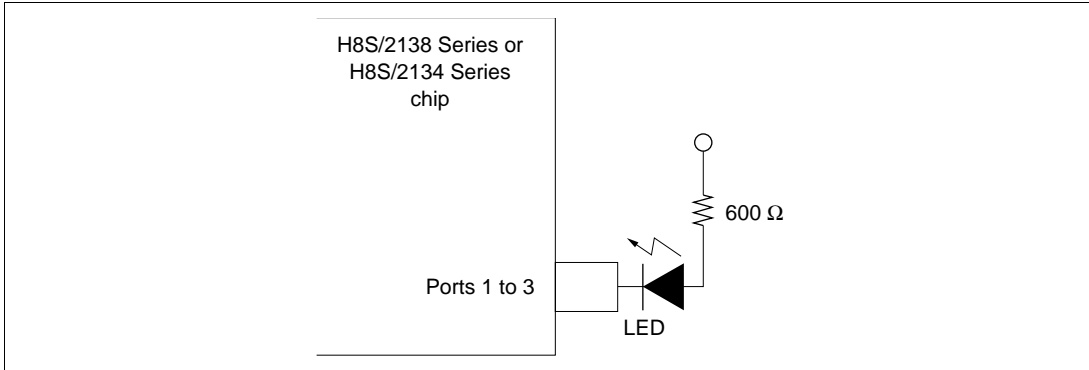
Figure 24.2   LED Drive Circuit (Example)

24.3   AC Characteristics

Figure 24.3 shows the test conditions for the AC characteristics.

C = 30 pF: All output ports
R_L = 2.4 kΩ
R_H = 12 kΩ

I/O timing test levels
• Low level: 0.8 V
• High level: 2.0 V
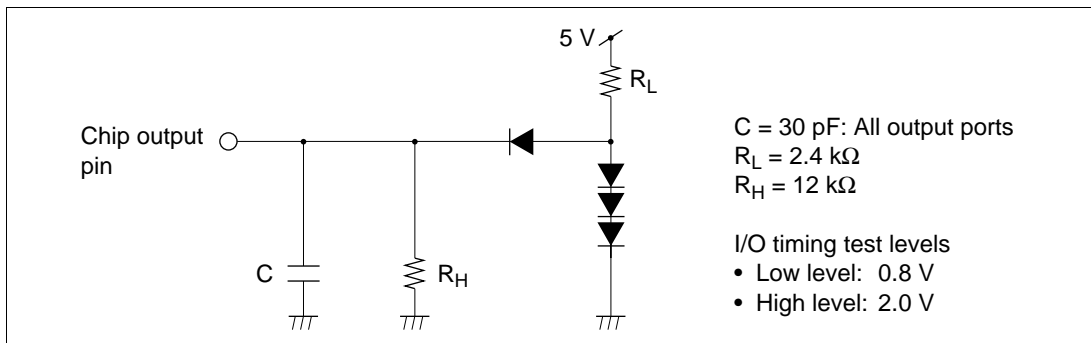
Figure 24.3   Output Load Circuit

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24.3.1 Clock Timing

Table 24.5 shows the clock timing. The clock timing specified here covers clock (ø) output and clock pulse generator (crystal) and external clock input (EXTAL pin) oscillation settling times. For details of external clock input (EXTAL pin and EXCL pin) timing, see section 22, Clock Pulse Generator.

Table 24.5   Clock Timing — Preliminary —

Condition A: $V_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = 0$ V, ø = 2 MHz to maximum operating frequency,
$T_a = -20$ to $+75°C$ (regular specifications),
$T_a = -40$ to $+85°C$ (wide-range specifications)

Condition B: $V_{CC} = 4.0$ V to 5.5V, $V_{SS} = 0$ V, ø = 2 MHz to maximum operating frequency,
$T_a = -20$ to $+75°C$ (regular specifications),
$T_a = -40$ to $+85°C$ (wide-range specifications)

Condition C: $V_{CC} = 2.7$ V to 5.5V, $V_{SS} = 0$ V, ø = 2 MHz to maximum operating frequency,
$T_a = -20$ to $+75°C$ (regular specifications)

Item	Symbol	Condition A 20 MHz Min	Max	Condition B 16 MHz Min	Max	Condition C 10 MHz Min	Max	Unit	Test Conditions
Clock cycle time	t_{cyc}	50	500	62.5	500	100	500	ns	Figure 24.4
Clock high pulse width	t_{CH}	17	—	20	—	30	—	ns	Figure 24.4
Clock low pulse width	t_{CL}	17	—	20	—	30	—	ns	
Clock rise time	t_{Cr}	—	8	—	10	—	20	ns	
Clock fall time	t_{Cf}	—	8	—	10	—	20	ns	
Oscillation settling time at reset (crystal)	t_{OSC1}	10	—	10	—	20	—	ms	Figure 24.5 Figure 24.6
Oscillation settling time in software standby (crystal)	t_{OSC2}	8	—	8	—	8	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	500	—	µs	

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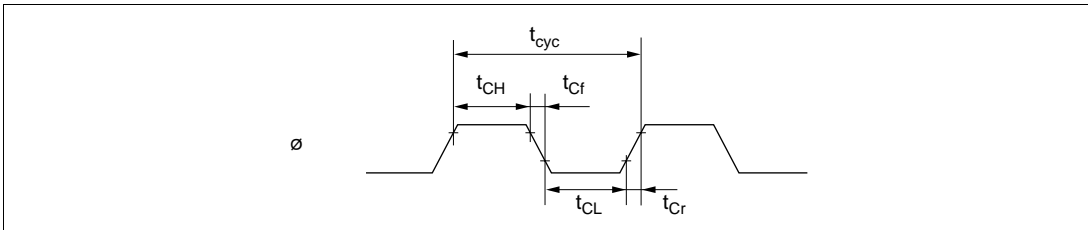
Figure 24.4   System Clock Timing
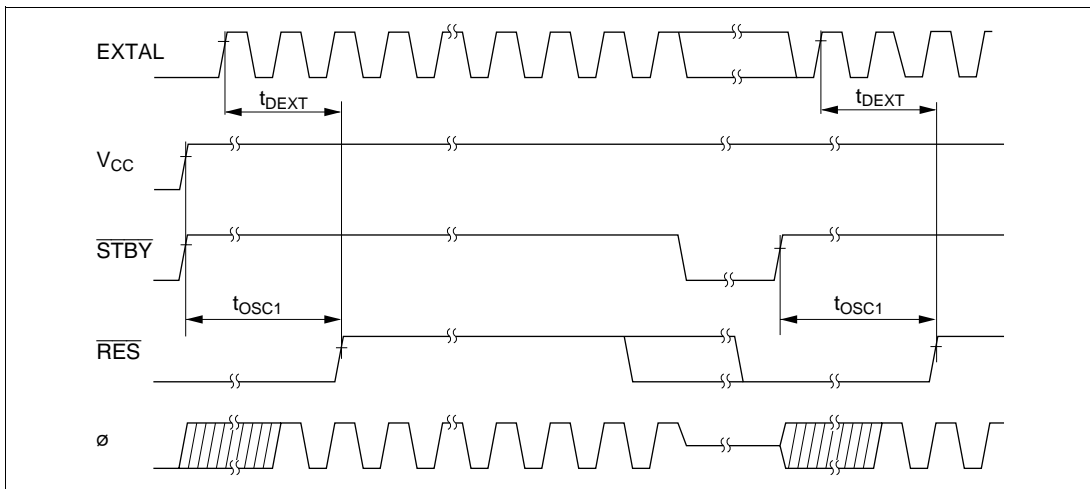
Figure 24.5   Oscillation Settling Timing
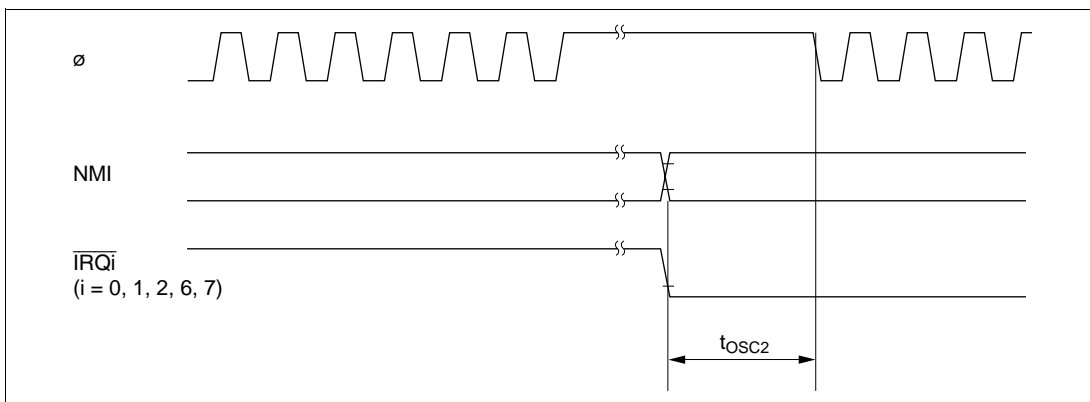
Figure 24.6   Oscillation Setting Timing (Exiting Software Standby Mode)

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24.3.2 Control Signal Timing

Table 24.6 shows the control signal timing. The only external interrupts that can operate on the subclock (ø = 32.768 kHz) are NMI and IRQ0, IRQ1, IRQ2, IRQ6, and IRQ7.
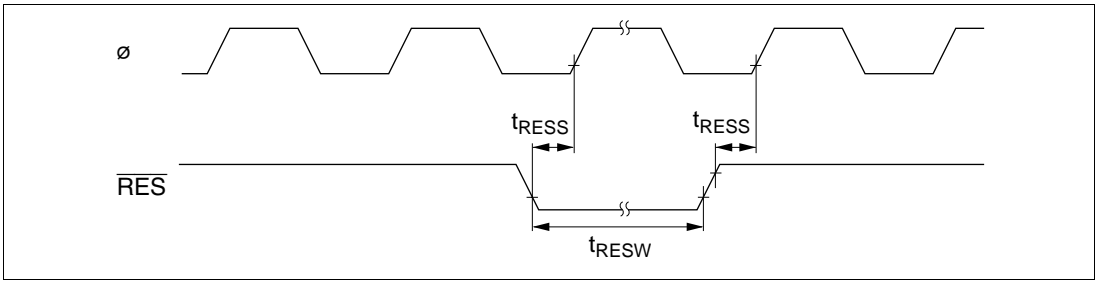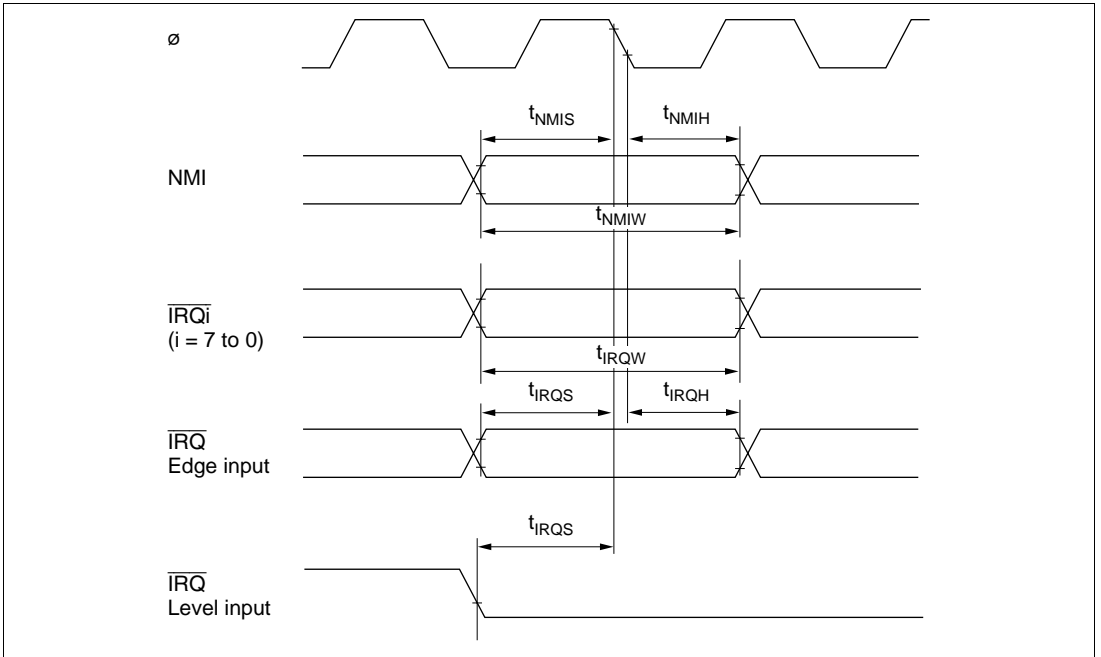
Table 24.6 Control Signal Timing   **– Preliminary –**

Condition A: V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5V, V_{SS} = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5V, V_{SS} = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications)

Item	Symbol	Condition A 20 MHz		Condition B 16 MHz		Condition C 10 MHz		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	300	—	ns	Figure 24.7
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	20	—	t_{cyc}	
NMI setup time (NMI)	t_{NMIS}	150	—	150	—	250	—	ns	Figure 24.8
NMI hold time (NMI)	t_{NMIH}	10	—	10	—	10	—		
NMI pulse width (exiting software standby mode)	t_{NMIW}	200	—	200	—	200	—	ns	
IRQ setup time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQS}	150	—	150	—	250	—	ns	
IRQ hold time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQH}	10	—	10	—	10	—	ns	
IRQ pulse width ($\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ2}$ to $\overline{IRQ0}$) (exiting software standby mode)	t_{IRQW}	200	—	200	—	200	—	ns	

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Figure 24.7   Reset Input Timing

Figure 24.8   Interrupt Input Timing

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24.3.3 Bus Timing

Table 24.7 shows the bus timing. Operation in external expansion mode is not guaranteed when operating on the subclock (ϕ = 32.768 kHz).

Table 24.7   Bus Timing — Preliminary —

Condition A: V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (regular specifications)

| Item	Symbol	Condition A 20 MHz Min	Condition A 20 MHz Max	Condition B 16 MHz Min	Condition B 16 MHz Max	Condition C 10 MHz Min	Condition C 10 MHz Max	Unit	Test Conditions
Address delay time	t_{AD}	—	20	—	30	—	40	ns	Figure 24.9 to figure 24.13
Address setup time	t_{AS}	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 30$	—	ns	
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 20$	—	ns	
$\overline{CS}$ delay time ($\overline{IOS}$)	t_{CSD}	—	20	—	30	—	40	ns	
$\overline{AS}$ delay time	t_{ASD}	—	30	—	45	—	60	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	30	—	45	—	60	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	30	—	45	—	60	ns	
Read data setup time	t_{RDS}	15	—	20	—	35	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 30$	—	$1.0 \times t_{cyc} - 40$	—	$1.0 \times t_{cyc} - 60$	ns	
Read data access time 2	t_{ACC2}	—	$1.5 \times t_{cyc} - 25$	—	$1.5 \times t_{cyc} - 35$	—	$1.5 \times t_{cyc} - 50$	ns	

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Condition A: $V_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = 0$ V, $\varnothing = 2$ MHz to maximum operating frequency,
$T_a = -20$ to $+75°C$ (regular specifications),
$T_a = -40$ to $+85°C$ (wide-range specifications)

Condition B: $V_{CC} = 4.0$ V to 5.5V, $V_{SS} = 0$ V, $\varnothing = 2$ MHz to maximum operating frequency,
$T_a = -20$ to $+75°C$ (regular specifications),
$T_a = -40$ to $+85°C$ (wide-range specifications)

Condition C: $V_{CC} = 2.7$ V to 5.5V, $V_{SS} = 0$ V, $\varnothing = 2$ MHz to maximum operating frequency,
$T_a = -20$ to $+75°C$ (regular specifications)

Item	Symbol	Condition A 20 MHz Min	Max	Condition B 16 MHz Min	Max	Condition C 10 MHz Min	Max	Unit	Test Conditions
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 30$	—	$2.0 \times t_{cyc} - 40$	—	$2.0 \times t_{cyc} - 60$	ns	Figure 24.9 to figure 24.13
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 25$	—	$2.5 \times t_{cyc} - 35$	—	$2.5 \times t_{cyc} - 50$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 30$	—	$3.0 \times t_{cyc} - 40$	—	$3.0 \times t_{cyc} - 60$	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	30	—	45	—	60	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	30	—	45	—	60	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 30$	—	$1.0 \times t_{cyc} - 40$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 30$	—	$1.5 \times t_{cyc} - 40$	—	ns	
Write data delay time	t_{WDD}	—	30	—	45	—	60	ns	
Write data setup time	t_{WDS}	0	—	0	—	0	—	ns	
Write data hold time	t_{WDH}	10	—	15	—	20	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	30	—	45	—	60	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	10	—	ns	
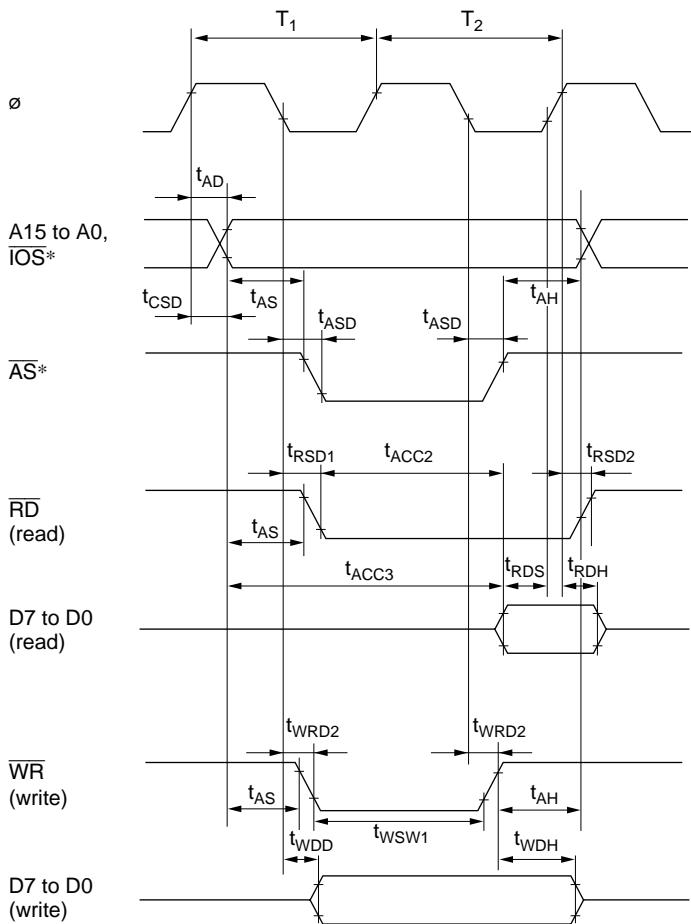
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Figure 24.9   Basic Bus Timing (Two-State Access)
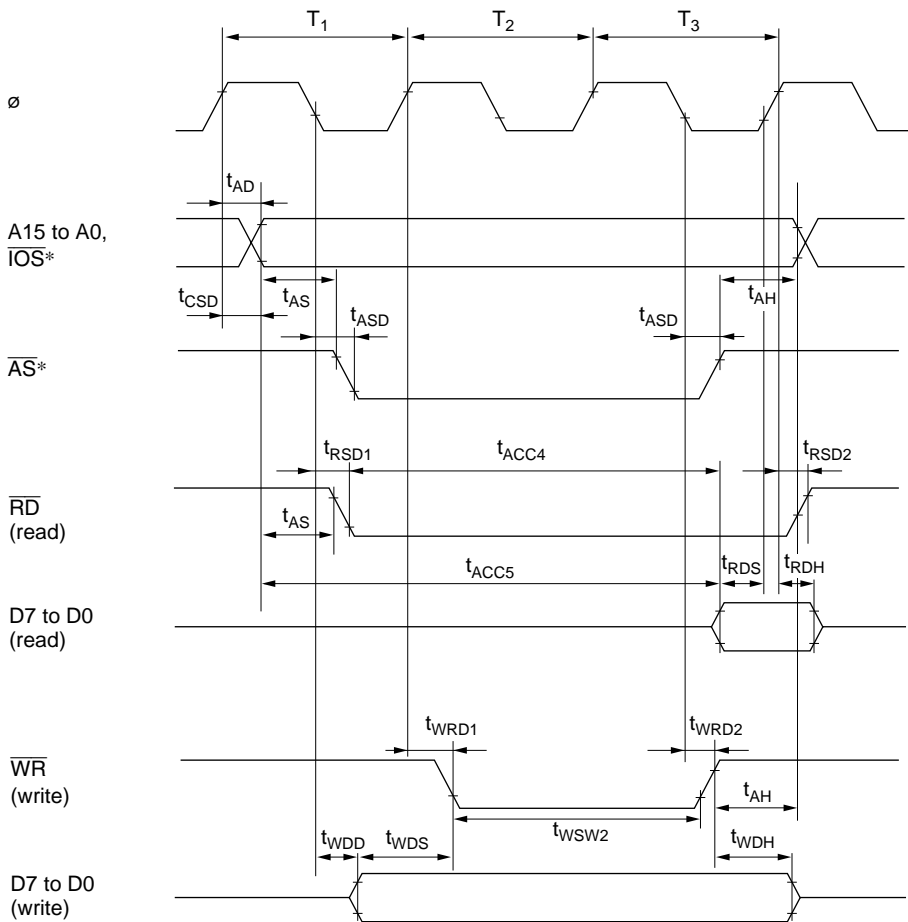
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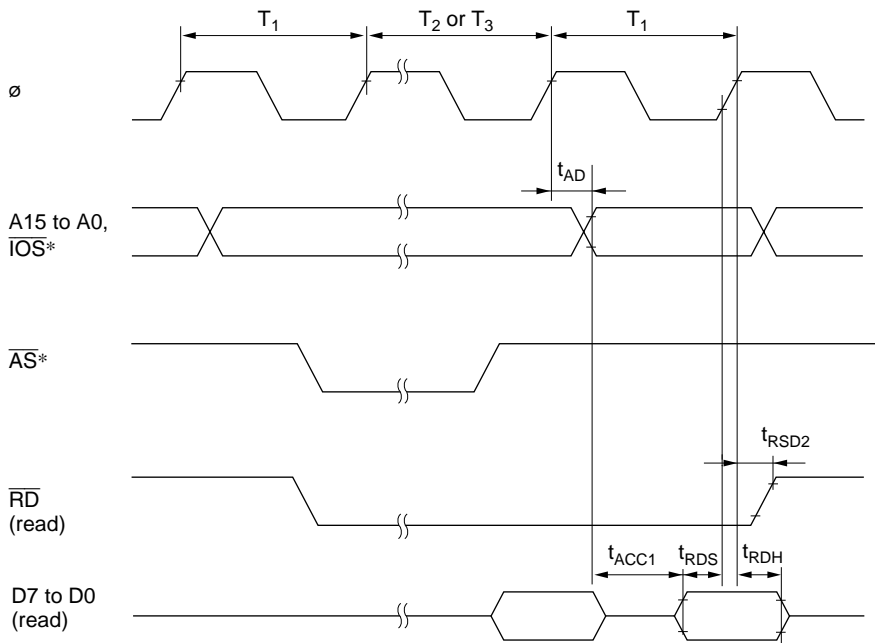**Figure 24.10   Basic Bus Timing (Three-State Access)**
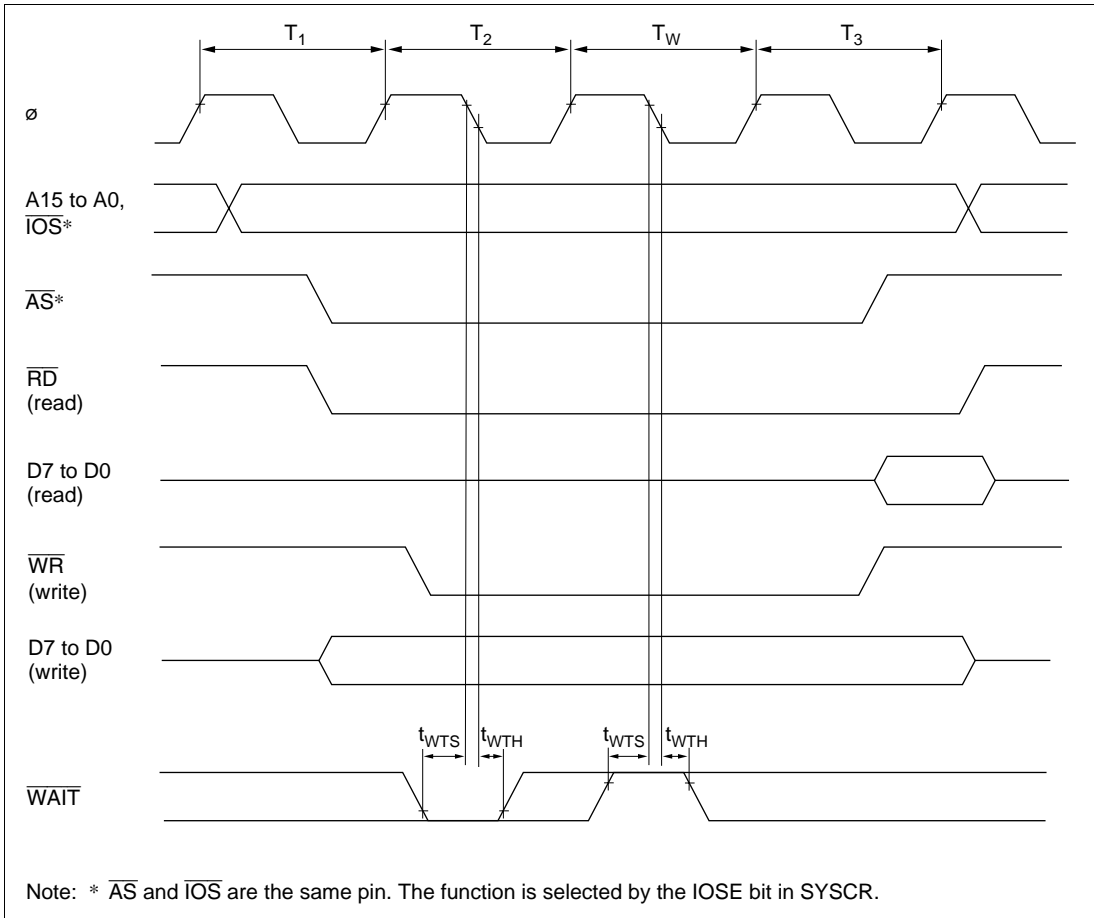
Figure 24.11   Basic Bus Timing (Three-State Access with One Wait State)

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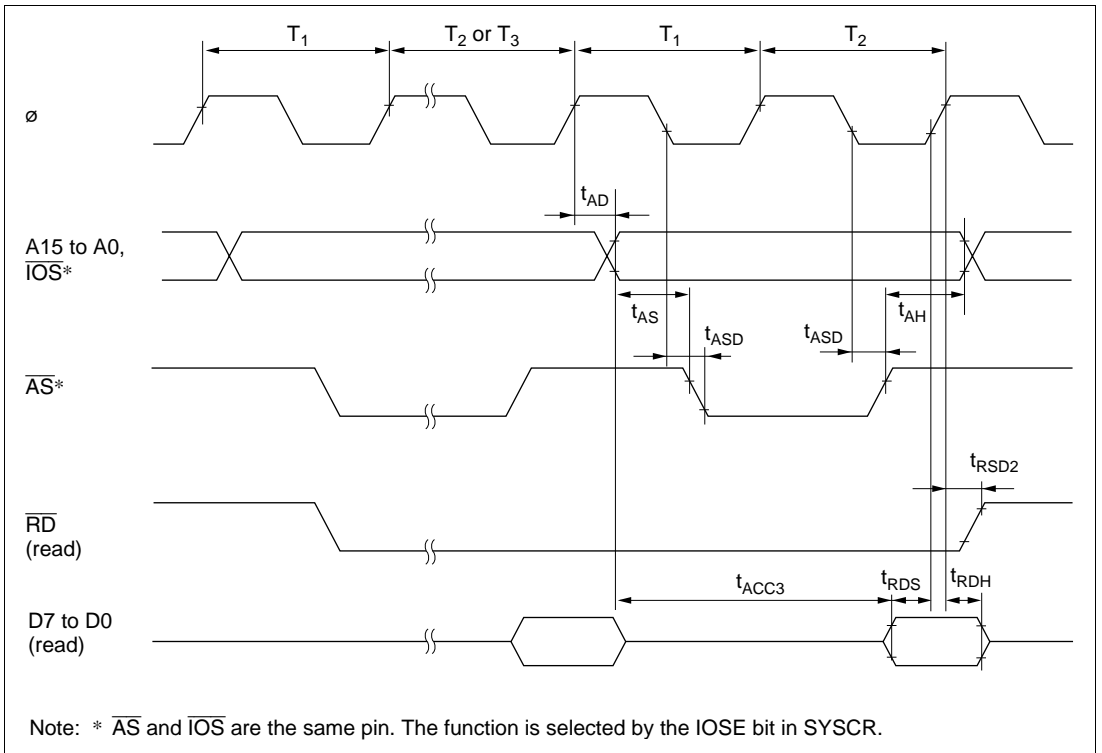
Figure 24.12   Burst ROM Access Timing (Two-State Access)

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Figure 24.13   Burst ROM Access Timing (One-State Access)

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24.3.4 Timing of On-Chip Supporting Modules

Tables 24.8 and 24.9 show the on-chip supporting module timing. The only on-chip supporting modules that can operate in subclock operation (ϕ = 32.768 kHz) are the I/O ports, external interrupts (NMI and IRQ0, 1, 2, 6, and 7), the watchdog timer, and the 8-bit timer (channels 0 and 1).

Table 24.8 Timing of On-Chip Supporting Modules (1)   **– Preliminary –**

Condition A: V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, ϕ = 32.768 kHz*, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5V, V_{SS} = 0 V, ϕ = 32.768 kHz*, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5V, V_{SS} = 0 V, ϕ = 32.768 kHz*, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications)

Item		Symbol	Condition A 20 MHz		Condition B 16 MHz		Condition C 10 MHz		Unit	Test Conditions
			Min	Max	Min	Max	Min	Max		
I/O ports	Output data delay time	t_{PWD}	—	50	—	50	—	100	ns	Figure 24.14
	Input data setup time	t_{PRS}	30	—	30	—	50	—		
	Input data hold time	t_{PRH}	30	—	30	—	50	—		
FRT	Timer output delay time	t_{FTOD}	—	50	—	50	—	100	ns	Figure 24.15
	Timer input setup time	t_{FTIS}	30	—	30	—	50	—		
	Timer clock input setup time	t_{FTCS}	30	—	30	—	50	—		Figure 24.16
	Timer clock pulse width	Single edge	t_{FTCWH}	1.5	—	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{FTCWL}	2.5	—	2.5	—	2.5	—		

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Table 24.8　Timing of On-Chip Supporting Modules (1) (cont)　　　　**– Preliminary –**

Condition A:　V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B:　V_{CC} = 4.0 V to 5.5V, V_{SS} = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C:　V_{CC} = 2.7 V to 5.5V, V_{SS} = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications)

Item		Symbol	Condition A 20 MHz Min	Max	Condition B 16 MHz Min	Max	Condition C 10 MHz Min	Max	Unit	Test Conditions
TMR	Timer output delay time	t_{TMOD}	—	50	—	50	—	100	ns	Figure 24.17
	Timer reset input setup time	t_{TMRS}	30	—	30	—	50	—		Figure 24.19
	Timer clock input setup time	t_{TMCS}	30	—	30	—	50	—		Figure 24.18
	Timer clock pulse width Single edge	t_{TMCWH}	1.5	—	1.5	—	1.5	—	t_{cyc}	
	Both edges	t_{TMCWL}	2.5	—	2.5	—	2.5	—		
PWM, PWMX	Pulse output delay time	t_{PWOD}	—	50	—	50	—	100	ns	Figure 24.20
SCI	Input clock cycle Asynchronous	t_{Scyc}	4	—	4	—	4	—	t_{cyc}	Figure 24.21
	Synchronous		6	—	6	—	6	—		
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time	t_{SCKr}	—	1.5	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time	t_{SCKf}	—	1.5	—	1.5	—	1.5		

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Table 24.8   Timing of On-Chip Supporting Modules (1) (cont)   – Preliminary –

Condition A: $V_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = 0$ V, $\phi = 32.768$ kHz*, 2 MHz to maximum operating
frequency, $T_a = -20$ to $+75°C$ (regular specifications),
$T_a = -40$ to $+85°C$ (wide-range specifications)

Condition B: $V_{CC} = 4.0$ V to 5.5V, $V_{SS} = 0$ V, $\phi = 32.768$ kHz*, 2 MHz to maximum operating
frequency, $T_a = -20$ to $+75°C$ (regular specifications),
$T_a = -40$ to $+85°C$ (wide-range specifications)

Condition C: $V_{CC} = 2.7$ V to 5.5V, $V_{SS} = 0$ V, $\phi = 32.768$ kHz*, 2 MHz to maximum operating
frequency, $T_a = -20$ to $+75°C$ (regular specifications)

| Item		Symbol	Condition A 20 MHz		Condition B 16 MHz		Condition C 10 MHz		Unit	Test Conditions
			Min	Max	Min	Max	Min	Max		
SCI	Transmit data delay time (synchronous)	t_{TXD}	—	50	—	50	—	100	ns	Figure 24.22
	Receive data setup time (synchronous)	t_{RXS}	50	—	50	—	100	—	ns	
	Receive data hold time (synchronous)	t_{RXH}	50	—	50	—	100	—	ns	
A/D converter	Trigger input setup time	t_{RGS}	30	—	30	—	50	—	ns	Figure 24.23

Note: * Only supporting modules that can be used in subclock operation
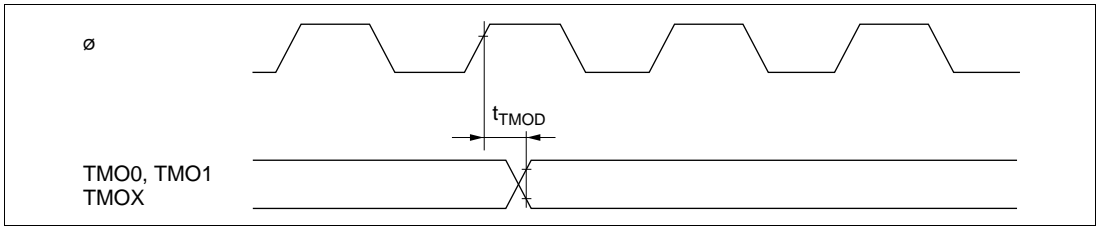
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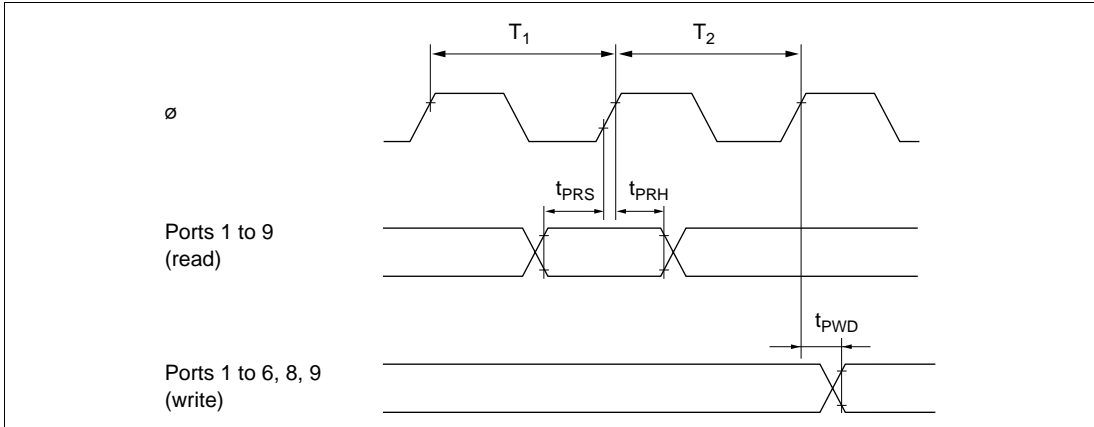
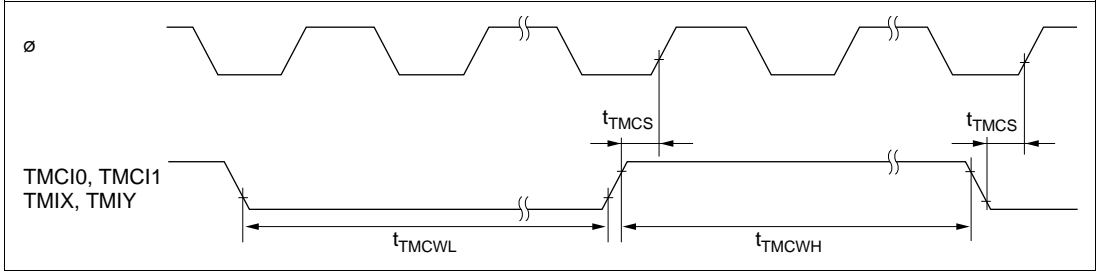**Figure 24.14   I/O Port Input/Output Timing**
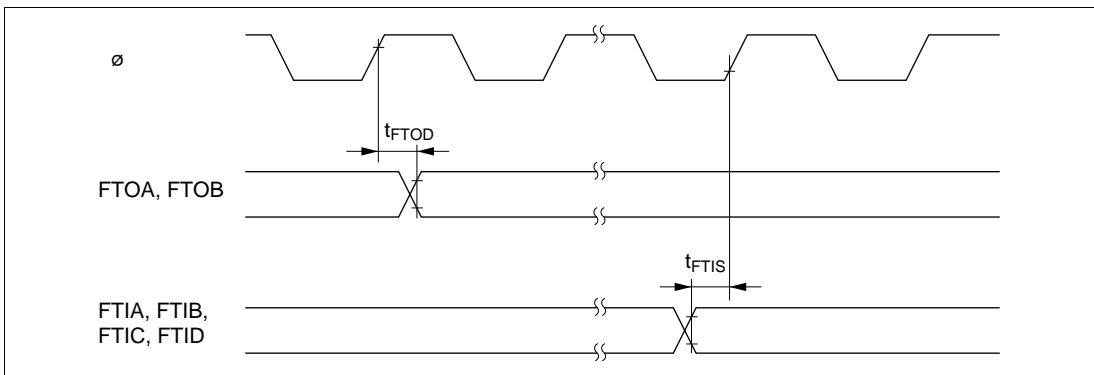
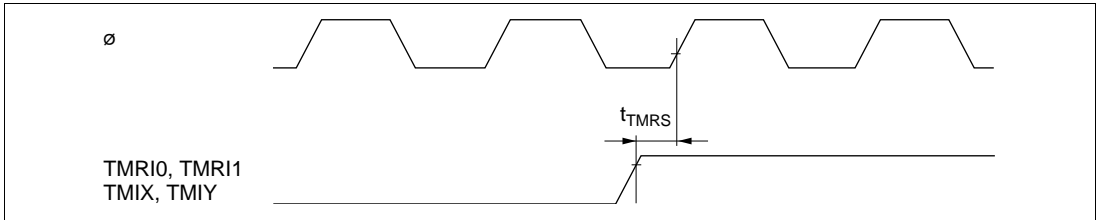**Figure 24.15   FRT Input/Output Timing**
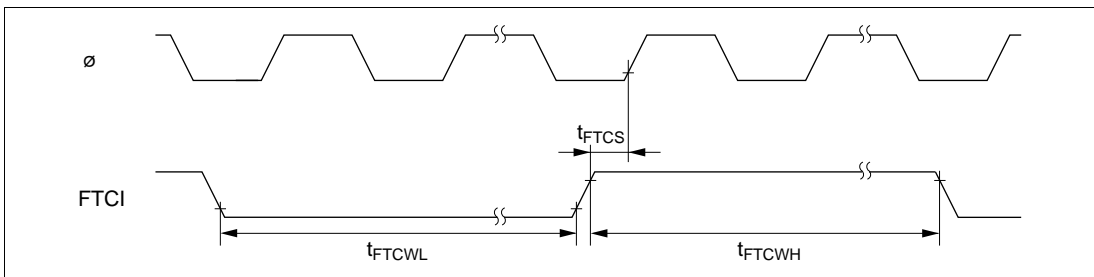
Figure 24.16   FRT Clock Input Timing
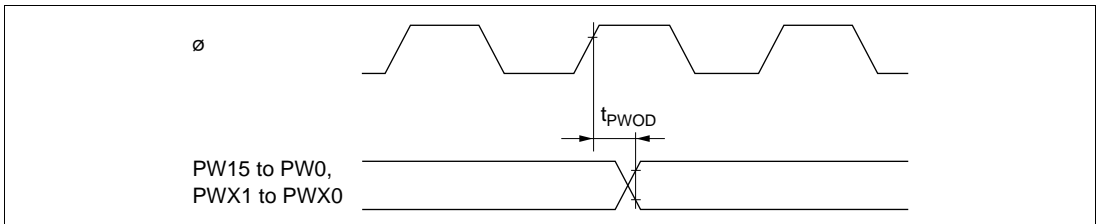
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Figure 24.17   8-Bit Timer Output Timing

Figure 24.18   8-Bit Timer Clock Input Timing
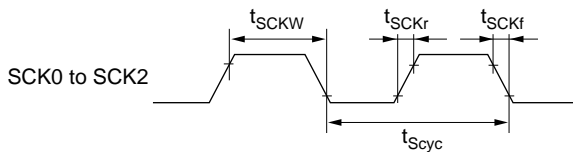

Figure 24.19   8-Bit Timer Reset Input Timing
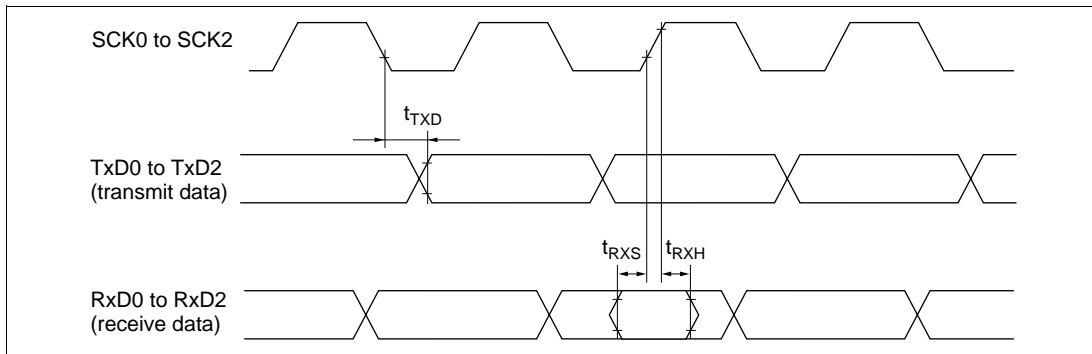

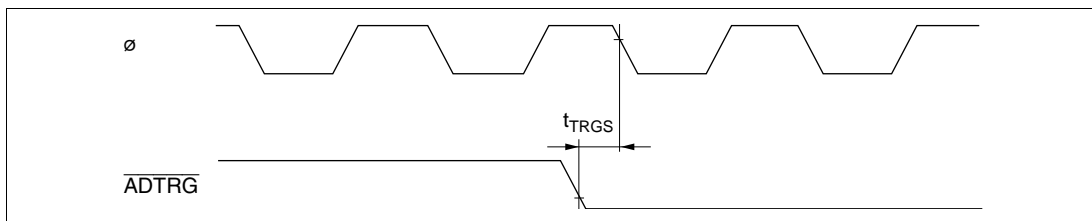**Figure 24.20   PWM, PWMX Output Timing**

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Figure 24.21   SCK Clock Input Timing

Figure 24.22   SCI Input/Output Timing (Synchronous Mode)

Figure 24.23   A/D Converter External Trigger Input Timing

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**Table 24.8   Timing of On-Chip Supporting Modules (2)**   **– Preliminary –**

Condition A: $V_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = 0$ V, ø = 2 MHz to maximum operating frequency,
               $T_a = -20$ to +75°C (regular specifications),
               $T_a = -40$ to +85°C (wide-range specifications)

Condition B: $V_{CC} = 4.0$ V to 5.5V, $V_{SS} = 0$ V, ø = 2 MHz to maximum operating frequency,
               $T_a = -20$ to +75°C (regular specifications),
               $T_a = -40$ to +85°C (wide-range specifications)

Condition C: $V_{CC} = 2.7$ V to 5.5V, $V_{SS} = 0$ V, ø = 2 MHz to maximum operating frequency,
               $T_a = -20$ to +75°C (regular specifications)

Item		Symbol	Condition A 20 MHz Min	Max	Condition B 16 MHz Min	Max	Condition C 10 MHz Min	Max	Unit	Test Conditions
HIF read cycle	$\overline{CS}$/HA0 setup item	t_{HAR}	10	—	10	—	10	—	ns	Figure 24.24
	$\overline{CS}$/HA0 hold time	t_{HRA}	10	—	10	—	10	—	ns	
	$\overline{IOR}$ pulse width	t_{HRPW}	120	—	120	—	220	—	ns	
	HDB delay time	t_{HRD}	—	100	—	100	—	200	ns	
	HDB hold time	t_{HRF}	0	25	0	25	0	40	ns	
	HIRQ delay time	t_{HIRQ}	—	120	—	120	—	200	ns	
HIF write cycle	$\overline{CS}$/HA0 setup item	t_{HAW}	10	—	10	—	10	—	ns	
	$\overline{CS}$/HA0 hold time	t_{HWA}	10	—	10	—	10	—	ns	
	$\overline{IOW}$ pulse width	t_{HWPW}	60	—	60	—	100	—	ns	
	HDB setup time Fast A20 gate not used	t_{HDW}	30	—	30	—	50	—	ns	
	Fast A20 gate used		45	—	55	—	85	—	ns	
	HDB hold time	t_{HWD}	15	—	15	—	25	—	ns	
	GA20 delay time	t_{HGA}	—	90	—	90	—	180	ns	

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Host interface read timing
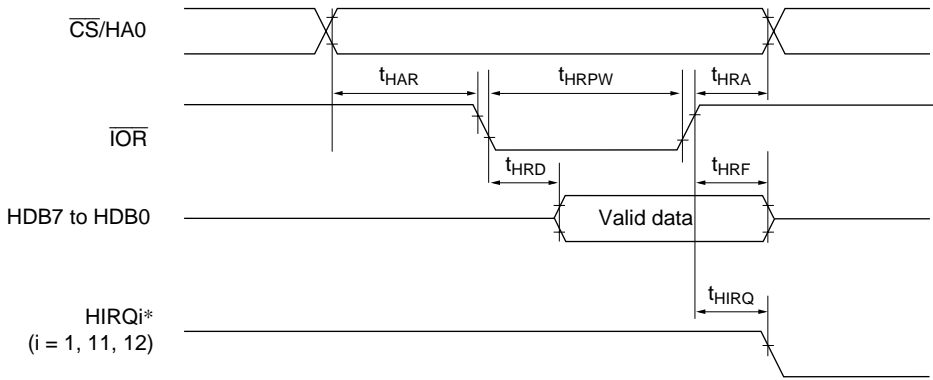
Note: * The rising edge timing is the same as the port 4 output timing.
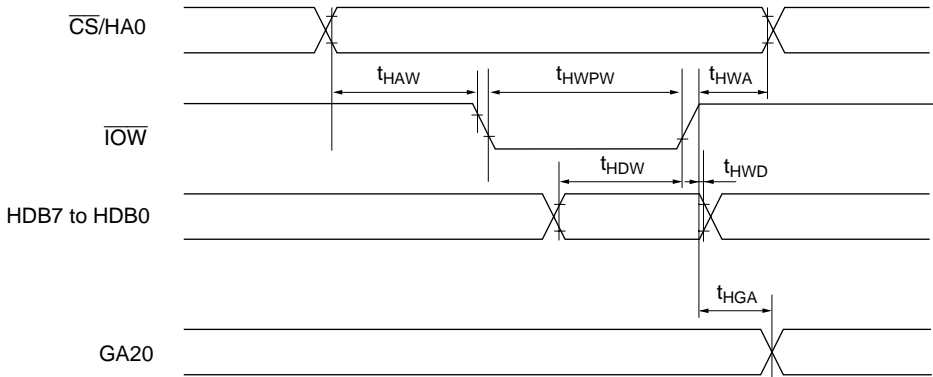See figure 24.14.

Host interface write timing

Figure 24.24 Host Interface Timing

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Conditions: V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, ø = 5 MHz to maximum operating frequency,
T_a = –20 to +75°C

Item	Symbol	Ratings			Unit	Test Conditions	Notes
		Min	Typ	Max			
SCL clock cycle time	t_{SCL}	12	—	—	t_{cyc}		Figure 24.25
SCL clock high pulse width	t_{SCLH}	3	—	—	t_{cyc}		
SCL clock low pulse width	t_{SCLL}	5	—	—	t_{cyc}		
SCL, SDA input rise time	t_{Sr}	—	—	7.5*	t_{cyc}		
SCL, SDA input fall time	t_{Sf}	—	—	300	ns		
SCL, SDA input spike pulse elimination time	t_{SP}	—	—	1	t_{cyc}		
SDA input bus free time	t_{BUF}	5	—	—	t_{cyc}		
Start condition input hold time	t_{STAH}	3	—	—	t_{cyc}		
Retransmission start condition input setup time	t_{STAS}	3	—	—	t_{cyc}		
Stop condition input setup time	t_{STOS}	3	—	—	t_{cyc}		
Data input setup time	t_{SDAS}	0.5	—	—	t_{cyc}		
Data input hold time	t_{SDAH}	0	—	—	ns		
SCL, SDA capacitive load	C_b	—	—	400	pF		

Note: * 17.5t_{cyc} can be set according to the clock selected for use by the I²C module. For details, see section 16.4, Usage Notes.

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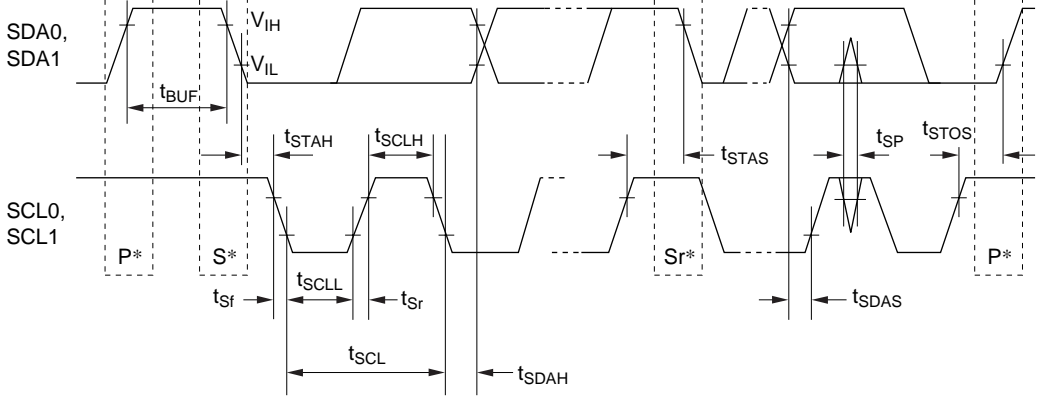
Note: * S, P, and Sr indicate the following conditions.

    S: Start condition
    P: Stop condition
    Sr: Retransmission start condition

Figure 24.25 I^{2}C Bus Interface Input/Output Timing (Option)

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24.4 A/D Conversion Characteristics

Tables 24.10 and 24.11 list the A/D conversion characteristics.

Table 24.10 A/D Conversion Characteristics
         (AN7 to AN0 Input: 134/266-State Conversion)   **– Preliminary –**

Condition A: $V_{CC} = 5.0$ V $\pm$ 10%, $AV_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = AV_{SS} = 0$ V, ø = 2 MHz to
        maximum operating frequency, $T_a = -20$ to $+75°C$ (regular specifications),
        $T_a = -40$ to $+85°C$ (wide-range specifications)

Condition B: $V_{CC} = 4.0$ V to 5.5 V, $AV_{CC} = 4.0$ V to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, ø = 2 MHz to
        maximum operating frequency, $T_a = -20$ to $+75°C$ (regular specifications),
        $T_a = -40$ to $+85°C$ (wide-range specifications)

Condition C: $V_{CC} = 2.7$ V to 5.5 V, $AV_{CC} = 2.7$ V to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, ø = 2 MHz to
        maximum operating frequency, $T_a = -20$ to $+75°C$ (regular specifications)

Item	Condition A 20 MHz			Condition B 16 MHz			Condition C 10 MHz			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	6.7	—	—	8.4	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*3 / 5*4	—	—	10*3 / 5*4	—	—	10*1 / 5*2	kΩ
Nonlinearity error	—	—	±3.0	—	—	±3.0	—	—	±7.0	LSB
Offset error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Full-scale error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	—	—	±4.0	—	—	±8.0	LSB

Notes: 1. When 4.0 V $\leq AV_{CC} \leq$ 5.5 V
     2. When 2.7 V $\leq AV_{CC} <$ 4.0 V
     3. When conversion time $\geq$ 11. 17 µs (CKS = 1 and ø $\leq$ 12 MHz, or CKS = 0)
     4. When conversion time < 11. 17 µs (CKS = 1 and ø > 12 MHz)

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Table 24.11 A/D Conversion Characteristics
(CIN7 to CIN0 Input: 134/266-State Conversion)   – Preliminary –

Condition A: $V_{CC} = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$, $\emptyset = 2\ MHz$ to maximum operating frequency, $T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Condition B: $V_{CC} = 4.0\ V$ to $5.5\ V$, $AV_{CC} = 4.0\ V$ to $5.5\ V$, $V_{SS} = AV_{SS} = 0\ V$, $\emptyset = 2\ MHz$ to maximum operating frequency, $T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Condition C: $V_{CC} = 2.7\ V$ to $5.5\ V$, $AV_{CC} = 2.7\ V$ to $5.5\ V$, $V_{SS} = AV_{SS} = 0\ V$, $\emptyset = 2\ MHz$ to maximum operating frequency, $T_a = -20$ to $+75°C$ (regular specifications)

| | Condition A | | | Condition B | | | Condition C | | | |
| | 20 MHz | | | 16 MHz | | | 10 MHz | | | |
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	6.7	—	—	8.4	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10[*3] / 5[*4]	—	—	10[*3] / 5[*4]	—	—	10[*1] / 5[*2]	kΩ
Nonlinearity error	—	—	±5.0	—	—	±5.0	—	—	±11.0	LSB
Offset error	—	—	±5.5	—	—	±5.5	—	—	±11.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	—	—	±11.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	—	—	±12.0	LSB

Notes: 1. When $4.0\ V \leq AV_{CC} \leq 5.5\ V$

2. When $2.7\ V \leq AV_{CC} < 4.0\ V$

3. When conversion time $\geq 11.\ 17$ µs (CKS = 1 and $\emptyset \leq 12$ MHz, or CKS = 0)

4. When conversion time $< 11.\ 17$ µs (CKS = 1 and $\emptyset > 12$ MHz)

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24.5　D/A Conversion Characteristics

Table 24.12 lists the D/A conversion characteristics.

Table 24.12　D/A Conversion Characteristics　　　　　　　　　　**– Preliminary –**

Condition A:　V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to
　　　　　　　maximum operating frequency, T_a = –20 to +75°C (regular specifications),
　　　　　　　T_a = –40 to +85°C (wide-range specifications)

Condition B:　V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to
　　　　　　　maximum operating frequency, T_a = –20 to +75°C (regular specifications),
　　　　　　　T_a = –40 to +85°C (wide-range specifications)

Condition C:　V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to
　　　　　　　maximum operating frequency, T_a = –20 to +75°C (regular specifications)

Item		Condition A 20 MHz			Condition B 16 MHz			Condition C 10 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	8	8	8	Bits
Conversion time	With 20 pF load capacitance	—	—	10	—	—	10	—	—	10	μs
Absolute accuracy	With 2 MΩ load resistance	—	±1.0	±1.5	—	±1.0	±1.5	—	±2.0	±3.0	LSB
	With 4 MΩ load resistance	—	—	±1.0	—	–	±1.0	—	—	±2.0	

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24.6　Flash Memory Characteristics

Table 24.13 shows the flash memory characteristics.

Table 24.13　Flash Memory Characteristics (5 V Version)[8]

Conditions:　V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V,
T_a = 0 to +75°C (Programming/erasing operating temperature)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Programming time[1],[2],[4]		tP	—	10	200	ms/ 32 bytes	
Erase time[1],[3],[5]		tE	—	100	1200	ms/ block	
Reprogramming count		N_{WEC}	—	—	100	Times	
Programming	Wait time after SWE-bit setting[1]	x	10	—	—	μs	
	Wait time after PSU-bit setting[1]	y	50	—	—	μs	
	Wait time after P-bit setting[1],[4]	z	150	—	200	μs	
	Wait time after P-bit clear[1]	α	10	—	—	μs	
	Wait time after PSU-bit clear[1]	β	10	—	—	μs	
	Wait time after PV-bit setting[1]	γ	4	—	—	μs	
	Wait time after dummy write[1]	ε	2	—	—	μs	
	Wait time after PV-bit clear[1]	η	4	—	—	μs	
	Maximum programming count[1],[4],[5]	N	—	—	1000	Times	tP = 200 μs

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Table 24.13 Flash Memory Characteristics (5 V Version)[8] (cont)

Conditions: $V_{CC} = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$,
$T_a = 0$ to $+75°C$ (Programming/erasing operating temperature)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Erase	Wait time after SWE-bit setting[1]	x	10	—	—	µs	
	Wait time after ESU-bit setting[1]	y	200	—	—	µs	
	Wait time after E-bit setting[1],[6]	z	5	—	10	ms	
	Wait time after E-bit clear[1]	α	10	—	—	µs	
	Wait time after ESU-bit clear[1]	β	10	—	—	µs	
	Wait time after EV-bit setting[1]	γ	20	—	—	µs	
	Wait time after dummy write[1]	ε	2	—	—	µs	
	Wait time after EV-bit clear[1]	η	5	—	—	µs	
	Maximum erase count[1],[6],[7]	N	—	—	120	Times	tE = 10 ms

Notes: 1. Set the times according to the program/erase algorithms.
2. Programming time per 32 bytes (Shows the total time the flash memory control register (FLMCR1) is set. It does not include the programming verification time.)
3. Block erase time (Shows the total period for which the E-bit in FLMCR1 is set. It does not include the erase verification time.)
4. Maximum programming time (tP (max) = wait time after P-bit setting (z) × maximum programming count (N))
5. Number of times when the wait time after P-bit setting (z) = 200 µs.
   The number of writes should be set according to the actual set value of z to allow programming within the maximum programming time (tP).
6. Maximum erase time (tE (max) = Wait time after E-bit setting (z) × maximum erase count (N))
7. Number of times when the wait time after E-bit setting (z) = 10 ms.
   The number of erases should be set according to the actual set value of z to allow erasing within the maximum erase time (tE).
8. Low-voltage version flash memory characteristics will be decided later.

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24.7 Usage Note

The F-ZTAT and mask ROM versions have been confirmed as fully meeting the reference values for electrical characteristics shown in this manual. However, actual performance figures, operating margins, noise margins, and other properties may vary due to differences in the manufacturing process, on-chip ROM, layout patterns, etc.

When system evaluation testing is carried out using the F-ZTAT version, the same evaluation tests should also be conducted for the mask ROM version when changing over to that version.

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Appendix F   Product Code Lineup

Table F.1   H8S/2138 Series and H8S/2134 Series Product Code Lineup   — Preliminary —

Product Type				Product Code	Mark Code	Package (Hitachi Package Code)	Notes
H8S/2138 Series	H8S/2138	Mask ROM version	Standard product (5 V version, 4 V version, 3 V version)	HD6432138	HD6432138(***)FA	80-pin QFP (FP-80A)	In planning stage
					HD6432138(***)TF	80-pin TQFP (TFP-80C)	
			Version with on-chip I^{2}C bus interface (5 V version, 4 V version, 3 V version)	HD6432138W	HD6432138W(***)FA	80-pin QFP (FP-80A)	
					HD6432138W(***)TF	80-pin TQFP (TFP-80C)	
		F-ZTAT version	Version with on-chip I^{2}C bus interface (5 V/4 V version)	HD64F2138	HD64F2138FA20	80-pin QFP (FP-80A)	Under development
					HD64F2138TF20	80-pin TQFP (TFP-80C)	
			Low-voltage version (3 V version)	HD64F2138V	HD64F2138VFA10	80-pin QFP (FP-80A)	Under development
					HD64F2138VTF10	80-pin TQFP (TFP-80C)	
	H8S/2137	Mask ROM version	Standard product (5 V version, 4 V version, 3 V version)	HD6432137	HD6432137(***)FA	80-pin QFP (FP-80A)	In planning stage
					HD6432137(***)TF	80-pin TQFP (TFP-80C)	
			Version with on-chip I^{2}C bus interface (5 V version, 4 V version, 3 V version)	HD6432137W	HD6432137W(***)FA	80-pin QFP (FP-80A)	
					HD6432137W(***)TF	80-pin TQFP (TFP-80C)	

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Table F.1 H8S/2138 Series and H8S/2134 Series Product Code Lineup (cont)

— Preliminary —

Product Type				Product Code	Mark Code	Package (Hitachi Package Code)	Notes
H8S/2134 Series	H8S/2134	Mask ROM version	Standard product (5 V version, 4 V version, 3 V version)	HD6432134	HD6432134(***)FA	80-pin QFP (FP-80A)	In planning stage
					HD6432134(***)TF	80-pin TQFP (TFP-80C)	
		F-ZTAT version	Standard product (5 V/4 V version)	HD64F2134	HD64F2134FA20	80-pin QFP (FP-80A)	
					HD64F2134TF20	80-pin TQFP (TFP-80C)	
			Low-voltage version (3 V version)	HD64F2134V	HD64F2134VFA10	80-pin QFP (FP-80A)	Under development
					HD64F2134VTF10	80-pin TQFP (TFP-80C)	
	H8S/2133	Mask ROM version	Standard product (5 V version, 4 V version, 3 V version)	HD6432133	HD6432133(***)FA	80-pin QFP (FP-80A)	In planning stage
					HD6432133(***)TF	80-pin TQFP (TFP-80C)	
	H8S/2132	Mask ROM version	Standard product (5 V version, 4 V version, 3 V version)	HD6432132	HD6432132(***)FA	80-pin QFP (FP-80A)	Under development
					HD6432132(***)TF	80-pin TQFP (TFP-80C)	
		F-ZTAT version	Standard product (5 V/4 V version)	HD64F2132	HD64F2132FA20	80-pin QFP (FP-80A)	
					HD64F2132TF20	80-pin TQFP (TFP-80C)	
			Low-voltage version (3 V version)	HD64F2132V	HD64F2132VFA10	80-pin QFP (FP-80A)	Under development
					HD64F2132VTF10	80-pin TQFP (TFP-80C)	
	H8S/2130	Mask ROM version	Standard product (5 V version, 4 V version, 3 V version)	HD64F2130	HD6432130(***)FA	80-pin QFP (FP-80A)	Under development
					HD6432130(***)TF	80-pin TQFP (TFP-80C)	

Note: (***) is the ROM code.

The F-ZTAT version of the H8S/2138 has an on-chip I^2C bus interface as standard.

The F-ZTAT 5 V/4 V version supports the operating ranges of the 5 V version and the 4 V version.

The operating range of the F-ZTAT low-voltage version will be decided later.

The above table includes products in the planning stage or under development. Information on the status of individual products can be obtained from Hitachi's sales offices.

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H8S/2138 Series and H8S/2134 Series Hardware Manual Supplementary Edition

Publication Date: 1st Edition, August 1998
Published by: Electronic Devices Sales & Marketing Group
                   Hitachi, Ltd.
Edited by: Technical Documentation Group
                   UL Media Co., Ltd.