

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS118

DECEMBER 1983 — REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

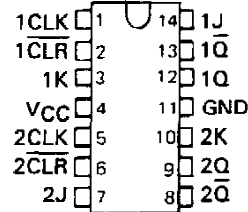
description

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \bar{Q} output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7473, and the SN74LS73A are characterized for operation from 0°C to 70°C .

SN5473, SN54LS73A . . . J OR W PACKAGE
SN7473 . . . N PACKAGE
SN74LS73A . . . D OR N PACKAGE
(TOP VIEW)



73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	
H	\downarrow	X	X	Q_0	\bar{Q}_0

'LS73A
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	
H	\downarrow	X	X	Q_0	\bar{Q}_0

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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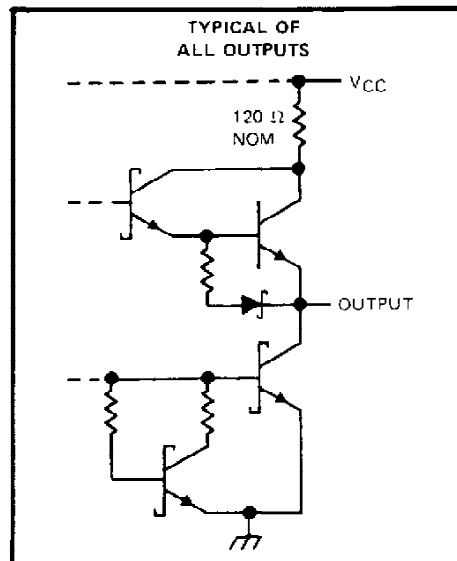
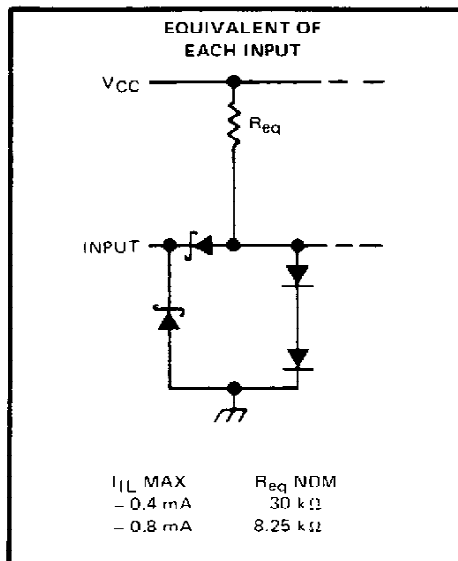
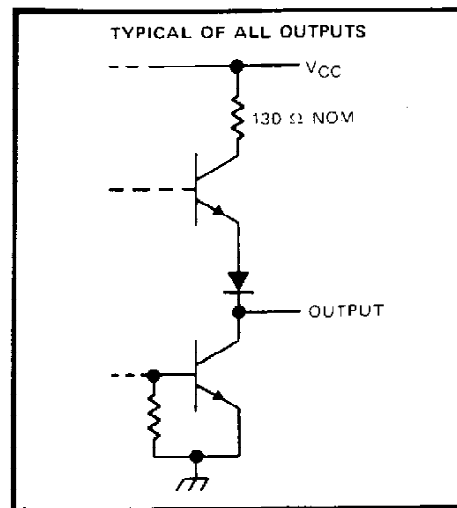
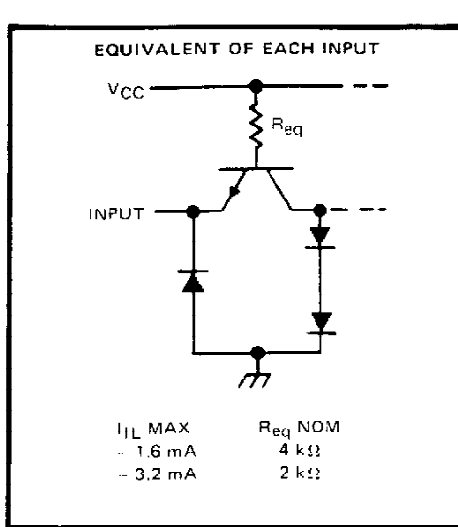
SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

logic symbols†



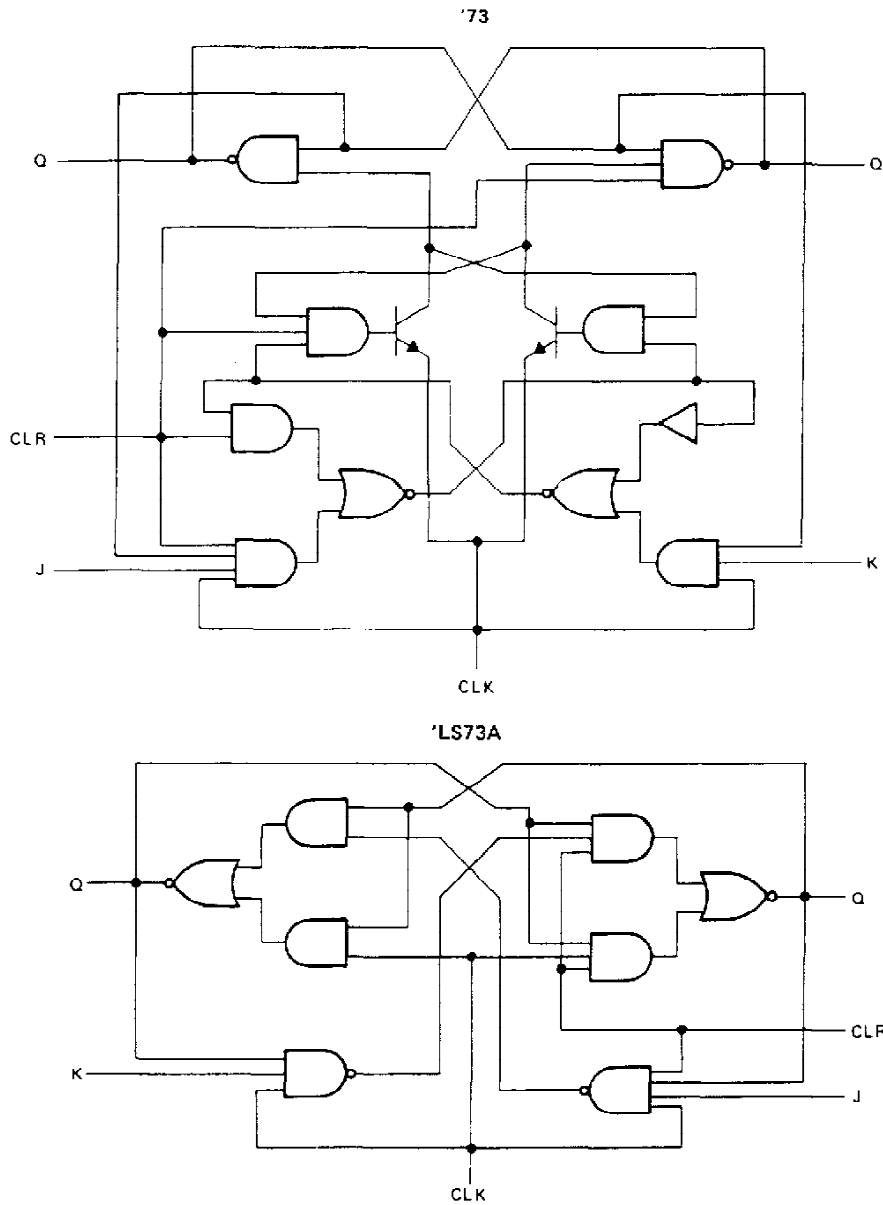
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage: '73	5.5 V
'LS73A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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SN5473, SN7473

DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

	SN5473			SN7473			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	6.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			16			16	mA
t _w Pulse duration	CLK high	20		20			ns
	CLK low	47		47			
	CLR low	25		25			
t _{su} Input setup time before CLK †	0			0			ns
t _h Input hold time data after CLK †	0			0			ns
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5473		SN7473		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5		-1.5	V	
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4			2.4 3.4	V	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA			0.2	0.4		V	
I _I	V _{CC} = MAX, V _I = 5.5 V			1		1	mA	
I _{IH}	J or K			40		40	μA	
	CLR or CLK			80		80		
I _{IL}	J or K			-1.6		-1.6	mA	
	CLR			-3.2		-3.2		
	CLK			-3.2		-3.2		
I _{OS} §	V _{CC} = MAX	-20		-57		-18 -57	mA	
I _{CC} ¶	V _{CC} = MAX, See Note 2			10	20	10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

¶ Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 400 Ω, C _L = 15 pF	15	20		MHz
t _{PLH}	CLR	\bar{Q}			16	25	ns
t _{PHL}		Q			25	40	ns
t _{PLH}	CLK	Q or \bar{Q}			16	25	ns
t _{PHL}						25	40

#f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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SN54LS73A, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

		SN54LS73A			SN74LS73A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.7			V
I_{OH}	High-level output current				-0.4			mA
I_{OL}	Low-level output current				4			mA
f_{clock}	Clock frequency	0			30			MHz
t_w	Pulse duration	CLK high		20		20		ns
		CLR low		25		20		
t_{su}	Set up time-before CLK ↓	data high or low		20		20		ns
		CLR inactive		20		20		
t_h	Hold time-data after CLK ↓	0			0			ns
T_A	Operating free-air temperature	-55		125		0		70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS73A		SN74LS73A		UNIT
		MIN	TYP‡	MAX	MIN	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5		-1.5		V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4	2.7	3.4	V
V_{OL}	$V_{CC} = \text{MIN}, I_{OL} = 4 \text{ mA}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}$	0.25	0.4	0.25	0.4	V
	$V_{CC} = \text{MIN}, I_{OL} = 8 \text{ mA}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}$			0.35	0.5	
I_I	J or K			0.1		mA
	CLR	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.3		
	CLK			0.4		
I_{IH}	J or K			20		μA
	CLR	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		60		
	CLK			80		
I_{IL}	J or K			-0.4		mA
	CLR or CLK	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.8		
$I_{OS}§$	$V_{CC} = \text{MAX}, \text{ See Note 4}$	-20	-100	-20	-100	mA
I_{CC} (Total)	$V_{CC} = \text{MAX}, \text{ See Note 2}$	4	6	4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$	30	45		MHz
t_{PLH}	CLR or CLK	Q or \bar{Q}		15	20		ns
t_{PHL}				15	20		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.


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