Revision A2 may be identified by the date/revision brand yywwA2, where yy and ww are the year and workweek of manufacture, respectively. This errata sheet is valid only when used in conjunction with the most current version of the data sheet available from Dallas Semiconductor via the Internet.

This document contains the following types of information:

Errata: These are design errors that deviate from published specifications. Errata are intended to be fixed in subsequent revisions of the device.

Specification Modifications: These are changes to the published specifications and will be reflected in the next update of the documentation and apply to all subsequent revisions of the device.

Documentation Changes: This information includes typographical mistakes, errors, omissions or clarifications of device operation. Items listed in this section will be reflected in the next update of the documentation.

ERRATA

1. The maximum operating speed of the microcontroller core over the temperature range and voltage limits is 33 MHz. If the clock multiplier is used, the external oscillator or crystal frequency must be scaled appropriately so that the internal clock speed does not exceed 33 MHz.

   Work Around: None. Operating speed will be increased in later revisions.

2. The In-Application Programming feature is not functional when operating with program in internal flash memory or SRAM.

   Work Around: None. However this feature does operate normally in an external program memory

3. To enter loader mode, port pin P3.7 must be pulled high when the pin biasing combination of RST=1, $\overline{PSEN}$ = $\overline{EA}$ =0 is applied.

   Work Around: None.

4. MOVC instructions executed from internal SRAM (locations 0400h-07FFh) when the internal SRAM is configured as program memory (PRAME=1) will not execute correctly.

   Work Around: None.

5. Under some circumstances, writes to parallel I/O ports can be delayed one clock cycle. In most cases, this will have no effect on system operation. If the immediately following instruction reads that modified port, however, the read instruction may read the port before its output value has changed. This behavior would differ from that of the traditional 8051.

Work Around: In most cases, none will be necessary. If the application software incorporates the unlikely occurrence of a port write immediately followed by a read of that port, a NOP can be inserted between the two instructions to incorporate sufficient delay to obviate the problem. This erratum will be fixed in the next revision.

6. The device will not fetch from internal flash memory if all three port pins P2.5, P2.6, and P2.7 are held low during a power-on reset.

   Work around: When internal code fetching is desired ($\overline{EA}$ =1), make certain that at least one of the three pins P2.5, P2.6, or P2.7 is not being held low during a power-on reset.

7. Any Read-Modify-Write (RMW) instruction that has P0, P1, P2, or P3 as its destination (such as ANL P0, #data) can incorrectly activate the strong internal pull-up for two clock cycles. This will only occur if a pin is at a logic 0 state and the result of the RMW instruction writes a logic 1 to the corresponding bit in the port latch, even if the bit was previously 1. If external logic connected to that pin is holding it at a logic 0, the strong internal driver can cause the pin to glitch momentarily to a logic 1. This behavior contradicts the data sheet which indicates that the strong internal pull-up should only be activated when a 0-to-1 transition is required on a port pin. A complete list of RMW instructions is contained in the DS89C420 User's Guide.

   Work around: When using a port pin as an input, always make certain that any external device driving a logic 0 can sink sufficient current to keep the pin voltage below +0.8V (V_{IL}) during the temporary activation of the internal pull-up (V_{OH2}).

8. Bootstrap loader mode will not operate correctly if any of the lock bits (LB1, LB2, LB3) are set.

   Work around: If any of the lock bits had been set by a previous session, erase the part using the K command, exit and reenter the bootstrap loader mode. The part will now accept bootstrap loader commands correctly.

SPECIFICATION MODIFICATIONS

1. NONE

DOCUMENTATION CHANGES

1. NONE