

SN74LS373, SN74LS374

Octal Transparent Latch with 3-State Outputs; Octal D-Type Flip-Flop with 3-State Output

The SN74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

The SN74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all ON Semiconductor TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			-2.6	mA
I_{OL}	Output Current – Low			24	mA

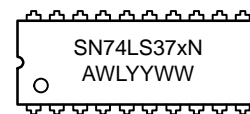
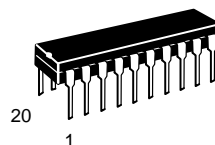


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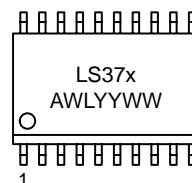
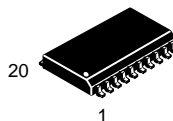
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**LOW
POWER
SCHOTTKY**

MARKING DIAGRAMS



**PDIP-20
N SUFFIX
CASE 738**



**SOIC-20
DW SUFFIX
CASE 751D**

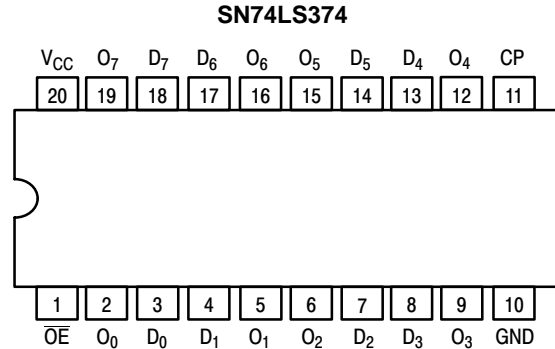
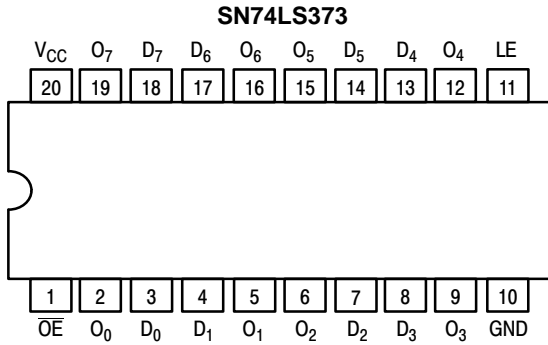
x = 3 or 4
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
SN74LS373N	PDIP-20	1440 Units/Box
SN74LS373DW	SOIC-20	2500/Tape & Reel
SN74LS374N	PDIP-20	1440 Units/Box
SN74LS374DW	SOIC-20	2500/Tape & Reel

SN74LS373, SN74LS374

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

D₀ - D₇ Data Inputs
 LE Latch Enable (Active HIGH) Input
 CP Clock (Active HIGH Going Edge) Input
 \overline{OE} Output Enable (Active LOW) Input
 O₀ - O₇ Outputs

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 U.L.	15 U.L.

TRUTH TABLE

LS373

D _n	LE	\overline{OE}	O _n
H	H	L	H
L	H	L	L
X	L	L	Q ₀
X	X	H	Z*

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

* Note: Contents of flip-flops unaffected by the state of the Output Enable input (\overline{OE}).

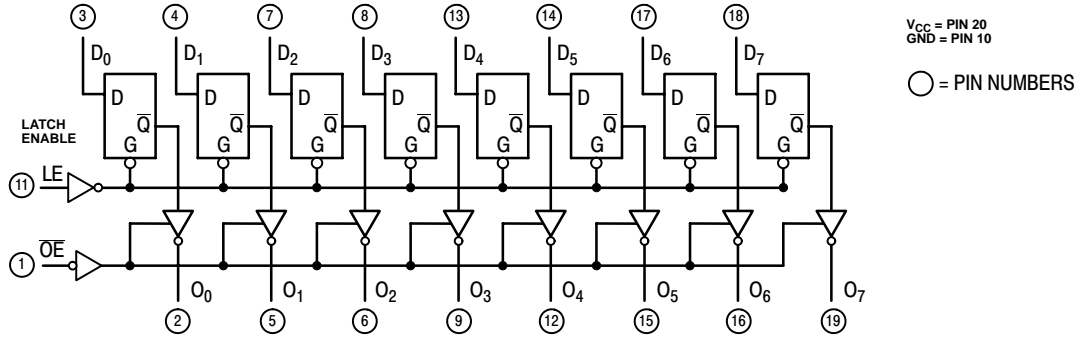
LS374

D _n	LE	\overline{OE}	O _n
H		L	H
L		L	L
X	X	H	Z*

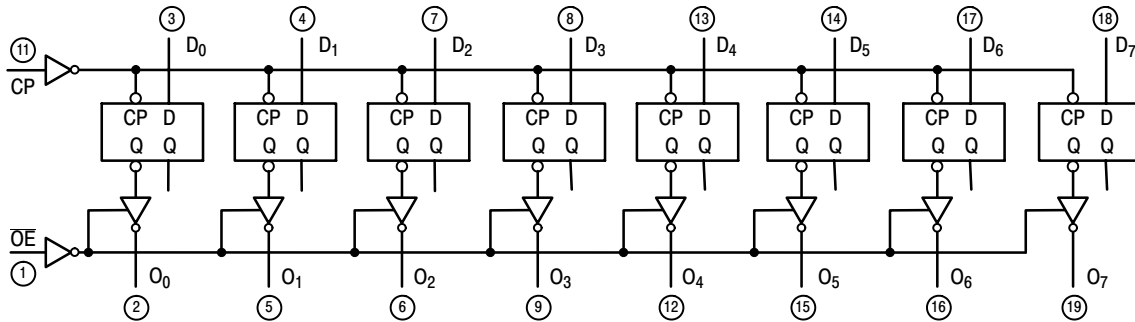
SN74LS373, SN74LS374

LOGIC DIAGRAMS

SN74LS373



SN74LS374



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4	3.1		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage		0.25	0.4	V	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
			0.35	0.5	V	
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1.)	-30		-130	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			40	mA	V _{CC} = MAX

1. Not more than one output should be shorted at a time, nor for more than 1 second.

SN74LS373, SN74LS374

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency				35	50		MHz	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	
t_{PLH} t_{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	$C_L = 5.0\text{ pF}$

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t_W	Clock Pulse Width	15		15		ns
t_s	Setup Time	5.0		20		ns
t_h	Hold Time	20		0		ns

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN74LS373, SN74LS374

SN74LS373

AC WAVEFORMS

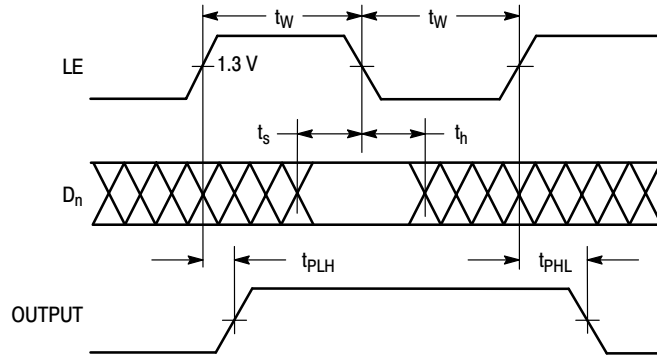


Figure 1.

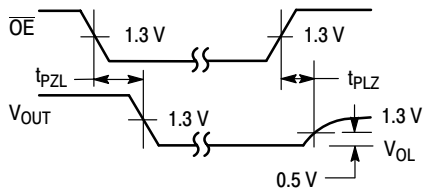


Figure 2.

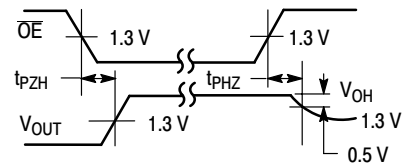
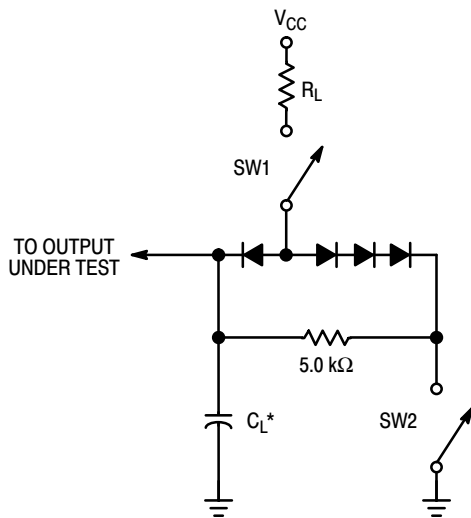


Figure 3.

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 4.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SN74LS373, SN74LS374

SN74LS374

AC WAVEFORMS

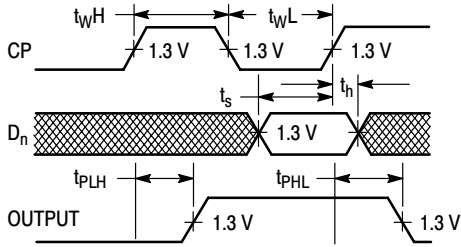


Figure 5.

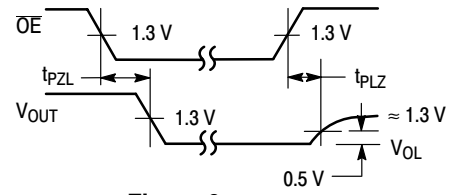


Figure 6.

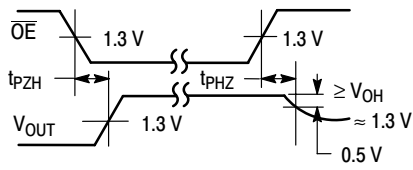
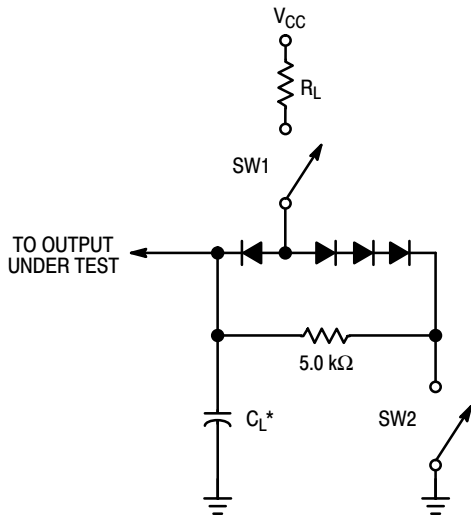


Figure 7.

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

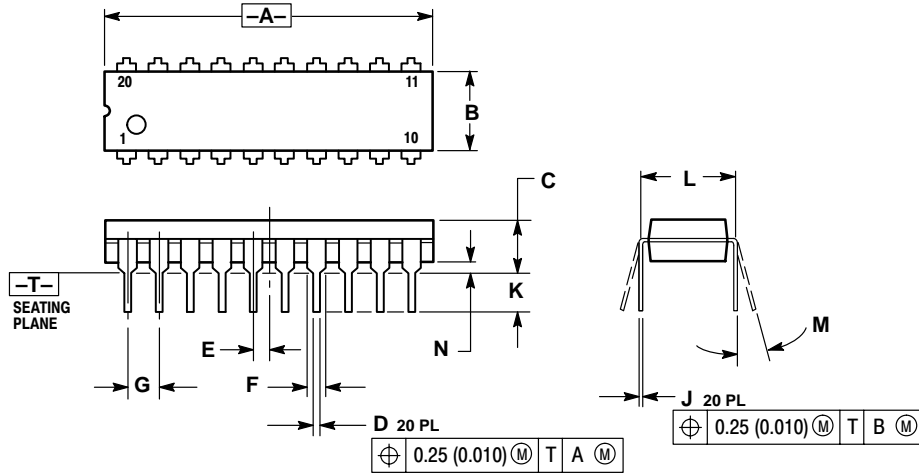
SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

Figure 8.

SN74LS373, SN74LS374

PACKAGE DIMENSIONS

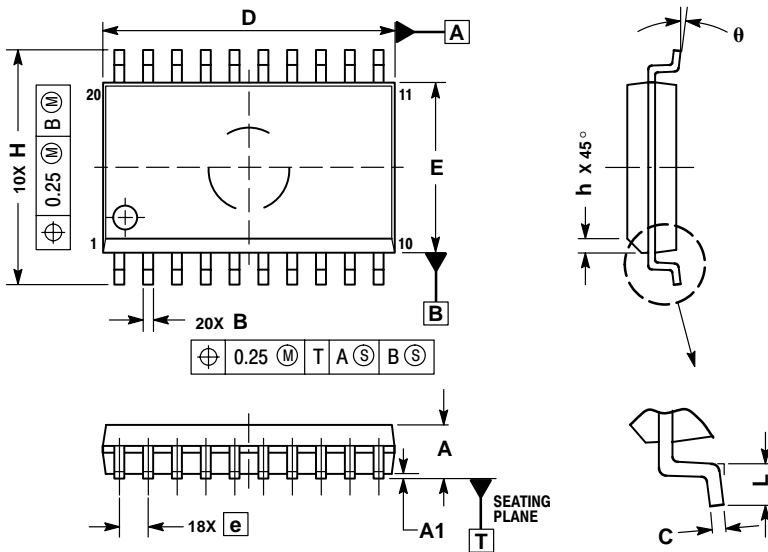
N SUFFIX PLASTIC PACKAGE CASE 738-03 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

D SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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