64-Bit Read/Write Memories

General Description

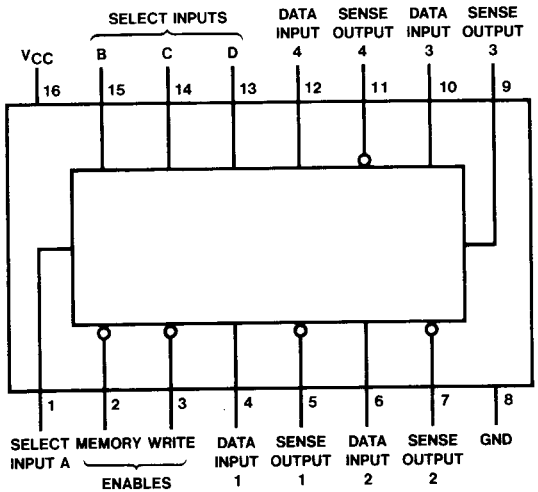
The DM5489B/DM7489B, DM54L89A/DM74L89A are fully decoded 64-bit RAMs organized as 16, 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

The "A" suffix on the low power versions is used to denote that full "tenth-power" technology has been employed in building this RAM.

Features

- For application as a "scratch pad" memory with nondestructive read-out
- Fully decoded memory organized as 16 words of four bits each
- Fast access time — DM54/74—35 ns typical; DM54L/74L—110 ns
- Diode-clamped, buffered inputs
- Open-collector outputs provide wire-OR capability
- Typical power dissipation — DM54/74—400 mW; DM54L/74L—75 mW
- Pin compatible with 3101, MM5501

Connection Diagram



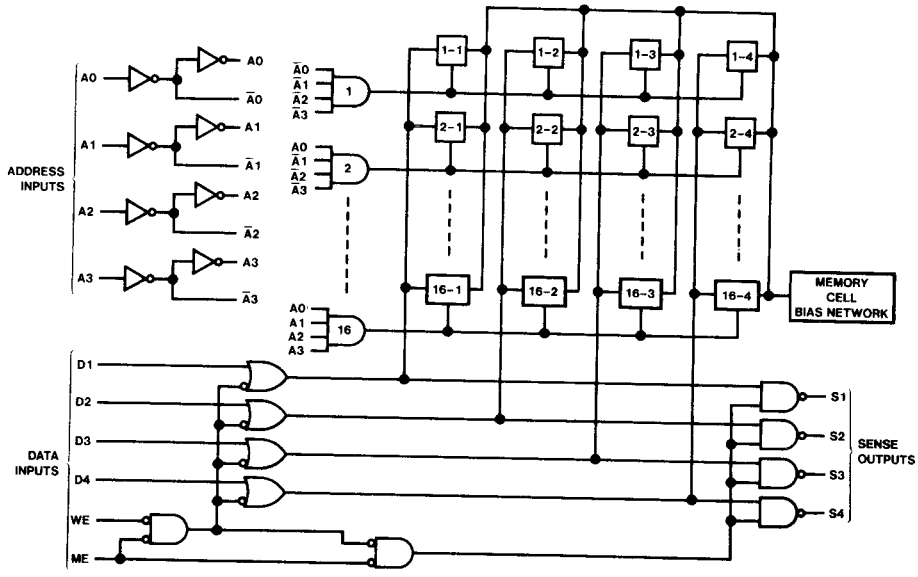
5489 (J)
54L89A (J,W)

7489 (N)
74L89A (N)

Truth Table

Memory Enable	Write Enable	Operation	Outputs
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

Logic Diagram



Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM54/74 89			DM54/74 L89A			Units
				Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, V_{OH} = 5.5 V	DM54			100			50	μA
			DM74			20			50	
I_{OL}	Low Level Output Current		DM54			12			2.0	mA
			DM74			12			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OL} = Max	DM54			0.4			0.3	V
			DM74			0.4			0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V				40			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V						−0.18	mA
			V_I = 0.4 V			−1.6				
I_{CC}	Supply Current	V_{CC} = Max (2)			80	120		15	19	mA
C_O	Off-State Output Capacitance	V_{CC} = 5 V, V_O = 2.0 V, f = 1 MHz			6			N/A		pF

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		Condition	DM54/74 89			Conditions	DM54/74L L89A			Units
			Min	Typ	Max		Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Memory Enable	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω		23	35	C_L = 50 pF, R_L = 4 kΩ		64	90	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Memory Enable			23	35			33	60	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Select			34	50			90	150	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Select			35	50			78	150	ns
t_{SR}	Sense Recovery Time After Writing			35	50			110	165	ns
t_W	Width of Write-Enable Pulse		40				50			ns
t_{SETUP}	Setup Time, Data Input With Respect to Write Enable		0				0			ns
t_{SETUP}	Select Input Setup Time With Respect to Write Enable		0				0			ns
t_{HOLD}	Hold Time, Data Input With Respect to Write Enable		0				0			ns
t_{HOLD}	Select Input Hold Time After Writing		5				0			ns

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