MJE13007
MJF13007

Designer's Data Sheet

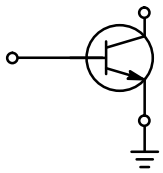
SWITCHMODE™

NPN Bipolar Power Transistor For Switching Power Supply Applications

POWER TRANSISTOR
8.0 AMPERES
400 VOLTS
80/40 WATTS

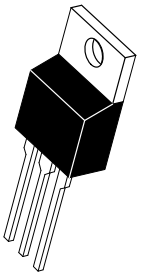
The MJE/MJF13007 is designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF13007 is UL Recognized to 3500 V_{RMS}, File #E69369



MAXIMUM RATINGS

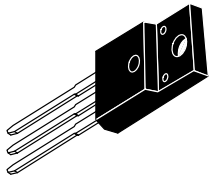
Rating	Symbol	MJE13007	MJF13007	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24		Adc
RMS Isolation Voltage (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Fig. 15 Test No. 2 Per Fig. 16 Test No. 3 Per Fig. 17 Proper strike and creepage distance must be provided	V_{ISOL}	 — — —	 4500 3500 1500	V
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	40* 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C



CASE 221A–06
TO–220AB
MJE13007

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.56 62.5	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C



CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED
MJF13007

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
*Measurement made with thermocouple contacting the bottom insulated mountign surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**							
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)			$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current			I_{CES}				mAdc
(V_{CES} = 700 Vdc)				—	—	0.1	
(V_{CES} = 700 Vdc, T_C = 125°C)				—	—	1.0	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)			I_{EBO}	—	—	100	μAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased			—	See Figure 7			
***ON CHARACTERISTICS**							
DC Current Gain			h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)				8.0	—	40	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)				5.0	—	30	
Collector–Emitter Saturation Voltage			$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	2.0	
(I_C = 8.0 Adc, I_B = 2.0 Adc)				—	—	3.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	3.0	
Base–Emitter Saturation Voltage			$V_{BE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.2	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	1.5	
DYNAMIC CHARACTERISTICS							
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)			f_T	4.0	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			C_{ob}	—	80	—	pF
Collector to Heatsink Capacitance, MJF13007			$C_{c–hs}$	—	3.0	—	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(V_{CC} = 125 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 25 μs, Duty Cycle ≤ 1.0%)		t_d	—	0.025	0.1	μs
Rise Time			t_r	—	0.5	1.5	
Storage Time			t_s	—	1.8	3.0	
Fall Time			t_f	—	0.23	0.7	
Inductive Load, Clamped (Table 1)							
Voltage Storage Time	V_{CC} = 15 Vdc, I_C = 5.0 A, V_{clamp} = 300 Vdc	T_C = 25°C	t_{sv}	—	1.2	2.0	μs
		T_C = 100°C		—	1.6	3.0	
Crossover Time	$I_{B(on)}$ = 1.0 A, $I_{B(off)}$ = 2.5 A, L_C = 200 μH	T_C = 25°C	t_c	—	0.15	0.30	μs
		T_C = 100°C		—	0.21	0.50	
Fall Time		T_C = 25°C	t_{fi}	—	0.04	0.12	μs
		T_C = 100°C		—	0.10	0.20	

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

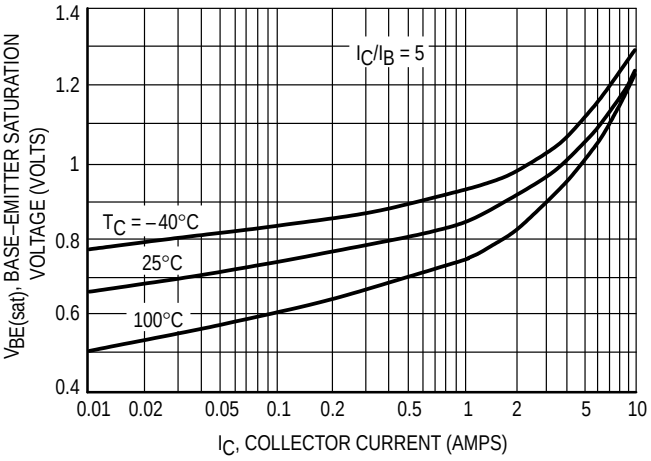


Figure 1. Base–Emitter Saturation Voltage

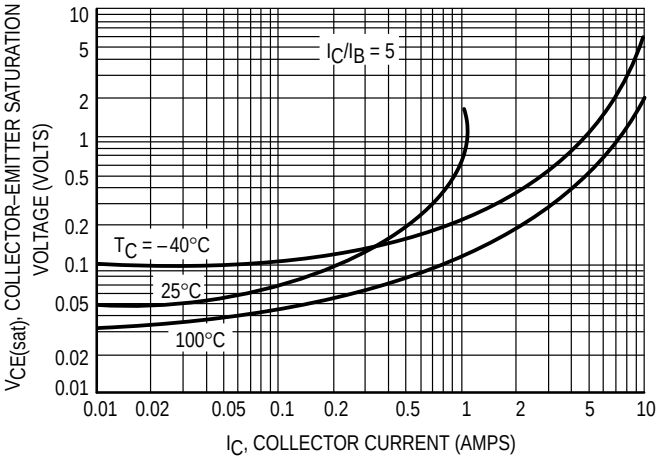


Figure 2. Collector–Emitter Saturation Voltage

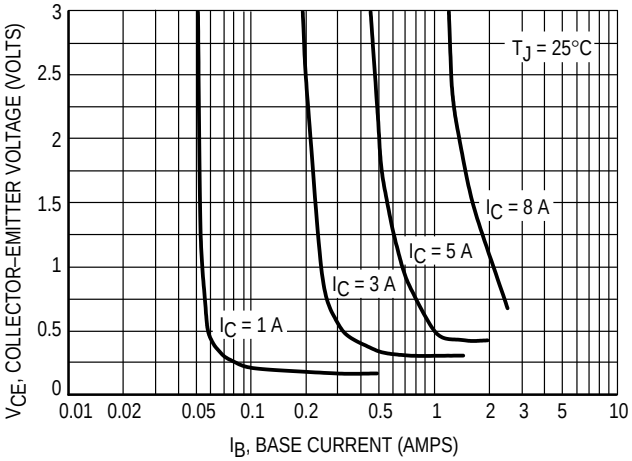


Figure 3. Collector Saturation Region

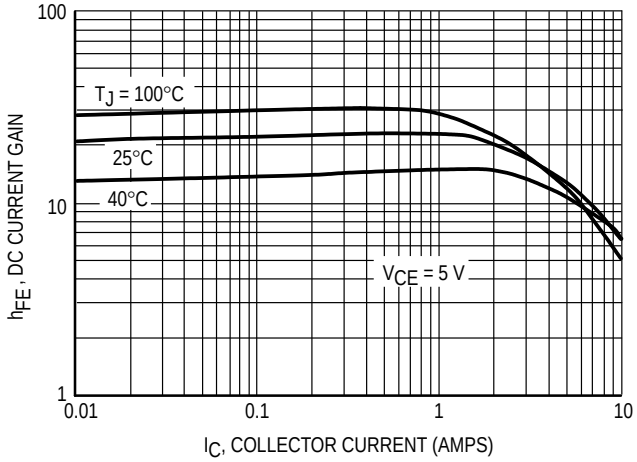


Figure 4. DC Current Gain

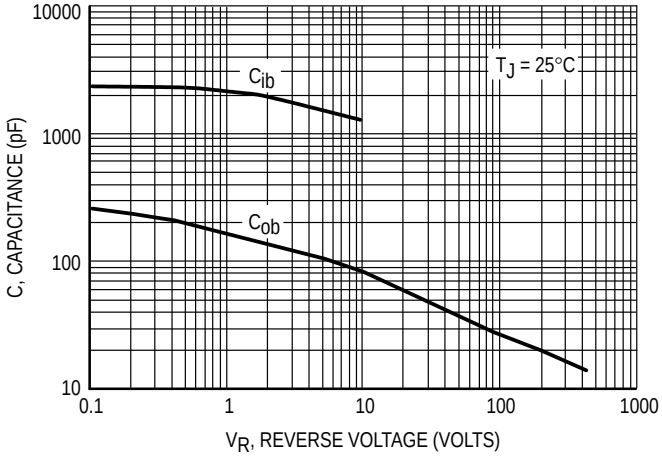


Figure 5. Capacitance

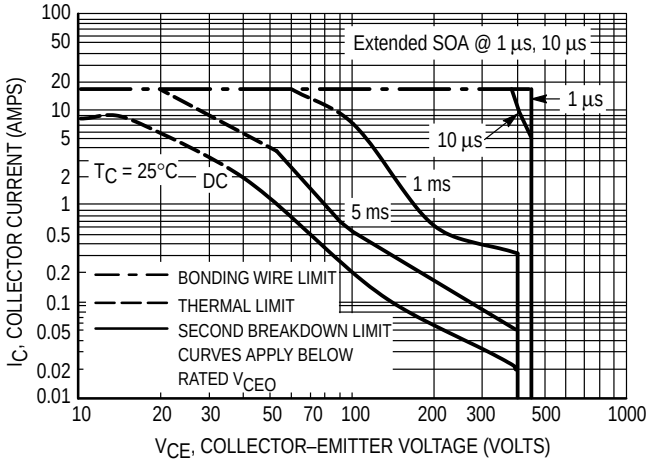


Figure 6. Maximum Forward Bias Safe Operating Area

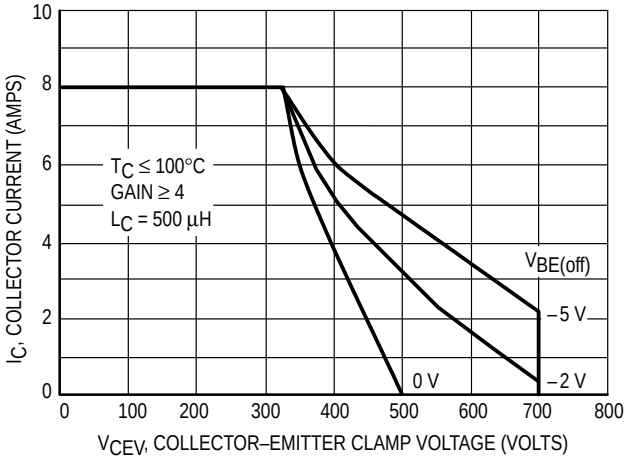


Figure 7. Maximum Reverse Bias Switching Safe Operating Area

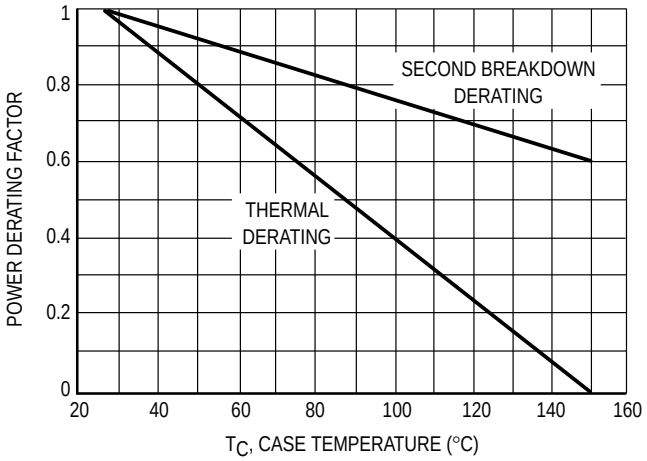


Figure 8. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 8.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 7) is discussed in the applications information section.

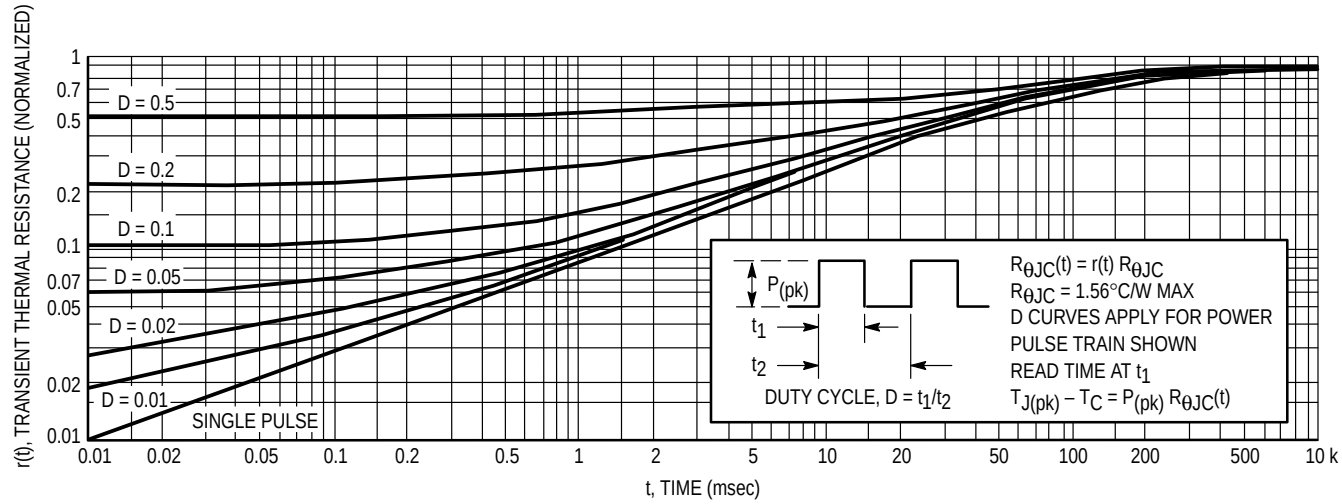


Figure 9. Typical Thermal Response for MJE13007

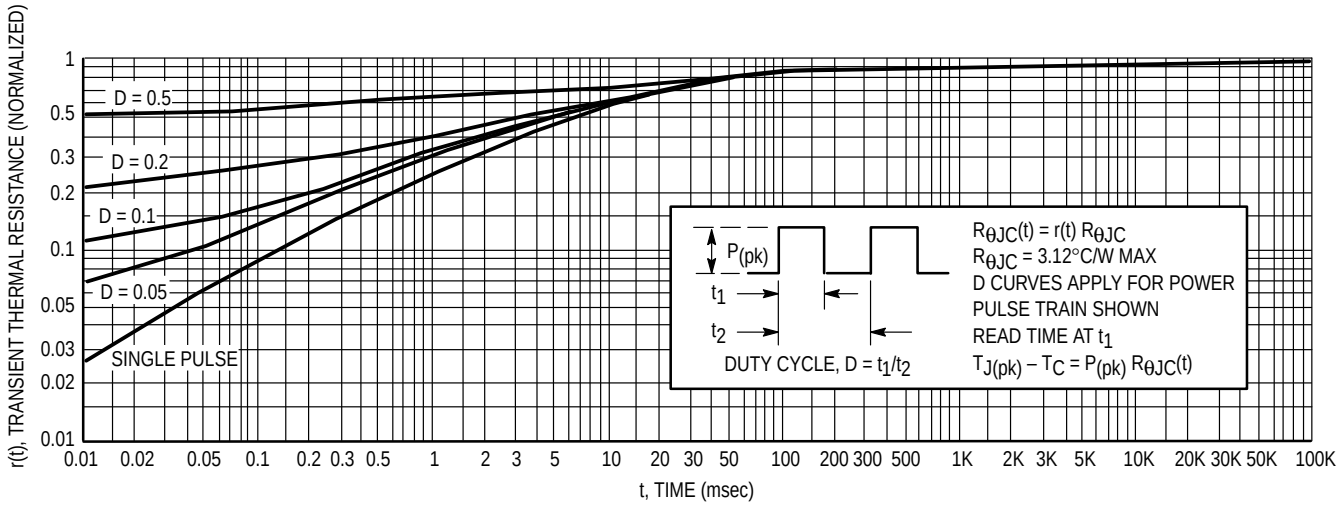


Figure 10. Typical Thermal Response for MJF13007

SPECIFICATION INFORMATION FOR SWITCHMODE APPLICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

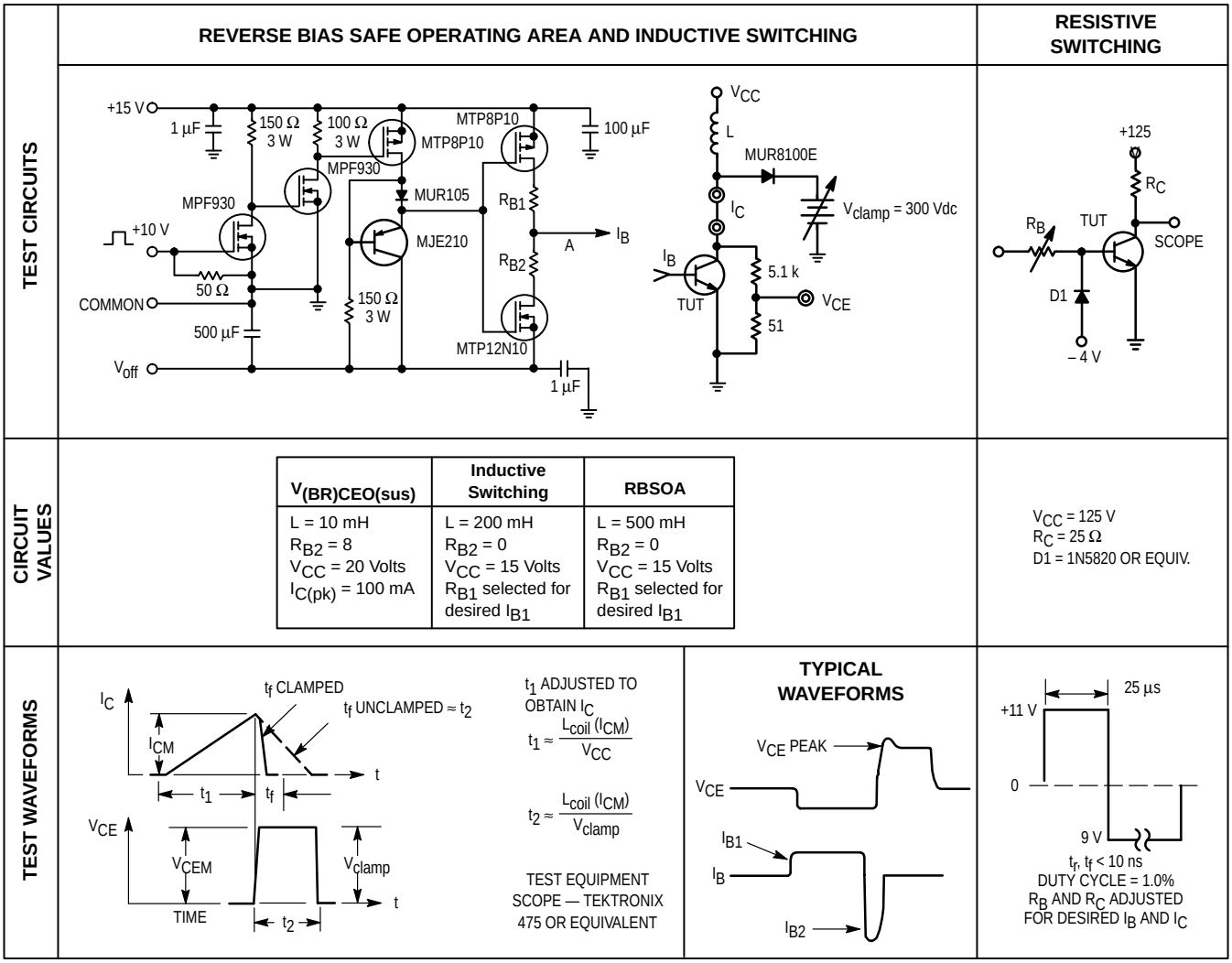
Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn–on and turn–off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn–on and the pulsed forward bias SOA curves (Figure 6) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 7) which represents voltage–current conditions that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

(1) For detailed information on specific switching applications, see Motorola Application Note AN719, AN873, AN875, AN951.

Table 1. Test Conditions For Dynamic Performance



VOLTAGE REQUIREMENTS (continued)

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn–off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn–on and within the reverse bias SOA curve during turn–off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn–on time does not exceed 10 µs (see standard pulsed forward SOA curves in Figure 6).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 7).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5.0 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base–emitter junction during turn–off. The reverse biased switching characteristics for inductive loads are shown in Figures 13 and 14 and resistive loads in Figures 11 and 12. Usually the inductive load components will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (see Table 1) providing correlation between test procedures and actual use conditions.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and any coil driver, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn–off waveforms is shown in Figure 13 to aid in the visual identity of these terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching times are shown in Figure 14. In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

SWITCHING PERFORMANCE

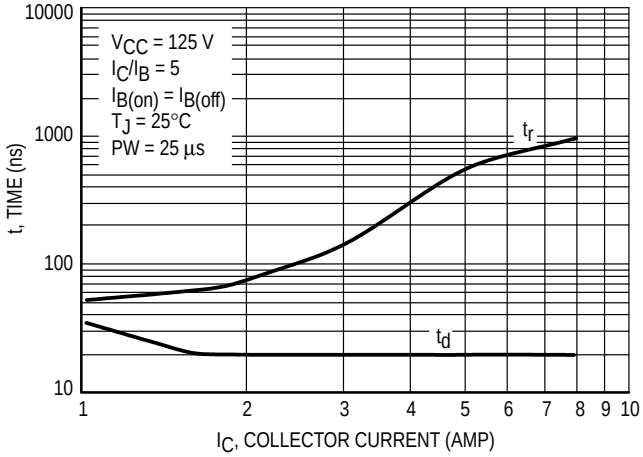


Figure 11. Turn–On Time (Resistive Load)

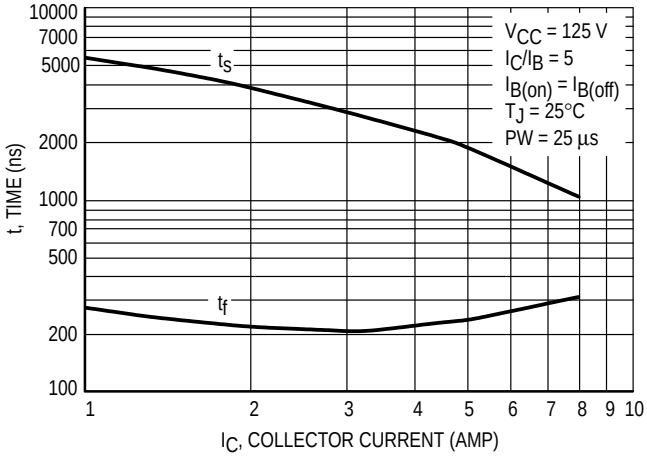


Figure 12. Turn–Off Time (Resistive Load)

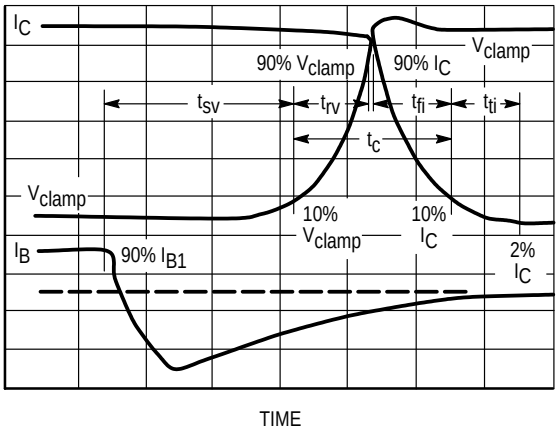


Figure 13. Inductive Switching Measurements

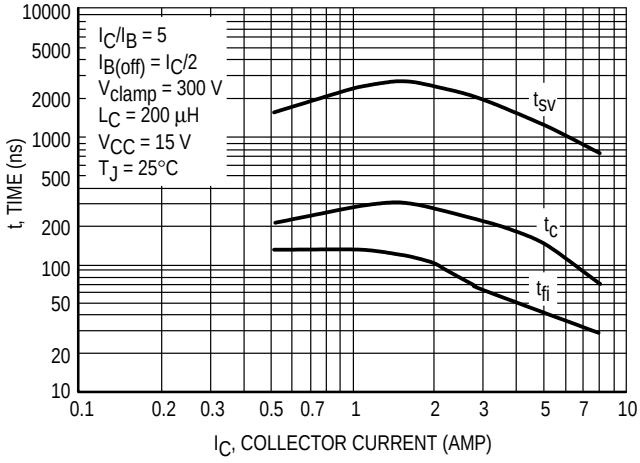
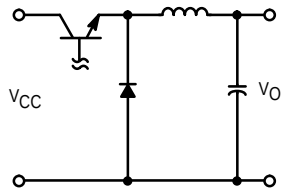
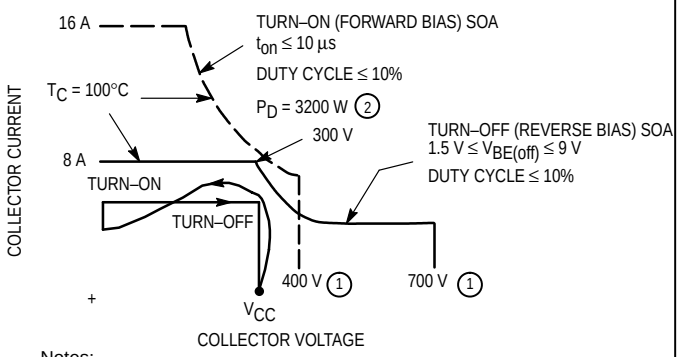
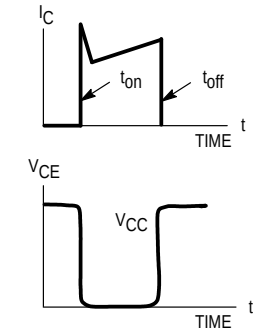
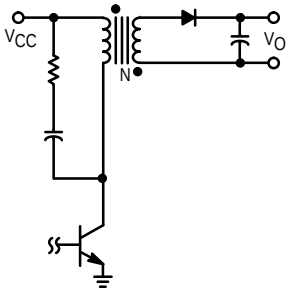
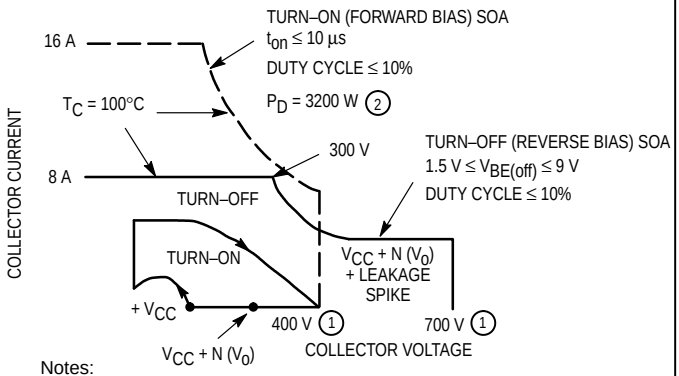
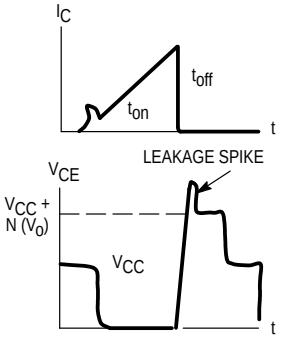
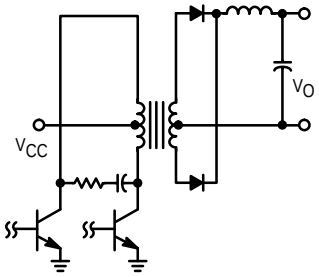
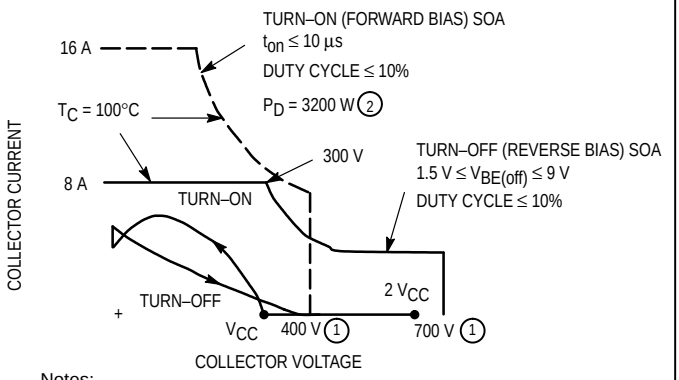
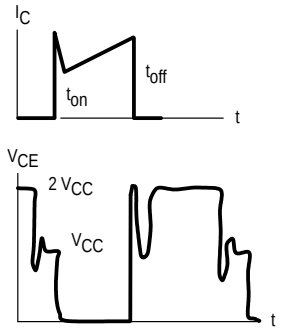
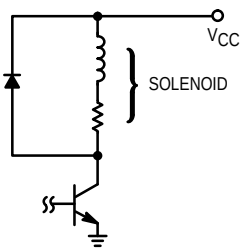
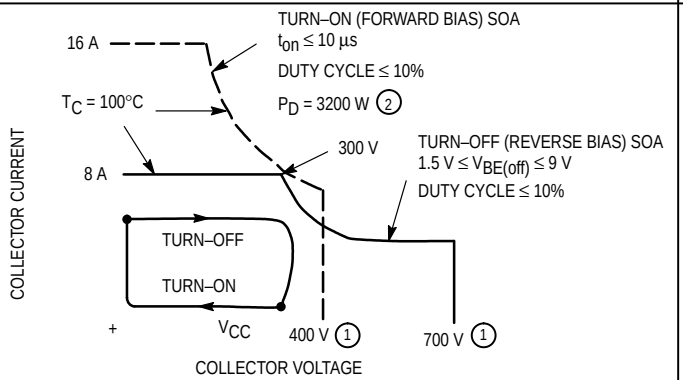
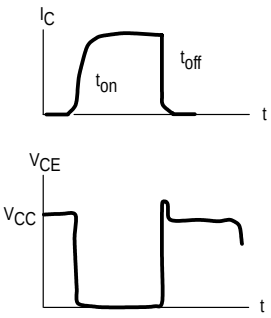


Figure 14. Typical Inductive Switching Times

Table 2. Applications Examples of Switching Circuits

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
B	**FLYBACK INVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
C	**PUSH–PULL INVERTER/CONVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	

TEST CONDITIONS FOR ISOLATION TESTS*

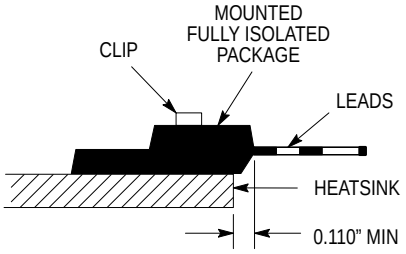


Figure 15. Screw or Clip Mounting Position for Isolation Test Number 1

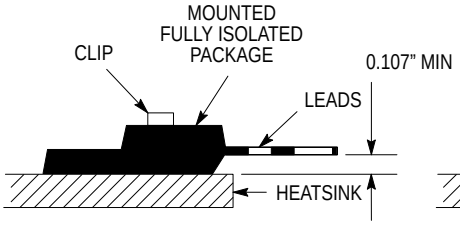


Figure 16. Clip Mounting Position for Isolation Test Number 2

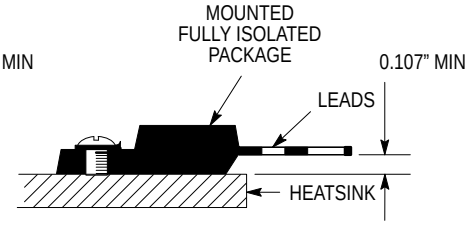
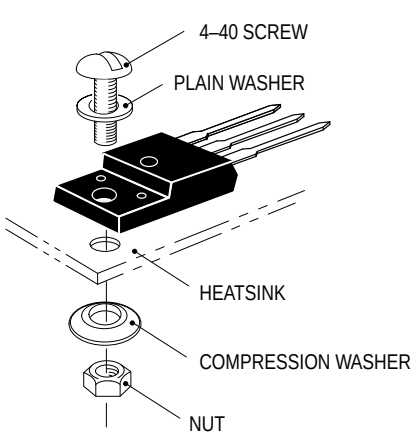


Figure 17. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION



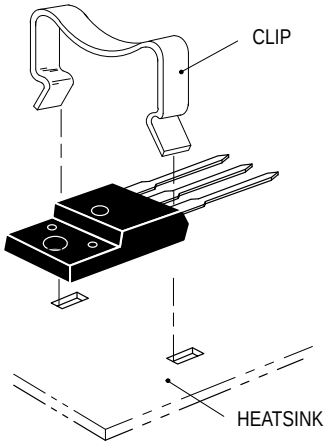


Figure 18. Typical Mounting Techniques for Isolated Package

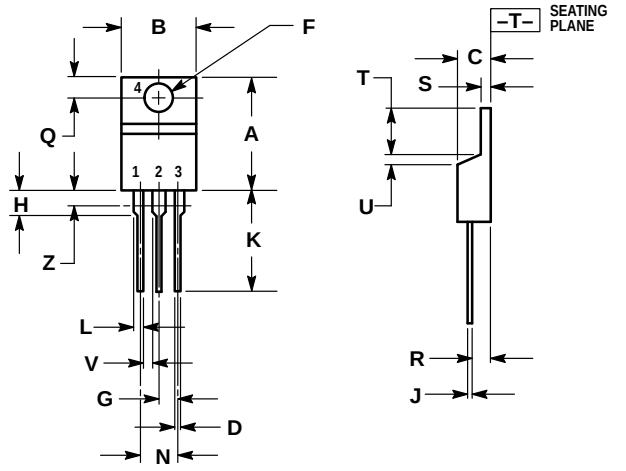
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

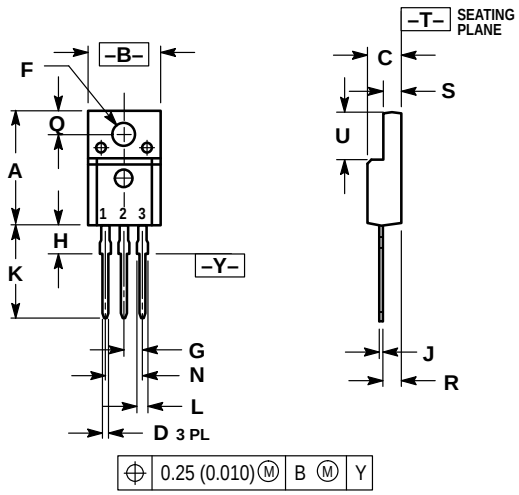


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 221D–02
ISOLATED TO–220 TYPE
ISSUE D

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