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**Introduction**

Zarlink Semiconductor manufactures a wide variety of components oriented towards microprocessor applications. Obviously, there are many different microprocessors, and many different bus architectures. This abundance of unique designs makes it difficult to interface a component directly to more than one type of microprocessor without running into complications for at least one type. The purpose of this application note is to provide an overview of what CPU buses Zarlink devices can interface to, and provide some ideas and examples on interfacing Zarlink components to various microprocessors.

The intent of the examples is to categorize interface architectures and microprocessor types, in order to help designers incorporate Zarlink components in their systems. The microprocessors for which some interfacing examples have been created are:

- |              |                    |
|--------------|--------------------|
| a/ The 68000 | g/ The 8085        |
| b/ The 68010 | h/ The Z80/Z8400   |
| c/ The 68008 | i/ The 8086        |
| d/ The 6809  | j/ The 8088        |
| e/ The 6802  | k/ The Z8002/Z280  |
| f/ The 6800  | l/ The 8051/68HC11 |

Zarlink Component	CPU					CPU				
	Non-Multiplexed Bus Structure					Multiplexed Bus Structure				
	6800	6802	6809	68302 68000 68008/10	Z-80 Z-8400	8085	8086/8	Z-8002 Z-280	8051	68HC11
MT8930, MT8992/3/4/5						✓	✓	✓	✓	✓
MT8880	✓	✓	✓	✓						
MT8888						✓	✓	✓	✓	
MT8889	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MT8980/1	✓	✓	✓							
MT8985, MT8986 (DIP-40)	✓	✓	✓	✓						
MT8986 (PLCC-44)	✓	✓	✓	✓		✓	✓	✓	✓	✓
MT8920B	✓	✓	✓	✓						
MT8952B	✓	✓	✓	✓						

**Table 1. Bus Compatibility between Zarlink Components and Some Popular CPUs**

Mitel Component	CPU					CPU				
	Non-Multiplexed Bus Structure					Multiplexed Bus Structure				
	6800	6802	6809	68302 68000 68008/10	Z-80 Z-8400	8085	8086/8	Z-8002 Z-280	8051	68HC11
MT8930, MT8992/3/4/5	-	2	2	2	-	-	-	10	-	-
MT8880	4	2	3	5	-	-	-	-	-	-
MT8888	-	-	-	-	9	7	7	-	7	-
MT8889	4	2	3	5	9	7	7	10	7	7
MT8980/1	13	11	12	-	-	-	-	17	-	-
MT8985, MT8986 (DIP-40)	13	11	12	14	16	15	15	17	*	-
MT8986 (PLCC-44)	13	11	12	14	16	15	15	-	*	-
MT8920B	20	18	19	21	23	22	24	25	-	-
MT8952B	2	2	3	5	9	6	8	10	6	6

\*See MT8986 data sheet

**Table 2. Cross Reference Interfacing Examples between Zarlink Components & Parallel Microprocessors**

Grouping Zarlink's components on the basis of similar interfacing requirements minimizes the total number of interface circuits. Zarlink devices with some specific bus operation are grouped as follows:

*Group 1*

- a/ MT8952B HDLC Controller
- b/ MT8880/8/9 DTMF Transceivers
- c/ MT8992/3 Phone Chips & MT8930/1 Transceivers

*Group 2*

- a/ MT8980/1 Digital Switches
- b/ MT8985/6 Digital Switches

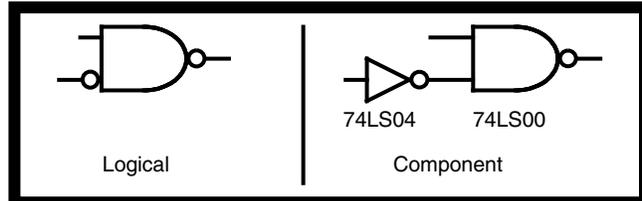
*Group 3*

- a/ MT8920B ST-BUS Parallel Access Device (STPA)

Table 1 is a cross reference of CPU bus compatibility between Zarlink components and some microprocessors. Bus compatibility means that a connection between the peripheral and the CPU can be done without conversion in the parallel data and address format.

In Table 1, the check-mark (✓) means that the component parallel data/address bus can be connected directly to the CPU described since it provides the appropriate multiplexed or non-multiplexed bus compatibility. Table 2 is a reference of the connection examples given in this application note. The contents of Table 2 represent the figure number of the examples between the corresponding CPU (column) and the Zarlink component (row).

To keep the interfaces independent of a particular system, as few actual "glue" components as possible



**Figure 1 - Logical Implementation vs. Component Implementation**

will be shown in the diagrams. Instead of showing commercially available components, only the logical symbol representing the desired operation shall be shown. This will leave the actual implementation to the designer (see Figure 1).

**1.0 Group 1 Components**

A basic feature of Group 1 components is that there is a requirement for the devices to interrupt the CPU. The device's remaining requirements for CPU data transfer and controlling procedures are common to the majority of the peripherals. Some of the Group 1 components provide a non-multiplexed bus structure (MT8952B and MT8880/9) while others provide only a multiplexed type of bus interface (MT8930/1, MT8888 and MT8992/3). This section will cover some issues on interconnection for both types of buses.

**Non-Multiplexed Bus**

The parallel bus interface for Group 1 components with a non-multiplexed structure is basically composed of:

- a/ a 4 or 8-bit bidirectional data port,

- b/ one or several inputs used for selecting internal registers (register selects),
- c/ chip select input(s),
- d/ a read/write control that specifies the direction of data flow (to or from the component),
- e/ an enable strobe that synchronizes component timing to the microprocessor's timing,
- f/ an interrupt output that is used to alert the microprocessor that a specific event has occurred at the component.

The signals described above are compatible to the majority of Motorola's non-multiplexed bus CPUs. Zarlink's MT8952B and MT8880C are the only two components in Group 1 that directly interface to Motorola's non-multiplexed bus structure. When interfacing to the 6802/09, 6800, and 68000, the circuit design is identical for both the MT8880C and the MT8952B.

Sections 1.1. to 1.4 shows examples of these connections.

### Multiplexed Bus

Many of the Group 1 components were developed to comply with multiplexed bus structure. This parallel bus usually complies with both Intel and Motorola CPU signal formats.

The parallel bus interface for Group 1 components with Intel multiplexed bus structure is composed of:

- a/ an 8-bit bidirectional data/address port,
- b/ chip select input,
- c/ separate read ( $\overline{RD}$ ) and write ( $\overline{WR}$ ) signals that specify the direction of data flow,
- d/ an address latch enable input to allow the internal demultiplexing between the data and address lines,
- e/ an interrupt output that is used to alert the microprocessor that a specific event has occurred at the component.

For Motorola multiplexed bus interface, the control signals are similar to Intel bus described above with two exceptions; the Read and Write signals are combined into one single input ( $R/\overline{W}$ ) and an

additional data strobe input (DS), is provided to synchronize the data transfer.

To facilitate the back-to-back connection between Zarlink DTMF transceivers and the majority of CPUs, Zarlink Semiconductor has introduced the MT8888 and MT8889 devices. These devices provide an enhanced CPU interface port to allow normal operation with different bus structures. The MT8888 is designed to suit the Intel type of backplane, including multiplexed bus architecture. The MT8889 provides an adaptive microport that operates with Motorola/Intel CPUs in both multiplexed and non-multiplexed bus architectures. In the MT8889, the identification of the connected CPU is done automatically without the need for programming. See the MT8889 data sheet for more details on CPU bus recognition procedures.

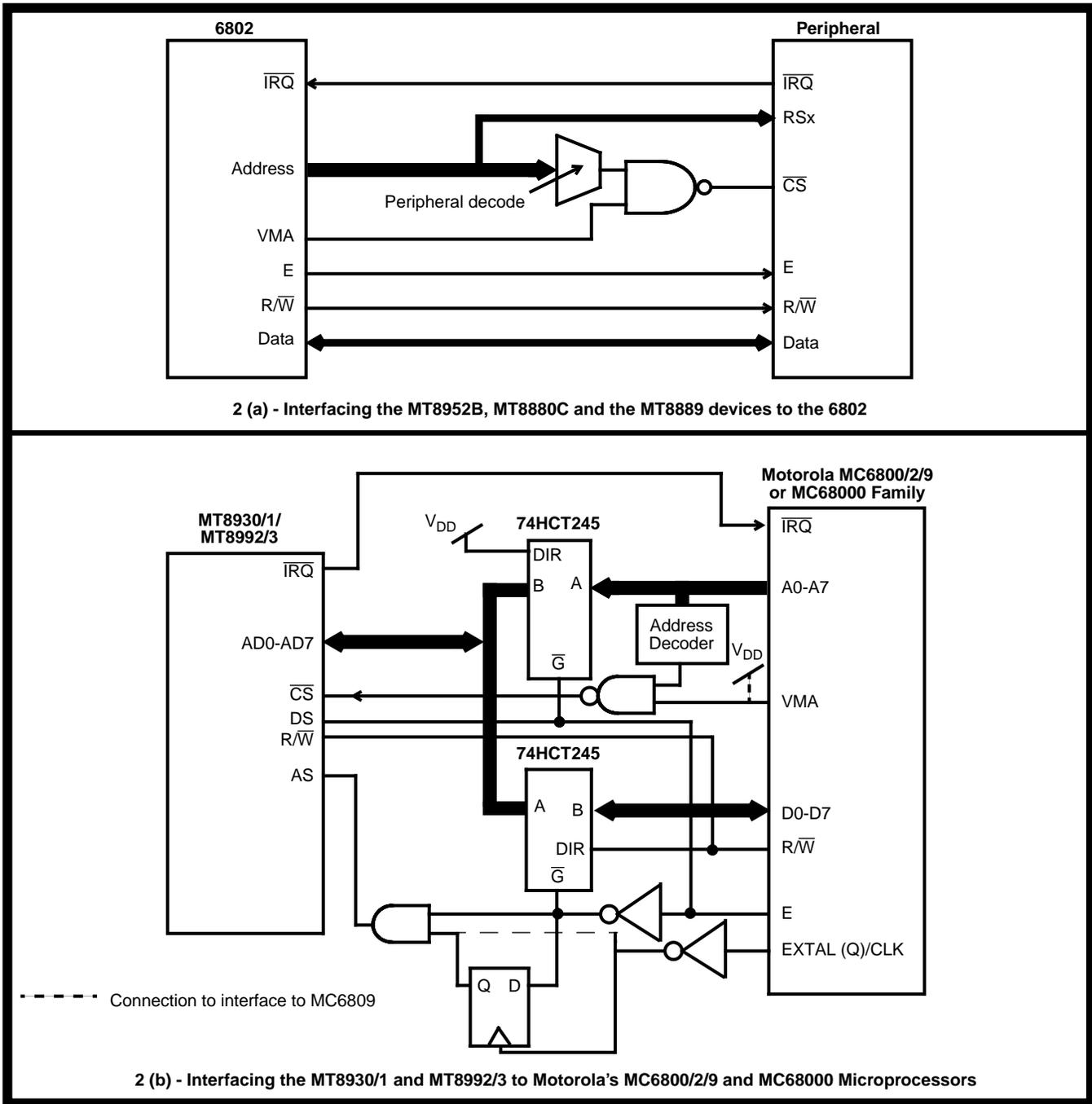
For Zarlink's MT8930 and MT8992/3 devices, the parallel microport is compatible to Motorola/Intel multiplexed bus architectures. As in the MT8889, the identification between Motorola or Intel signals is performed automatically by the device without user intervention (see the MT8930, MT8992/3 data sheets for details).

### 1.1 Interfacing to the 6802

Interfacing Group 1 components like the MT8952 and MT8880C family to the 6802 is the simplest interfacing task.

The 6802's signals relate to Group 1 signals almost directly. The address bus of the microprocessor must be decoded to produce the chip select(s) needed by a component before it will participate actively on the data bus. In a decode of the address bus, the validity of the address bus state must be qualified by the VMA (Valid Memory Address) signal. Any of the address bits may be connected directly to the register select inputs of the component (the least significant bits are the bits most commonly used).

When the chip select is active, and the enable signal is active, the data bus will be carrying either information from the microprocessor, or information from the component. The source of the information is dependent on the state of the  $R/\overline{W}$  signal from the 6802. If the  $R/\overline{W}$  is high (read), the component will turn on its data bus drivers and the contents of the selected register will be transferred to the data bus. If the  $R/\overline{W}$  signal is low (write), the device's data port will be high impedance and the microprocessor will transfer information to the data bus. The bus cycle is terminated by the falling edge of the E clock (strobe is a more appropriate term). When a write bus cycle is ended, the component will latch the state of the



**Figure 2 - Interfacing Group 1 Components**

data bus into the selected register. When a read bus cycle is ended, the component holds the data bus in the same state for a short period of time (hold time) before relinquishing control of the bus. Note that some of the components “acquire” the data from the bus on the rising edge of E. The appropriate set up time before this rising edge must be observed. Set up time is applicable to control signals, data and address information.

The interrupt output of Group 1 devices is an open drain configuration (analogous to open collector in TTL devices), therefore it must be pulled up to  $V_{CC}$  by a resistor. This output can be connected directly

to the 6802 or to a priority encoder, which is then connected to the 6802. Group 1 components signify the presence of an interrupt condition by pulling this line low. The microprocessor must clear this interrupt through an established procedure that is dependent on the type of component that initiated the interrupt. The resistor used to pull up any open drain outputs is not shown any of the diagrams in this note.

Figure 2a shows the connection of data bus as a straight connection; in reality, there will probably be a buffer intervening to give the microprocessor more driving capability.  $R/\bar{W}$  and E are also shown to be a straight connection. These signals are also usually

buffered. In further figures, details such as buffers will be omitted as they are dependent on the design of the target system.

The address bits are shown connected to a box labelled "peripheral decode". This can refer to any circuitry that produces an active high signal when the correct address is on the bus.

For Group 1 components with a multiplexed CPU bus only, like the MT8930/1 and MT8992/3 devices, a multiplexing logic (from the peripheral to the CPU) has to be built between the 6802 and the mentioned devices. Figure 2b gives an idea of how to implement this logic. The same concept can be applied to the other CPUs with a non-multiplexed bus architecture.

### 1.2 Interfacing to the 6809

The circuit needed to interface the 6809 to Group 1 devices with a non-multiplexed bus type structure (Figure 3) is almost the same as the circuit used to

interface to the 6802, due to the similarity between the two microprocessors' bus architectures. The only difference between the two circuits is that the 6809 does not have a VMA signal, so an equivalent signal must be generated by 'OR'ing the E and the Q signals of the 6809.

For the MT8930/1 and MT8992/3 devices, the same idea shown in Figure 2b can be employed to demultiplex the data and address lines.

### 1.3 Interfacing to the 6800

Interfacing the 6800 to Group 1 devices with a non-multiplexed bus type structure requires the same circuit used for interfacing Group 1 components to the 6802. The only difference between the circuits is that in Figure 4 the 6875 clock generator IC is shown connected to the 6800.

For connection of the 6800 to the MT8930/1 and MT8992/3, see Figure 2b.

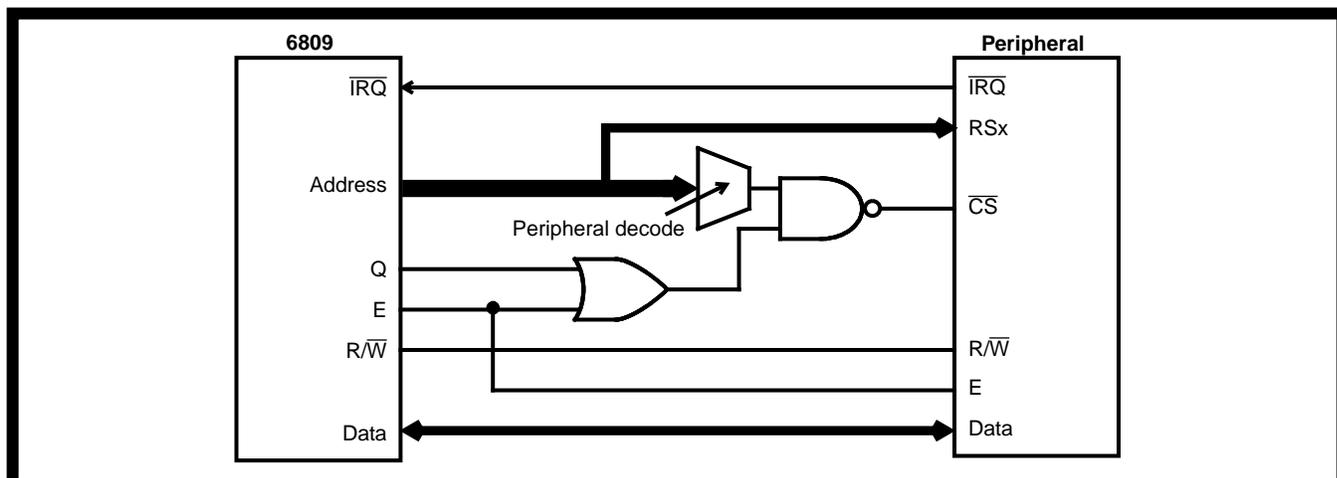


Figure 3 - Interfacing the MT8952B, MT8880C and the MT8889 to the 6809

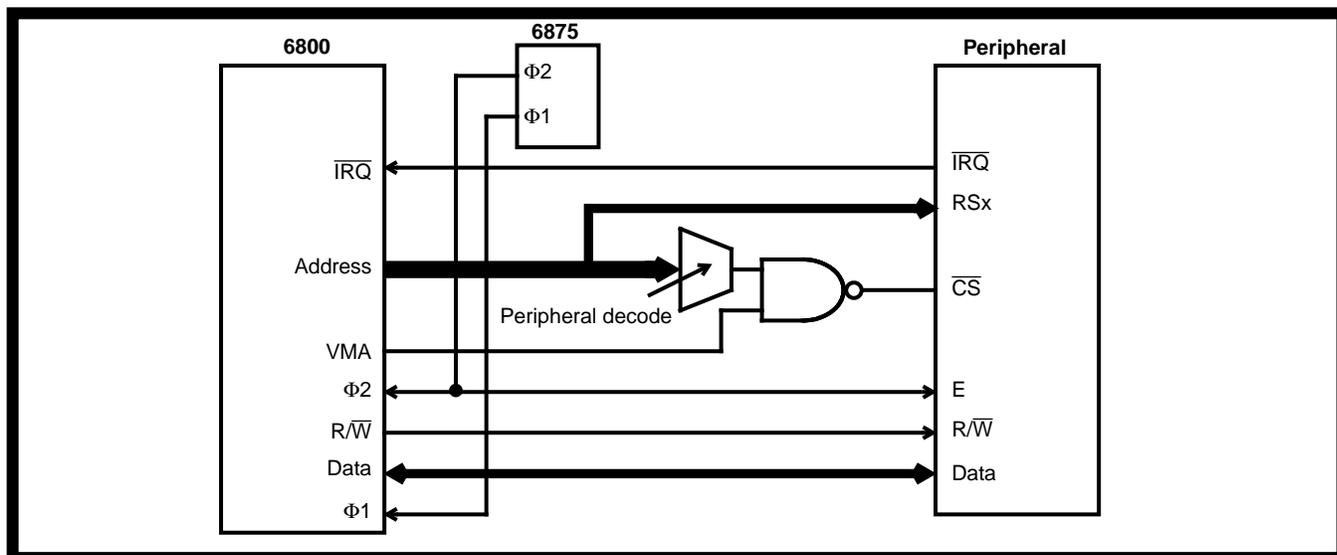


Figure 4 - Interfacing the MT8952B, MT8880C and the MT8889 to the 6800

1.4 Interfacing to the 68000/10/08

Motorola's 68000 16 bit microprocessor takes advantage of the broad line of interfaces designed around its 8 bit microprocessors. Normally, information transferral between the 68000 and a peripheral is performed asynchronously, as opposed to the synchronous method used by the 8 bit microprocessors (6800, 6802, 6809, etc.). The 68000, however, can be forced to perform a synchronous transfer.

Synchronous transfers are achieved by referencing all bus events to the edges of the E strobe. Asynchronous transfers involve a handshake between the 68000 and the component involved in the data transfer. When the 68000 wants to read or write to a device, the 68000 asserts  $\overline{\text{LDS}}$  or  $\overline{\text{UDS}}$  ( $\overline{\text{DS}}$  in the 68008) and when the component has accepted the data (write) or has put valid data on the data bus (read), the component asserts an open drain signal called  $\overline{\text{DTACK}}$  (Data Acknowledge). This signal causes the 68000 to end the bus cycle by removing the data strobe signal. Following  $\overline{\text{DS}}$  negation, a read latches data into the microprocessor, the peripheral releases the data bus and negates  $\overline{\text{DTACK}}$ . If a write, the data is latched into the peripheral and it then negates  $\overline{\text{DTACK}}$ .

Motorola designed a mechanism to accommodate peripherals that do not have the capability to perform an asynchronous transfer with the 68000. The 68000 supplies an E clock, a  $\overline{\text{VMA}}$  signal and has an input called  $\overline{\text{VPA}}$ . If an address supplied by the 68000

(qualified by  $\overline{\text{AS}}$ ) causes the  $\overline{\text{VPA}}$  signal to be asserted, the 68000 synchronizes the data transfer to the E clock (see 68000 data sheet for timing details).

To synchronize, the 68000 waits for the E clock to go low (E clock timing has no relation to normal 68000 bus cycles), then the 68000 asserts  $\overline{\text{VMA}}$  and finishes the bus cycle like an 8-bit microprocessor. The finishing sequence is as follows: E goes high, data is transferred, the bus cycle terminates with E falling,  $\overline{\text{VMA}}$  is negated,  $\overline{\text{AS}}$  and the data strobes are negated).

The 68000's exception handling is very different from the 8-bit processors. Peripherals can take an active role in the determination of the exception vector. Any state on the Interrupt Priority Level inputs ( $\overline{\text{IPL0-2}}$ ), other than all ones (level 0), indicates an interrupt. If an interrupt is indicated, the state of the  $\overline{\text{IPL0-2}}$  inputs codes the level of the interrupt's priority. The information encoded on these inputs is inverted in the 68000 to represent the priority level on the 3 bit interrupt mask in the internal status register.

When the instruction that is being executed at the time of the interrupt is finished, the 68000 performs an interrupt acknowledge cycle. During an interrupt acknowledge cycle, the 20 most significant bits of the address are set high, the three least significant bits reflect the interrupt level, and the FC0-2 pins on the 68000 are all set (the real indicator that an interrupt acknowledge cycle is occurring).  $\overline{\text{AS}}$  is asserted, and then  $\overline{\text{LDS}}$  is asserted (an interrupt vector may only

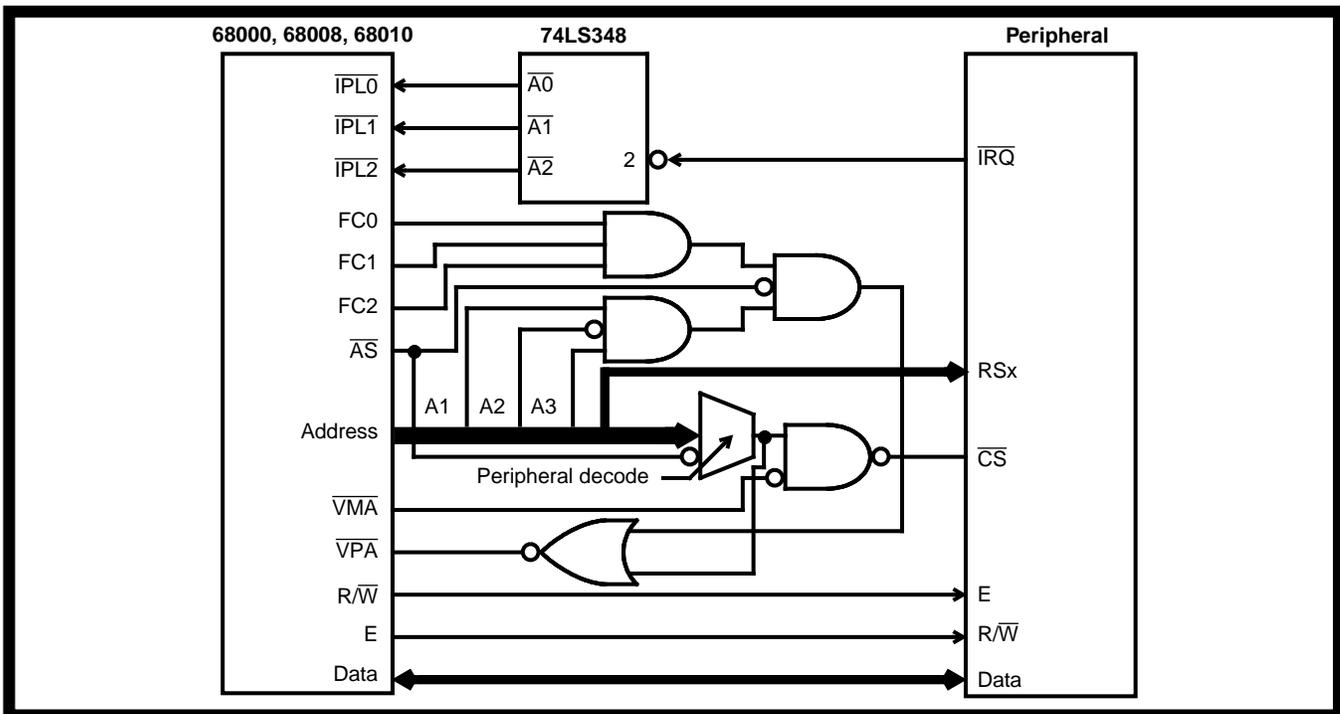


Figure 5 - Interfacing the MT8952B, MT8880C and the MT8889 to the 68000, 68008 and the 68010

be transferred on the lower half of the data bus in the 68000). The  $\overline{R/W}$  pin will be high because the 68000 is expecting the peripheral to place vector information on the data bus, as if the 68000 was reading one of the peripheral's internal registers. A peripheral designed for the 68000 will complete the handshake with the data required and return  $\overline{DTACK}$  just like a normal exchange.

Group 1 components do not have the above facility to provide the 68000 with an interrupt vector, just as they cannot perform an asynchronous transfer. However, Motorola has provided for 6800 peripherals in 68000 exception processing, just as provision was made for data transfers with 6800 peripherals. If the information that the 68000 provides to indicate an interrupt acknowledge cycle and the level of the interrupt can cause  $\overline{VPA}$  to be asserted, the 68000 will automatically fetch an exception vector at an address determined by the level of the interrupt (Motorola calls this auto-vectoring). There are seven autovector locations (7 interrupt priority levels) and they are located at address 000064<sub>H</sub> to 00007C<sub>H</sub>.

The circuit to interface the MT8952B, MT8880C and the MT8889 to the 68000 (Fig. 5) must be able to assert  $\overline{VPA}$  not only when the component is directly addressed, but also when the 68000 is indicating that the component was the source of the interrupt. Fig. 5 shows a block symbol to represent the decode of a group 1 device. The input of this block is the address bus and  $\overline{AS}$ ; the output is a signal that has two destinations: the input to the circuit that asserts  $\overline{VPA}$  and the input to the circuit that asserts the component's chip select.

To select the component for data transfer, the output of the peripheral decode circuitry is further decoded by  $\overline{VMA}$ . To generate  $\overline{VPA}$ , the peripheral decode output is 'NOR'ed with an interrupt acknowledge (IACK) signal. The IACK signal is formed by 'AND'ing the FC0-2 outputs, asserting  $\overline{AS}$ , and placing the correct priority level information on the three least significant address pins. All this information is 'AND'ed to produce IACK. Figure 5 shows a possible interrupt encoding scheme implemented with the  $\overline{IRQ}$  line driving a 74LS348 eight to three encoder. The 74LS348, in turn, drives the  $\overline{IPL}$  inputs (remember that the logic level is inverted to form the internal priority level).

For Group 1 components with a multiplexed bus architecture such as the MT8930/1B and the MT8992/3B, the idea described in Figure 2b can be applied when interconnecting to the 68000 family.

## 1.5 Interfacing to the 8085/6/8, 8051 and Motorola MC68HC11 Series

### 1.5.1 Connecting MT8952B to 8085 and 8051

The circuit in Figure 6a gives an example of a connection between Zarlink's MT8952B and Intel's 8085 or 8051 CPUs.

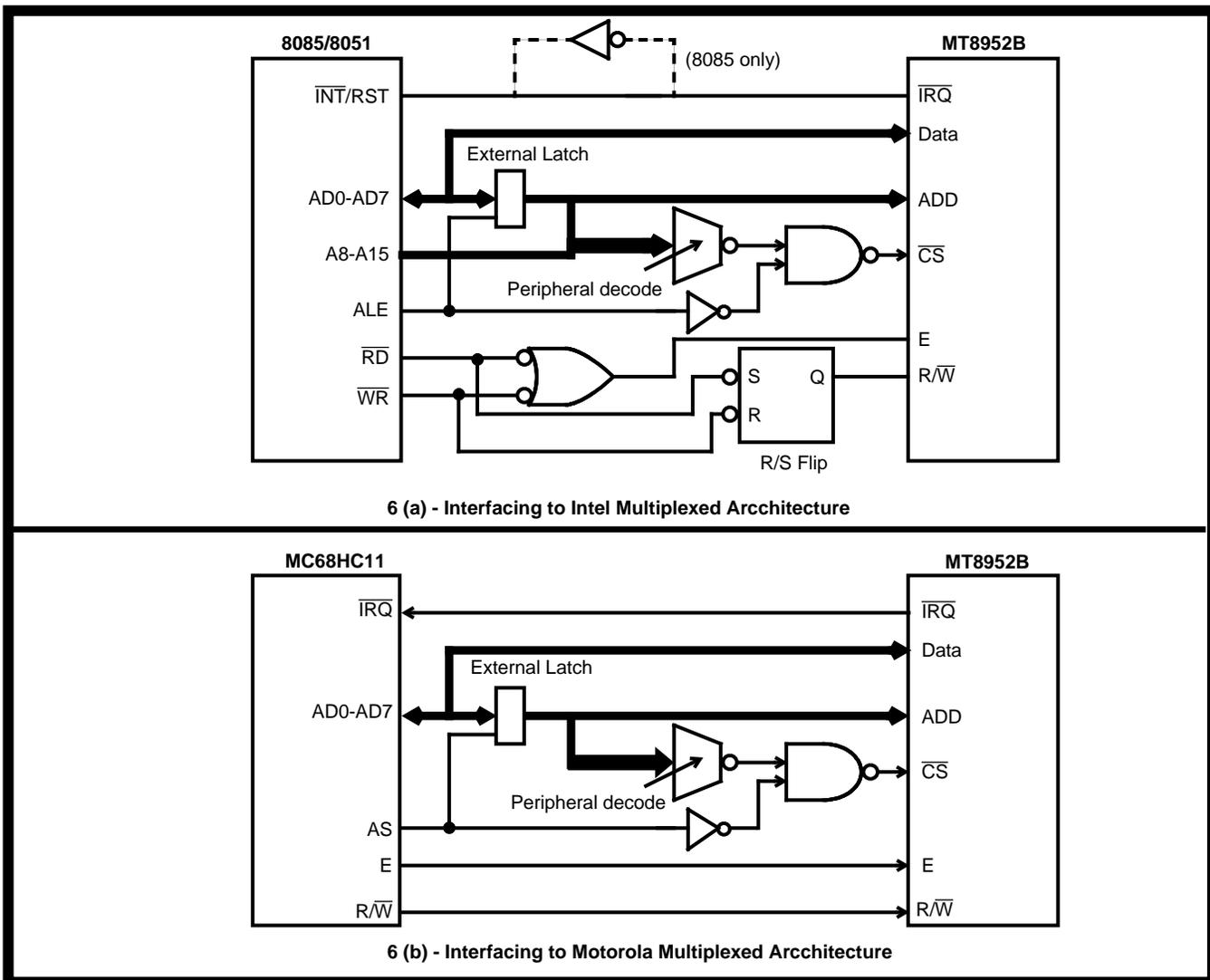
The circuit is different from the interface to Motorola's non-multiplexed 8 bit microprocessors in many respects. The first difference is that the Intel 8085 and 8051 has a multiplexed address/data bus. The first step in decoding an address generated by the CPU is to demultiplex the least significant half of the address from the data. An external latch is required to perform this function. The external latch is strobed by the ALE (Address Latch Enable) signal from the 8085/8051, when the address on the Address/data bus is valid. The demultiplexed address may then be decoded as in the Motorola system. The register select pins may be derived from any of the address bits.

The second difference is that rather than using the combination of a  $\overline{R/W}$  direction pin and an E strobe, the 8085/8051 uses a  $\overline{Read}$  strobe and a  $\overline{Write}$  strobe. When either of these strobes are active, the active period is equivalent to the period in a Motorola bus cycle where the E strobe is active. The direction of the data transfer is determined by which strobe, the  $\overline{RD}$  or the  $\overline{WR}$ , is present. For correct operation with the MT8952,  $\overline{R/W}$  and E must be generated from  $\overline{RD}$  and  $\overline{WR}$ . To generate E,  $\overline{RD}$  and  $\overline{WR}$  are 'NAND'ed together. The generation of the  $\overline{R/W}$  signal is done by driving the Set input and the Reset input of a  $\overline{RS}$  flip flop with  $\overline{RD}$  and  $\overline{WR}$ , respectively. The Q output may be connected directly to  $\overline{R/W}$ .  $\overline{R/W}$  will maintain the same state until the opposite operation occurs, but it will only affect the Group 1 component when the device is selected, and then it will have the correct state with ample set up and hold times. It is important to note that  $\overline{R/W}$  has a minimum set up time with respect to the rising edge of E. This must be accounted for in the circuit design, therefore E may have to be delayed.

The final difference in the 8085/51 circuit is that the interrupt input RST is active high, so the  $\overline{IRQ}$  output of the MT8952B must be inverted.

### 1.5.2 Connecting MT8952 to MC68HC11

For Motorola type of multiplexed CPU buses, such as in the MC68HC11 series, the connection of the MT8952B is simpler due to the CPU control lines being similar to the peripheral control lines. In this



**Figure 6 - Interfacing the MT8952B to the 8085/51 and MC68HC11**

case, the only requirement for the complete connection is the demultiplexing of data and address lines. Figure 6b gives an example of how to connect the MC68HC11 and the MT8952B.

### 1.5.3 Connecting MT8888/9 to 8085/51

Since the MT8888 transceiver was developed to suit the Intel multiplexed CPU bus, its connection to 8085 and 8051 does not require any "glue" circuit. See the MT8888 data sheet for connection diagram.

The MT8889 can be interfaced to the 8085/8051 as illustrated in Figure 7a. Due to its adaptive nature, the CPU port of the MT8889 can also be connected to the Motorola type of multiplexed bus (MC68HC11) as shown in Figure 7b.

### 1.5.4 Connecting MT8952B & MT8889 to 8086/8

For Intel's 8086 and 8088 microprocessors, the circuit to interface the MT8952B and MT8889 with a

Motorola bus is conceptually similar to the one built for Intel's 8085. The 8086/88 has a multiplexed address/data bus (AD0-15 for the 8086 and AD0-8 for the 8088), ALE strobes and  $\overline{RD}$  and  $\overline{WR}$  strobes. Conveniently, there is a signal that can be inverted and connected directly to the R/W inputs of MT8952 and MT8889. This signal is called DT/R (Data Transmit/Receive).

$\overline{BHE}$  (Bus High Enable) is an output used to indicate that information is on the high portion of the data bus (8086 only). This signal is used to qualify chip selects. To generate the E signal in applications where E need not be constant,  $\overline{RD}$  and  $\overline{WR}$  may be 'NAND'ed together. An example of an interface circuit between the MT8952B and 8086/88 is shown in Figure 8. For MT8888 and MT8889 devices, connection to the 8086/88 can be done as per Figure 7a.

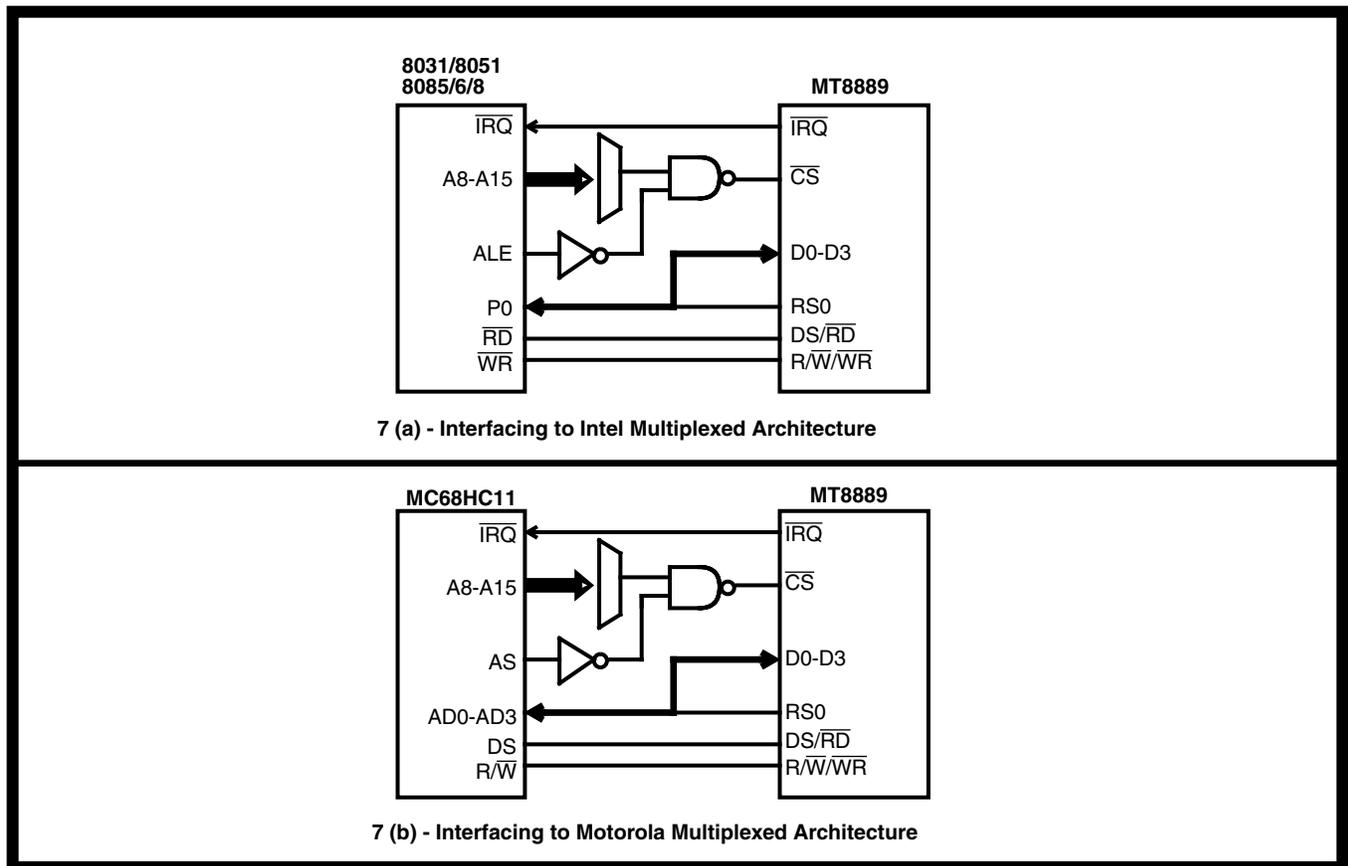


Figure 7 - Interfacing the MT8889 to the 8031/51, 8085/86/88 and MC68HC11

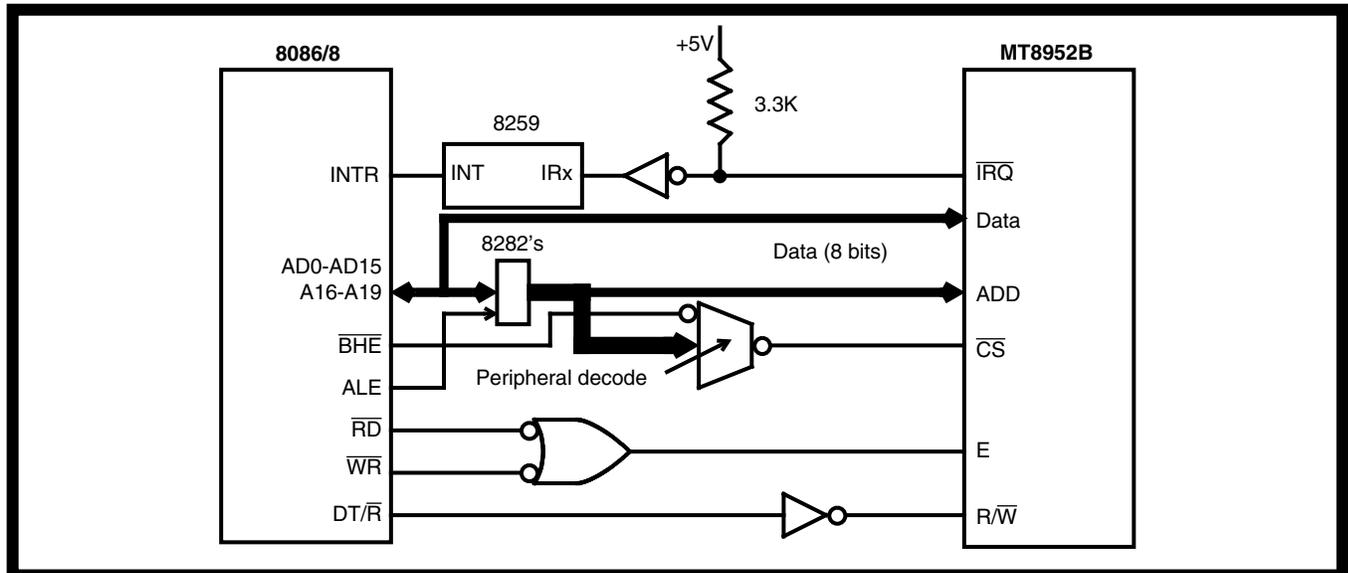


Figure 8 - Interfacing the MT8952B to the 8086/88

1.5.5 Connecting MT8930/1B and MT8992/3B

Since Zarlink's MT8930/1B and MT8992/3B family of devices provides compatibility with both Intel and Motorola multiplexed bus types, the connection of these peripherals to CPUs like Intel's 8085/6/8 and Motorola's 68HC11 families is simple, with no need for an external "glue" circuit. For details on CPU bus operation of these devices, see their respective data sheets.

1.6 Interfacing to the Z80/Z8400

The circuit for interfacing Group 1 components with the Motorola non-multiplexed bus to Z80/Z8400 is shown in Figure 9b. The Z80 must transform a  $\overline{RD}$  strobe and a  $\overline{WR}$  strobe into an E strobe and a  $R/\overline{W}$  signal (recall the set up time for the  $R/\overline{W}$  signal with respect to the E signal). This portion of the circuit is exactly the same as the circuit used for the 8085, i.e., 'NAND'ing  $\overline{RD}$  and  $\overline{WR}$  to form E and the RS flip

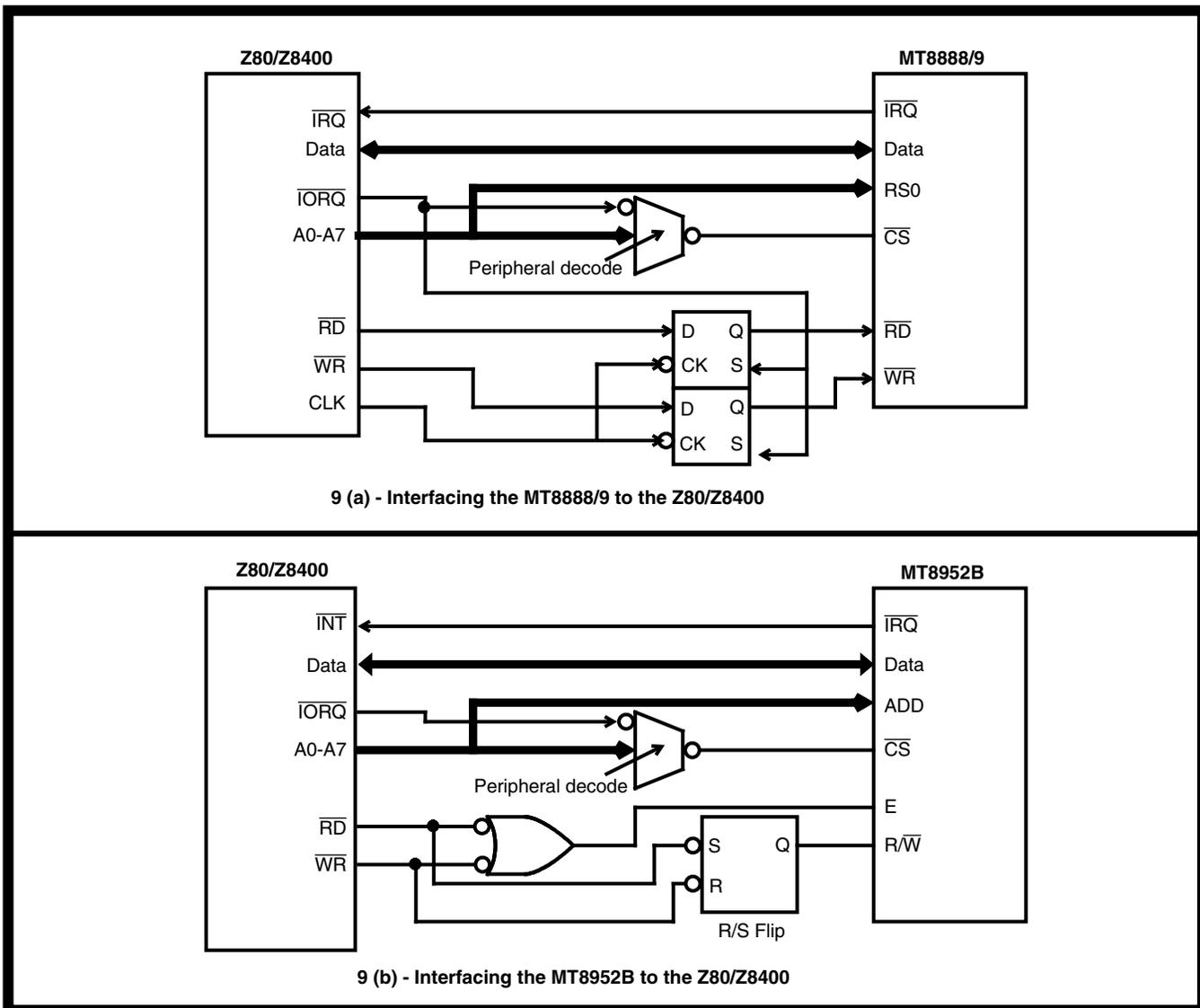


Figure 9 - Interfacing the MT8888/9 and the MT8952B to the Z80/Z8400 Family

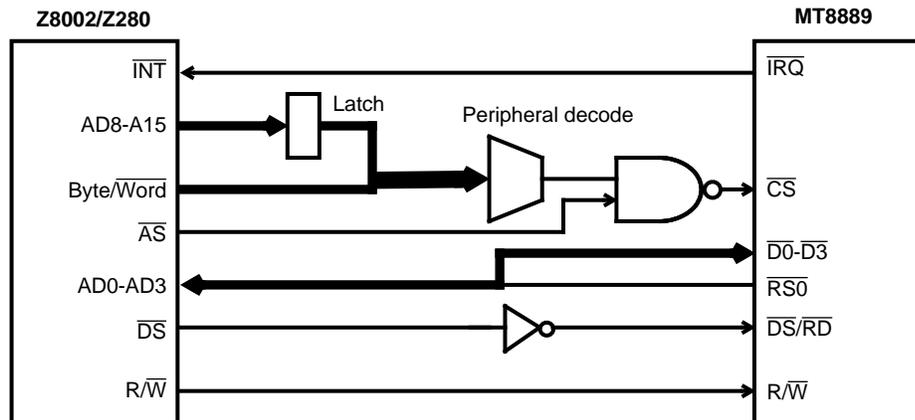
flop used to create  $R/\overline{W}$ . In the Z80/Z8400 circuit the peripheral decode has been arbitrarily chosen to include  $\overline{IORQ}$  (I/O request) active. By doing this, the eight most significant address bits need not be decoded, as an I/O access doesn't allow specification of more than an 8-bit address. Another difference between this circuit and the 8085 circuit is that the address bus of the Z80/Z8400 is not multiplexed so no latch is needed for a portion of the address.  $\overline{INT}$ , the interrupt input does not need an inverter between the Z80/Z8400 and the Group 1 component. Figures 9a and 9b show how the MT8888/9 and the MT8952B can easily be interfaced to the Z80/Z8400 family.

When interfacing Z80/Z8400 to Zarlink's MT8930/1 and MT8992/3 devices, the demultiplexing of the data and address (from the peripheral to the CPU direction) buses has to be implemented between the two devices. A similar example, but for Motorola CPU's, is shown in Figure 2b.

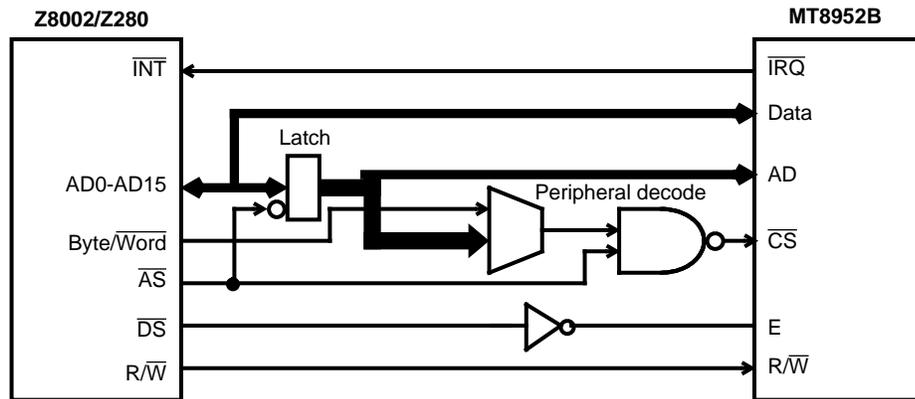
### 1.7 Interfacing to the Z8002/Z280

The circuits for interfacing the Z8002 and Z280 to Group 1 components (see Figure 10) are similar to the circuits for the 8086/88. The differences are:

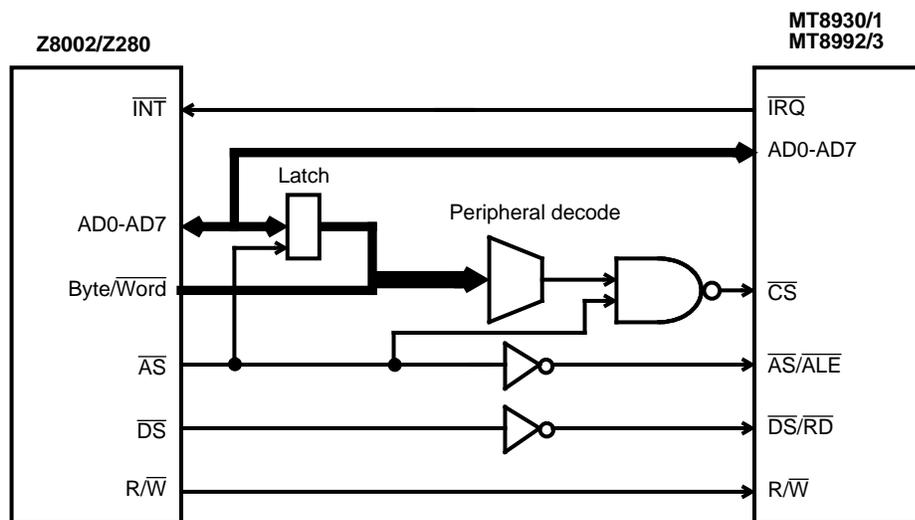
- The Z8002 has an active low "autovector" input.
- $\overline{AS}$ , the Zilog version of ALE, is active low and must be used to strobe the multiplexed address bits from the Address/Data bus into an external latch.
- The Z8002 supplies a  $R/\overline{W}$  signal.
- The Z8002  $\overline{DS}$  signal is active low and it is equivalent to 8086/88  $\overline{RD}$  and  $\overline{WR}$  strobes. This signal can be inverted to form E for Group 1 components.



10 (a) - Interfacing the MT8889 to the Z800/Z280



10 (b) - Interfacing the MT8952B to the Z800/Z280



10 (c) - Interfacing the MT8930/1 and the MT8992/3 to the Z800/Z280

Figure 10 - Interfacing the MT8889, MT8952B, MT8930/1 and the MT8992/3 to the Z8002/Z280

## 2.0 Group 2 Components

The interface of a Group 2 component is different from that of a Group 1 component in only two ways. The first difference is that there is no requirement for a Group 2 component to interrupt the microprocessor. The other difference is that a Group 2 device may respond more slowly to microprocessor accesses. This suggests a requirement for a Memory Ready output from the Group 2 component.

The Group 2 components have an output called  $\overline{DTA}$  which can also serve as an input to DTACK and MRDY on many CPUs. In fact, DTA was designed for the 68000, so it needs extra circuitry to interface to the "memory ready" schemes of the synchronous microprocessors. This circuit consists of 'NAND'ing the signal that selects the Group 2 component with the  $\overline{DTA}$  signal.

Aside from the above circuit changes, each Group 2 interface circuit is the same as the Group 1 circuit, so a discussion on each circuit is not necessary.

Zarlink Semiconductor provides five components under Group 2:

- MT8980
- MT8981
- MT8985
- MT8986

The MT8980/1/5 family provides signal compatibility to Motorola non-multiplexed bus type structure. Basically, the MT8980/1 devices provide timing compatibility to Motorola 8-bit CPUs such as the MC6800 family, including the 6802 and 6809. However, the MT8985 and MT8986 devices provide an enhanced parallel interface timing that allows a direct connection to faster CPUs such as Motorola's MC68000, Intel's 8086/8 and Zilog's Z8400 families.

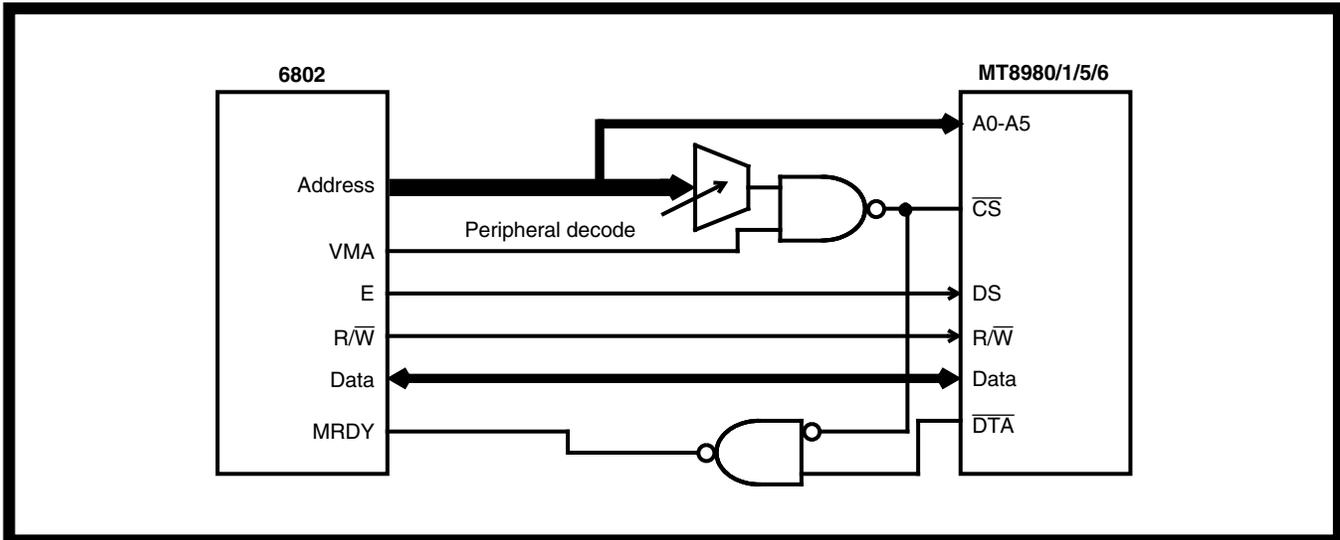


Figure 11 - Interfacing the MT8980/1/5/6 to the 6802

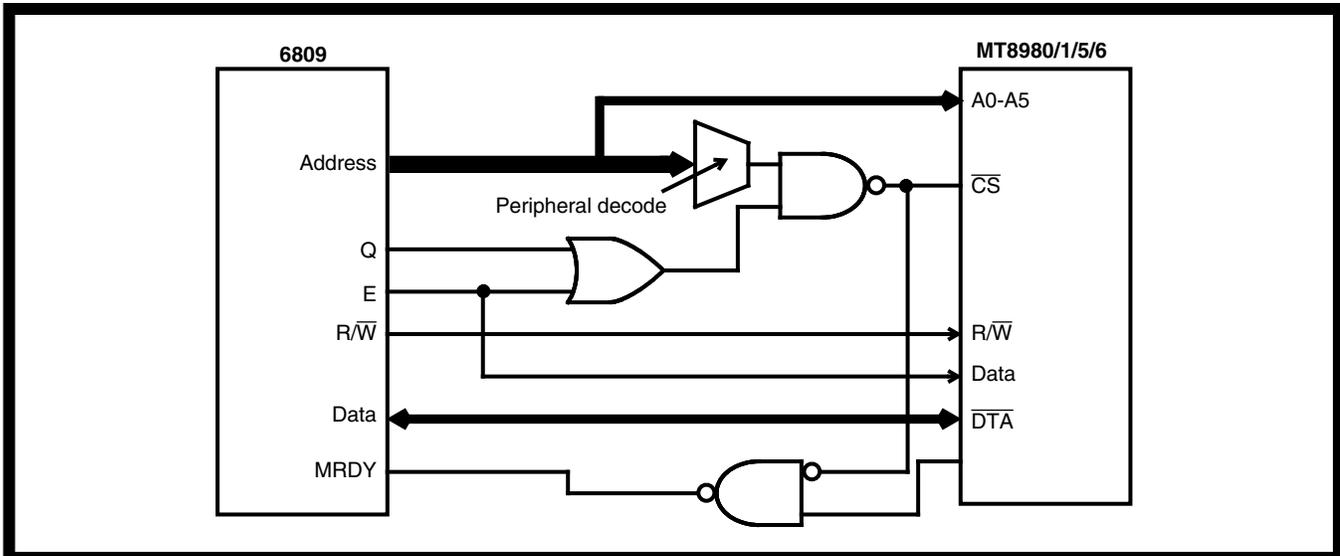


Figure 12 - Interfacing the MT8980/1/5/6 to the 6809

Since the MT8985 device retains all the functionality of the MT8980/1, Zarlink recommends the use of MT8985 with fast CPUs.

**2.1 Interfacing the MT8980 Family to the Intel 8051 or Motorola 68HC11**

An additional multiplexed bus structure is provided in the MT8986 PLCC-44 package. This simplifies the signal connection between the device and CPUs like Intel's 8085/6/8 and Zilog's Z8002/Z280.

When CPUs or microcontrollers do not provide  $\overline{DTACK}$  or MRDY input lines (e.g., Intel 8051, Motorola MC68HC11), an external "glue" circuit and a special software arrangement have to be implemented to allow for normal operation. For the details on the implementation of this circuit, see the *Applications* section of the MT8986 data sheet.

Figures 11 to 17 illustrates the connection examples for all of the MT8980 family.

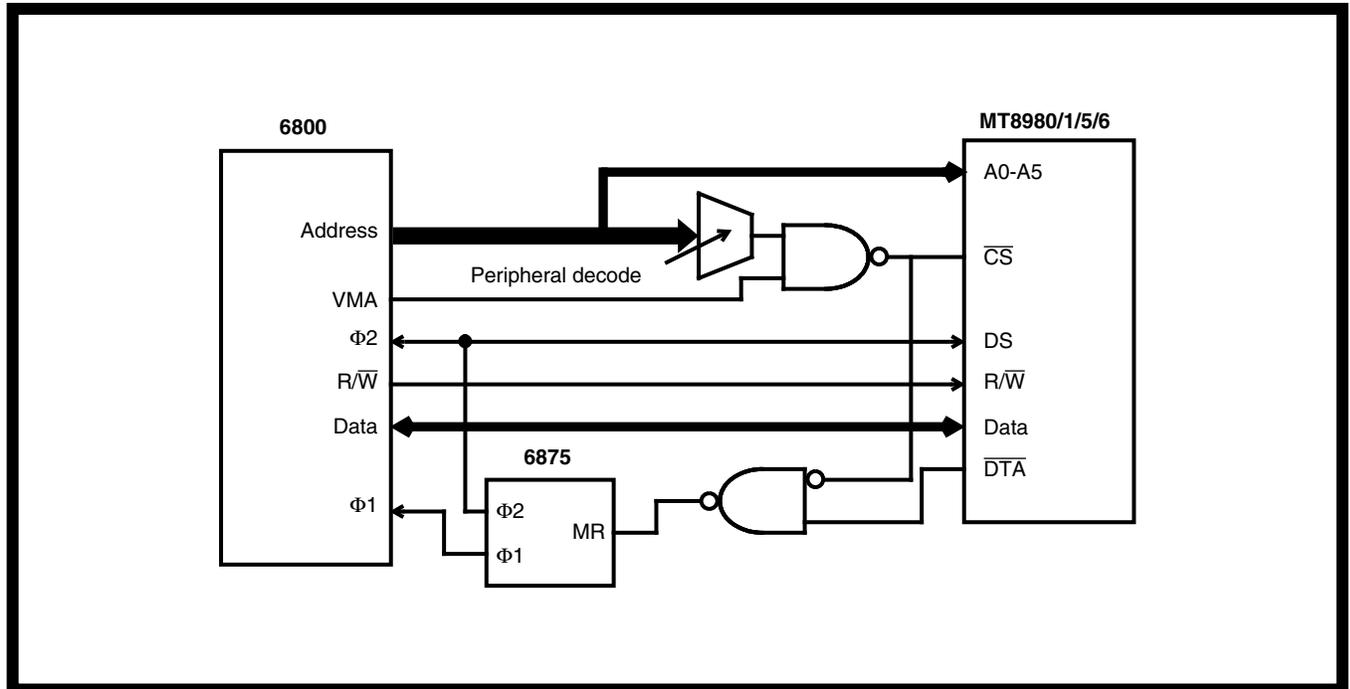


Figure 13 - Interfacing the MT8980/1/5/6 to the 6800

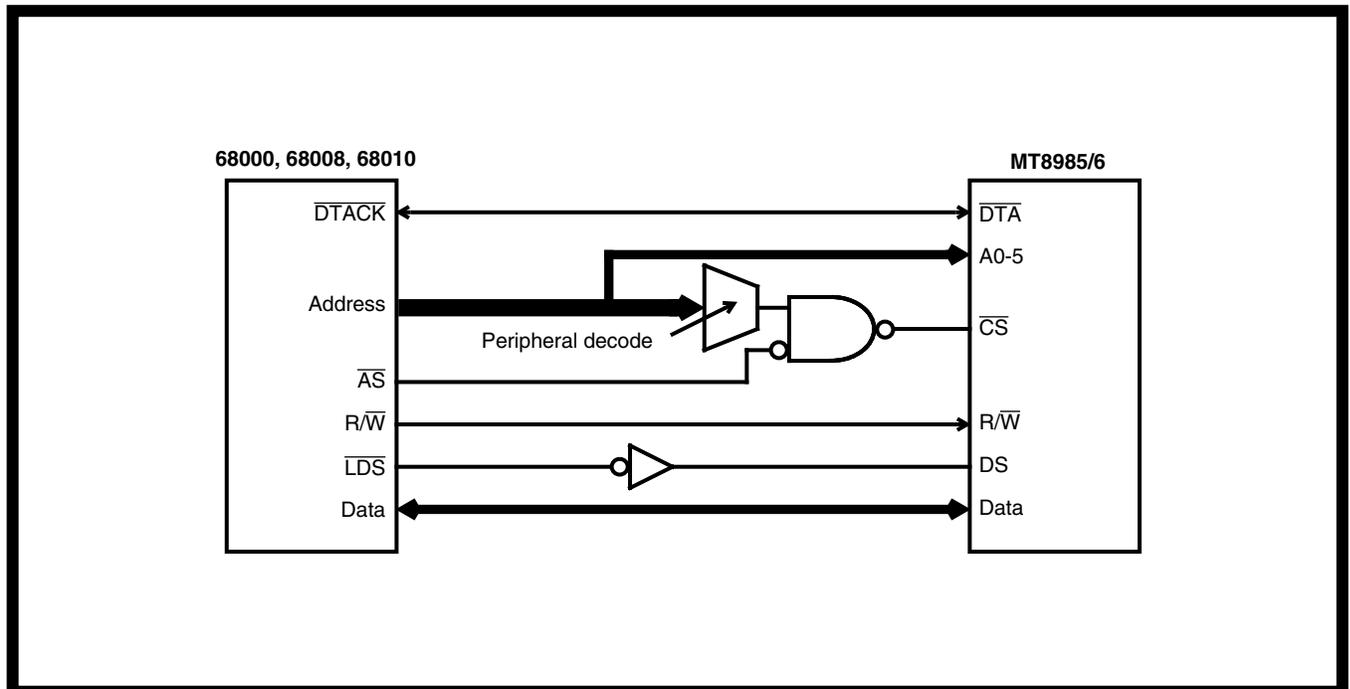


Figure 14 - Interfacing the MT8985/6 to the 68000, 68010 and the 68008

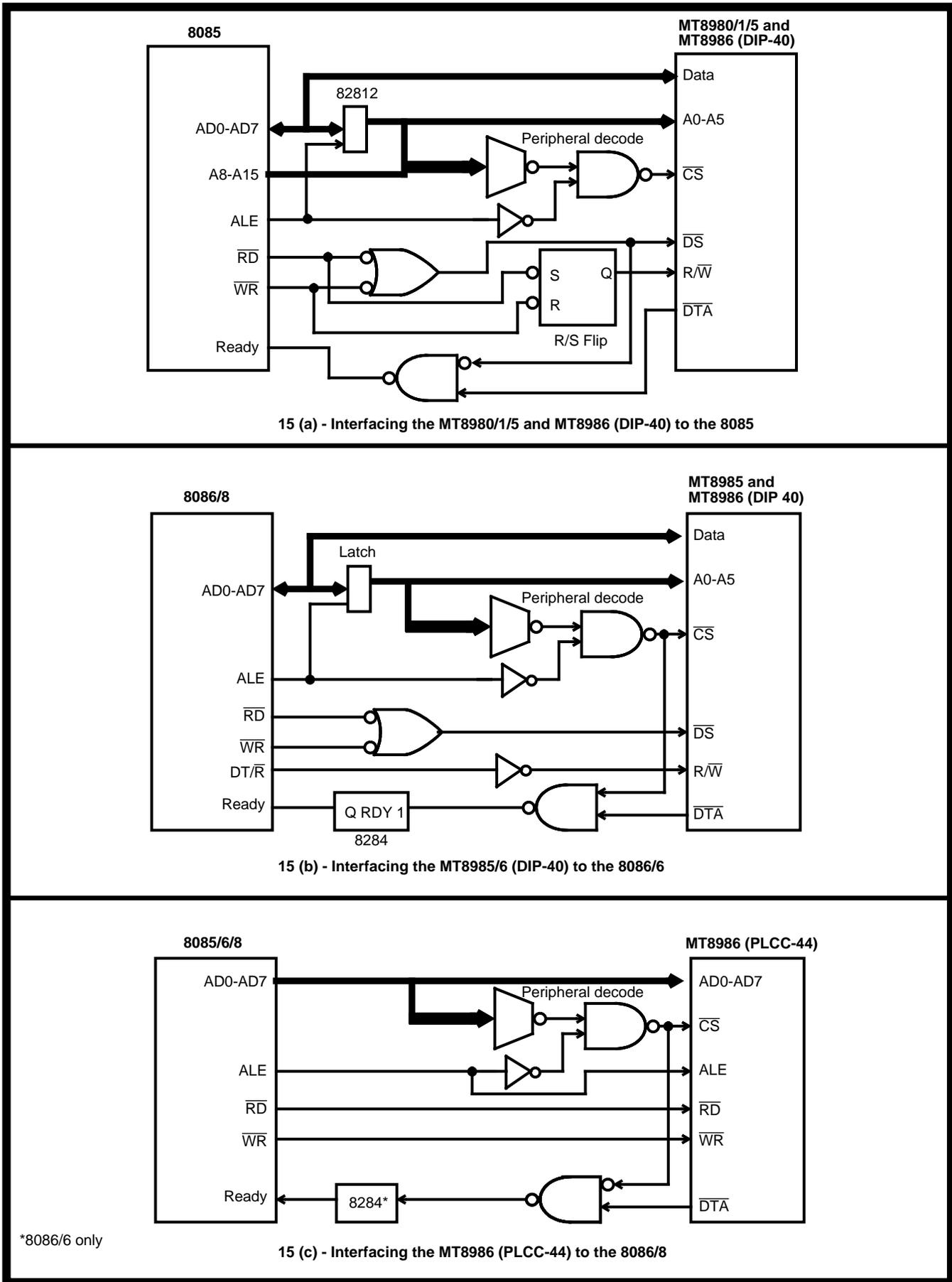


Figure 15 - Interfacing the MT8980/1/5/6 to the 8085/6/8

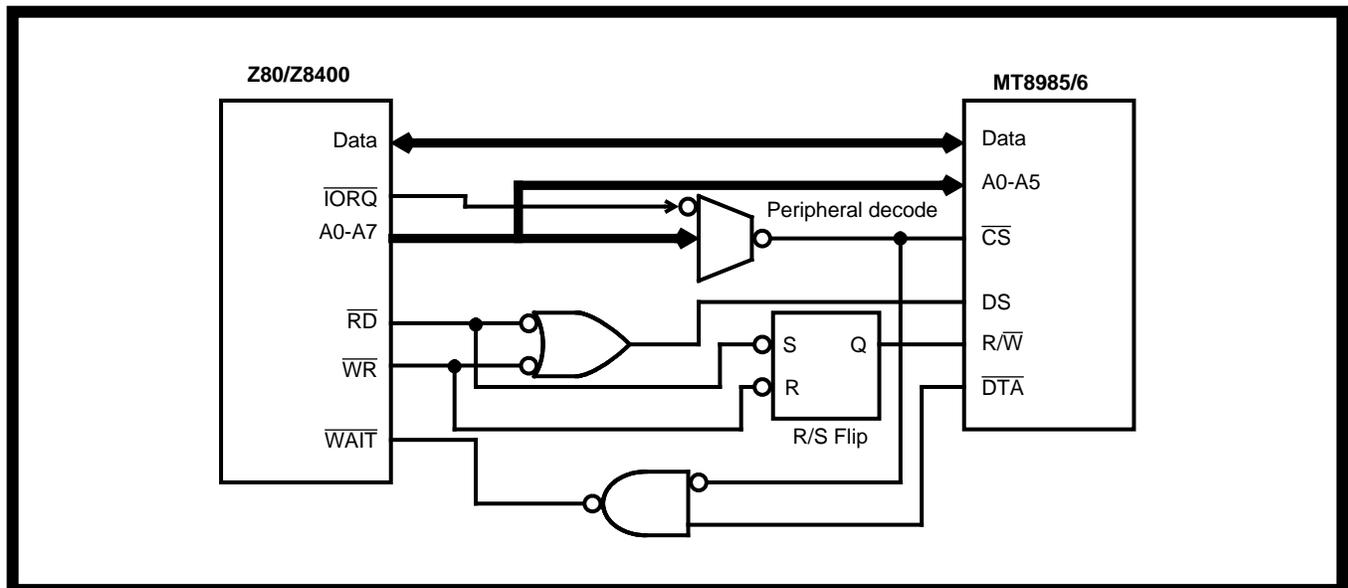


Figure 16 - Interfacing the MT8985/6 to the Z80/Z8400

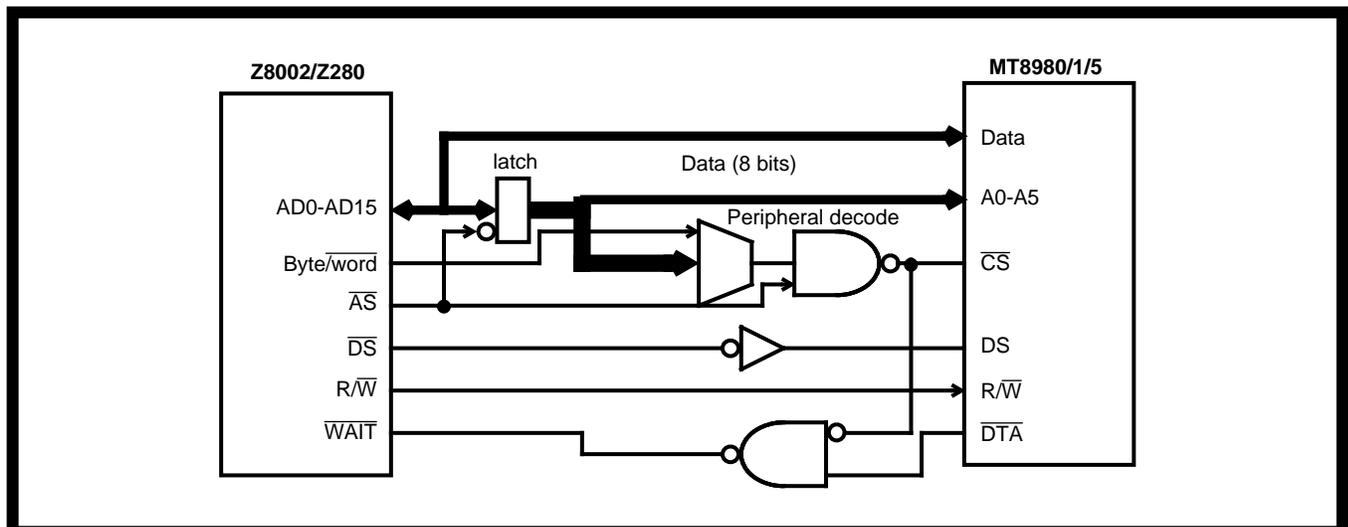


Figure 17 - Interfacing the MT8989/1/5 to the Z8002/Z280

### 3.0 Group 3 Components

The Group 3 component is a device called the ST-BUS Parallel Access (STPA). The STPA has three operating modes, but only one mode was designed specifically for microprocessor control, so the others shall not be covered. The STPA has almost the same interface as the Group 1 devices. The differences are:

- Data strobe is the proper polarity for the 68000 which means it must be inverted for Motorola 8-bit microprocessors. Only slight modifications are performed for other microprocessors.
- The STPA can provide vectored interrupts for the 68000. This will change the 68000/10/08 interface circuit.

Figures 18 to 25 show diagrams of Group 3 interfaces.

#### 3.1 Interfacing to the 68000/10/08

Figure 21 shows the circuit required to interface the MT8920 to the 68000. Note that  $\overline{\text{IACK}}$  is decoded, but rather than being combined with the chip select signal to produce  $\overline{\text{VPA}}$ ,  $\overline{\text{IACK}}$  combines with the state of A1-3 to provide an alternative select to the MT8980 (as opposed to the normal decode of the address bus). This dual approach to selecting the MT8980 is used because an interrupt acknowledge cycle transfers information from the MT8920 in the same manner as any normal read cycle. The decoded signal  $\overline{\text{IACK}}$  tells the MT8920 that it must transfer the interrupt vector programmed into it on to the data bus.

**3.2 Interfacing to the 8051 or 68HC11 Microcontrollers**

As explained in section 20, for CPUs not providing MRDY or  $\overline{DTACK}$  input lines (like 8051 and 68HC11), special hardware and software arrangements can be

made to allow Read/Write operations between the STPA and those CPUs. For an idea on how to implement these arrangements, see the Applications section of the MT8920B data sheet (*How to Interface the MT8920B and Intel's 8051*).

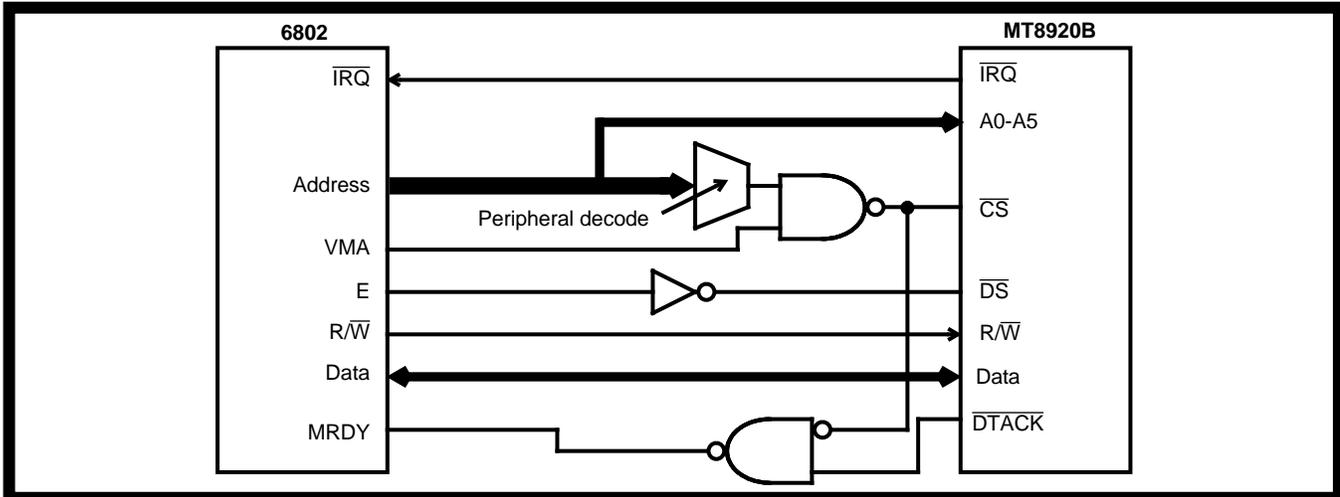


Figure 18 - Interfacing the MT8920B to the 6802

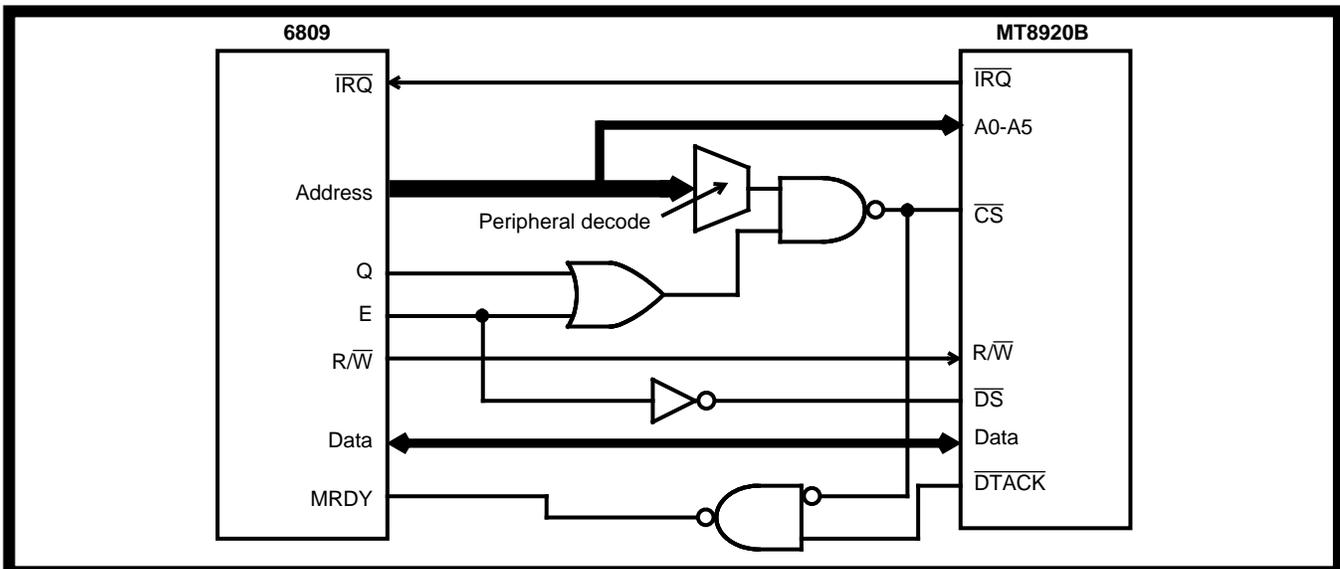


Figure 19 - Interfacing the MT8920B to the 6809

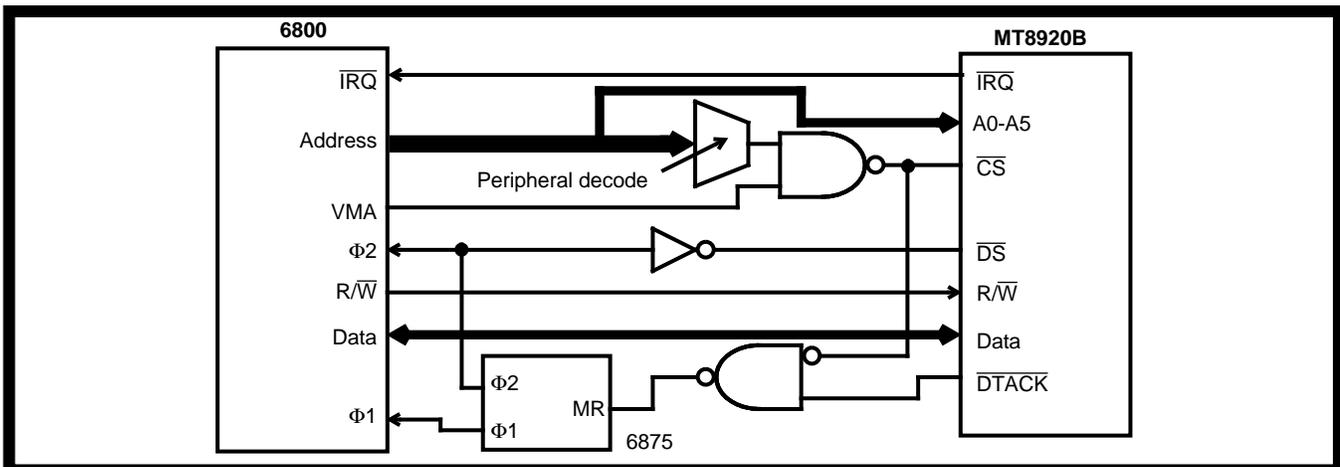


Figure 20 - Interfacing the MT8920B to the 6800

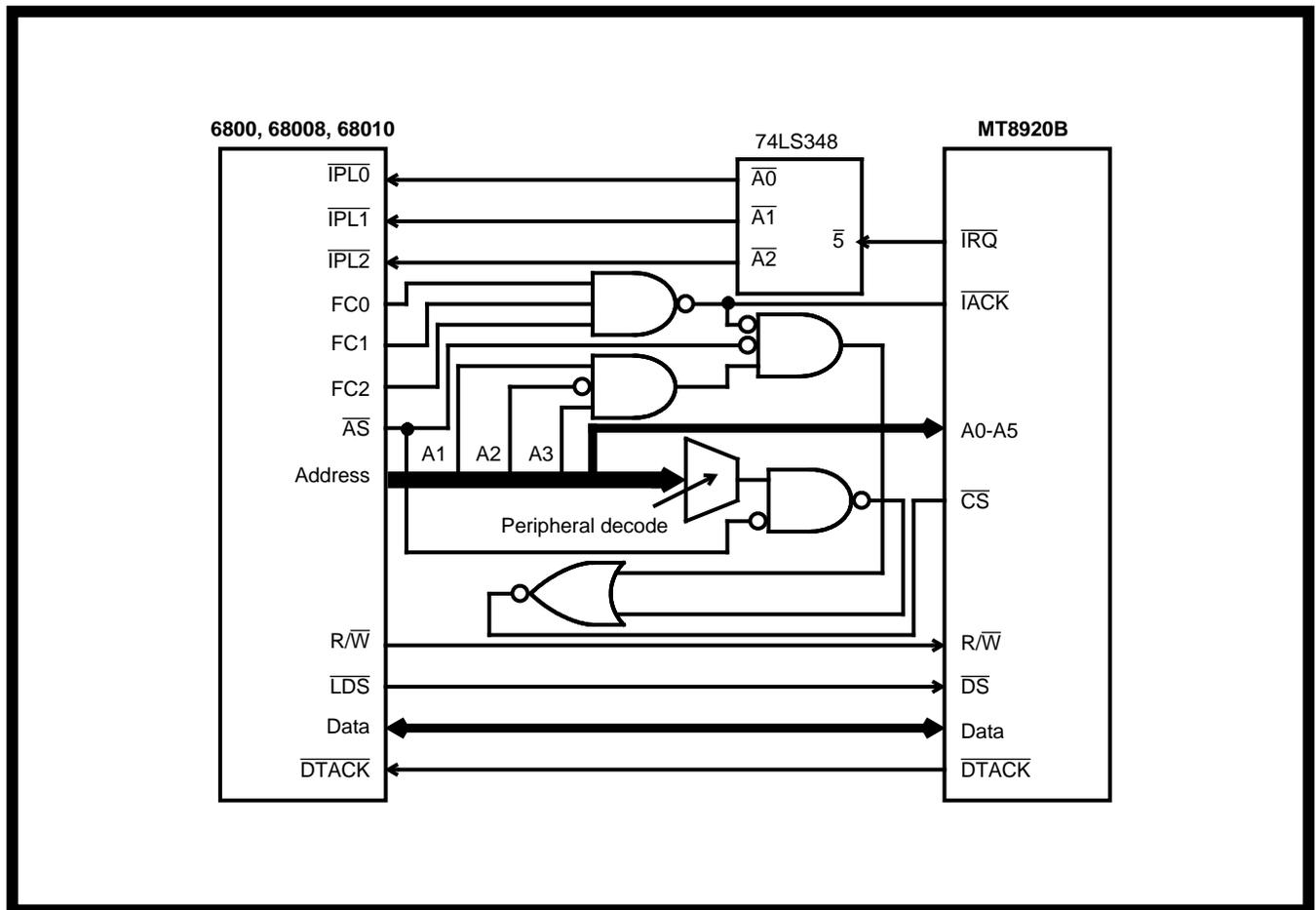


Figure 21 - Interfacing the MT8920B to the 68000, 68010 and the 68008

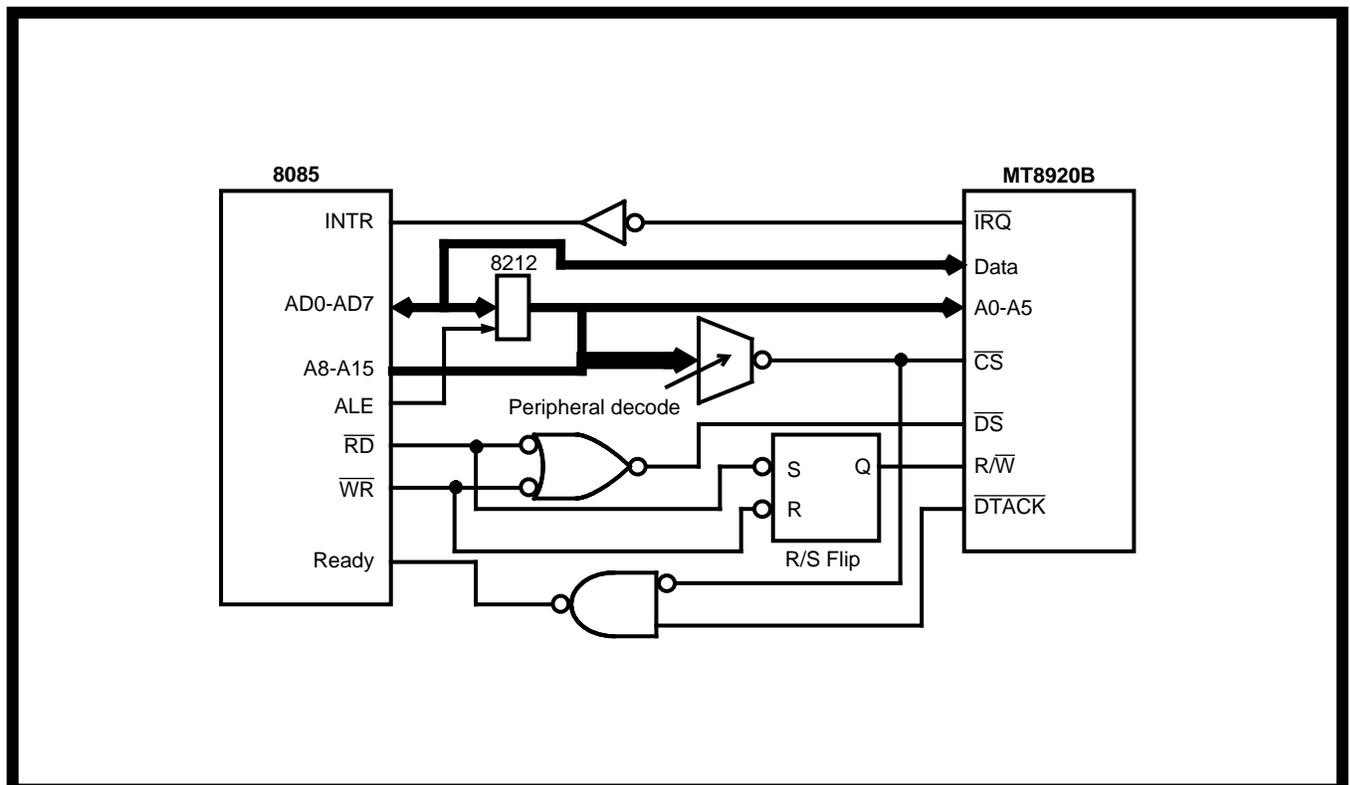


Figure 22 - Interfacing the MT8920B to the 8085

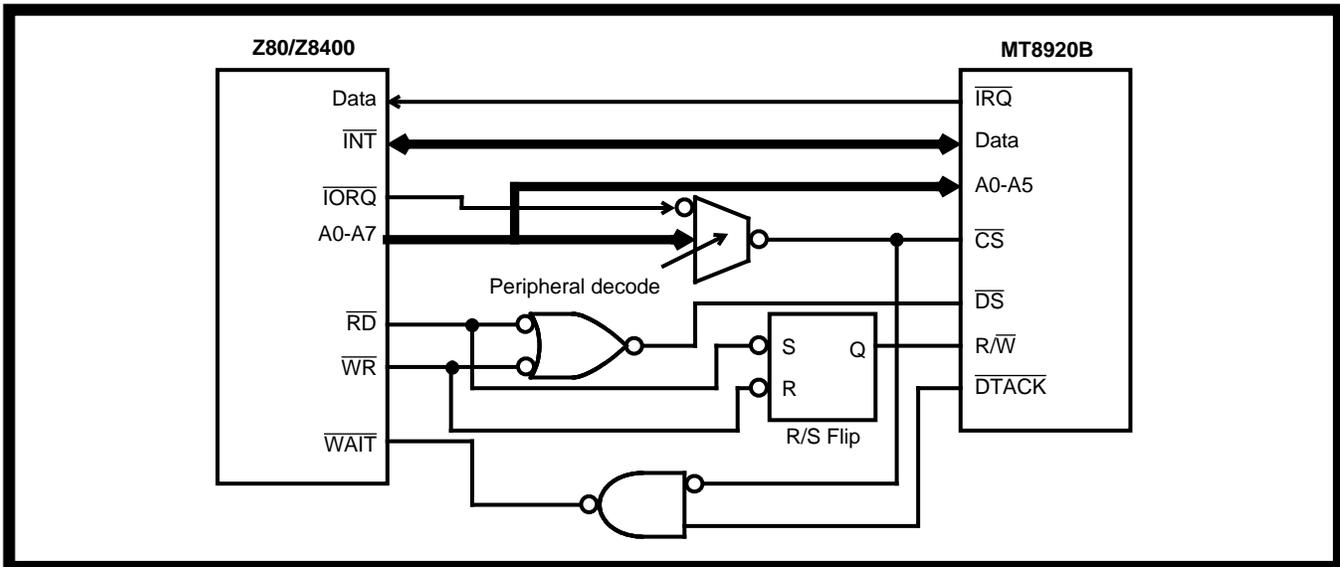


Figure 23 - Interfacing the MT8920B to the Z80/Z8400

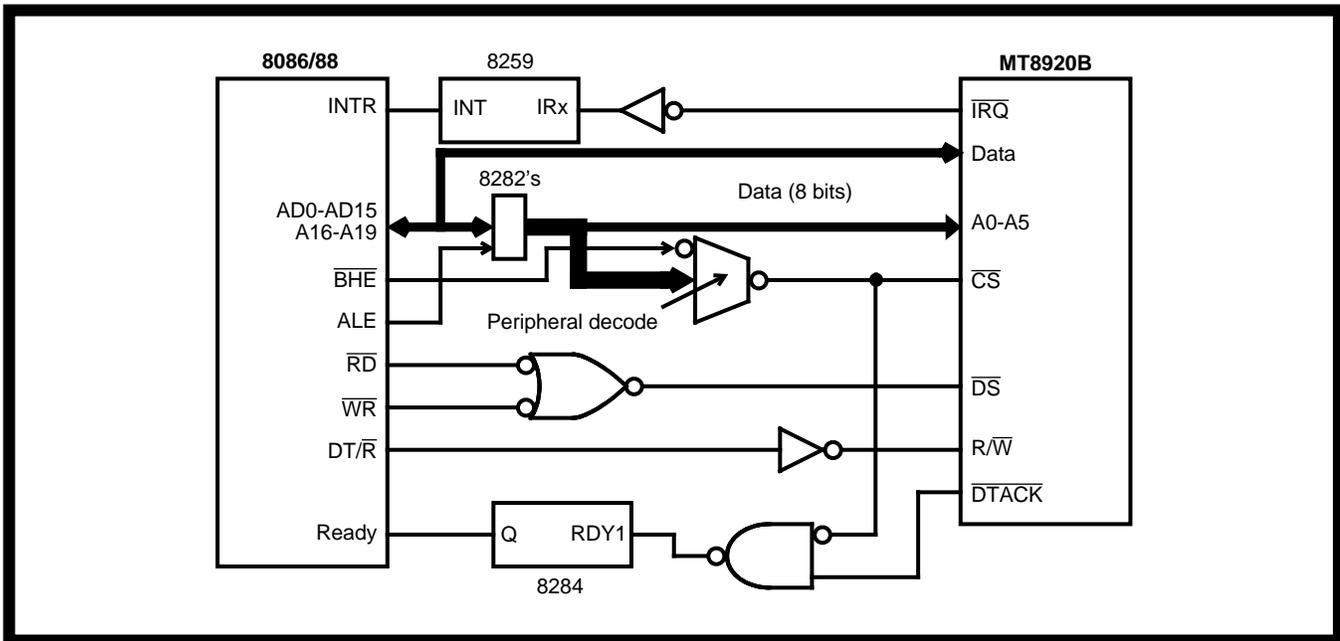


Figure 24 - Interfacing the MT8920B to the 8086/88

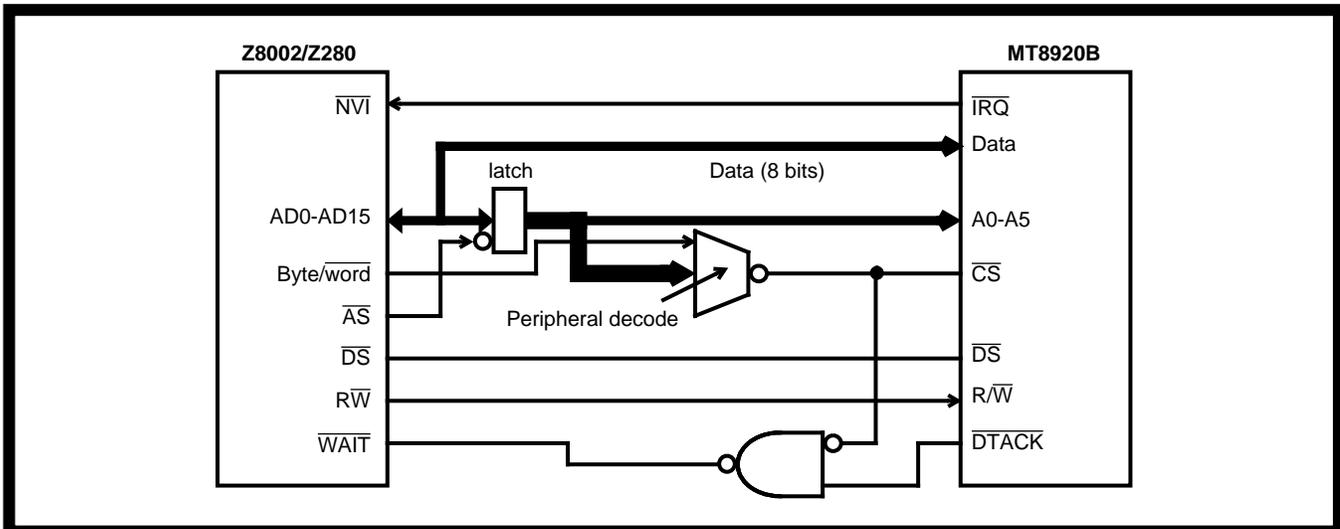


Figure 25 - Interfacing the MT8920B to the Z8002/Z280



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