DATA SHEET

NE567/SE567
Tone decoder/phase-locked loop

Product data
Supersedes data of 1992 Apr 15

2002 Sep 25

Philips
Semiconductors

PHILIPS

Tone decoder/phase-locked loop NE567/SE567

DESCRIPTION

The NE567/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

PIN CONFIGURATION

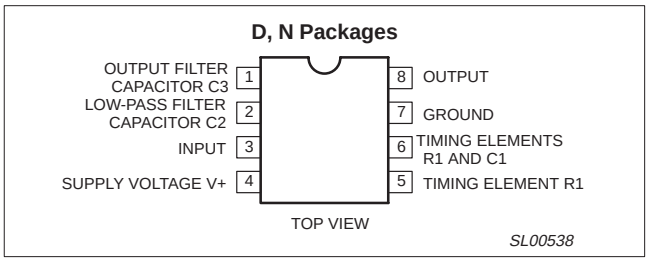

Figure 1. Pin configuration

FEATURES

- Wide frequency range (0.01 Hz to 500 kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100 mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor

APPLICATIONS

- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

BLOCK DIAGRAM

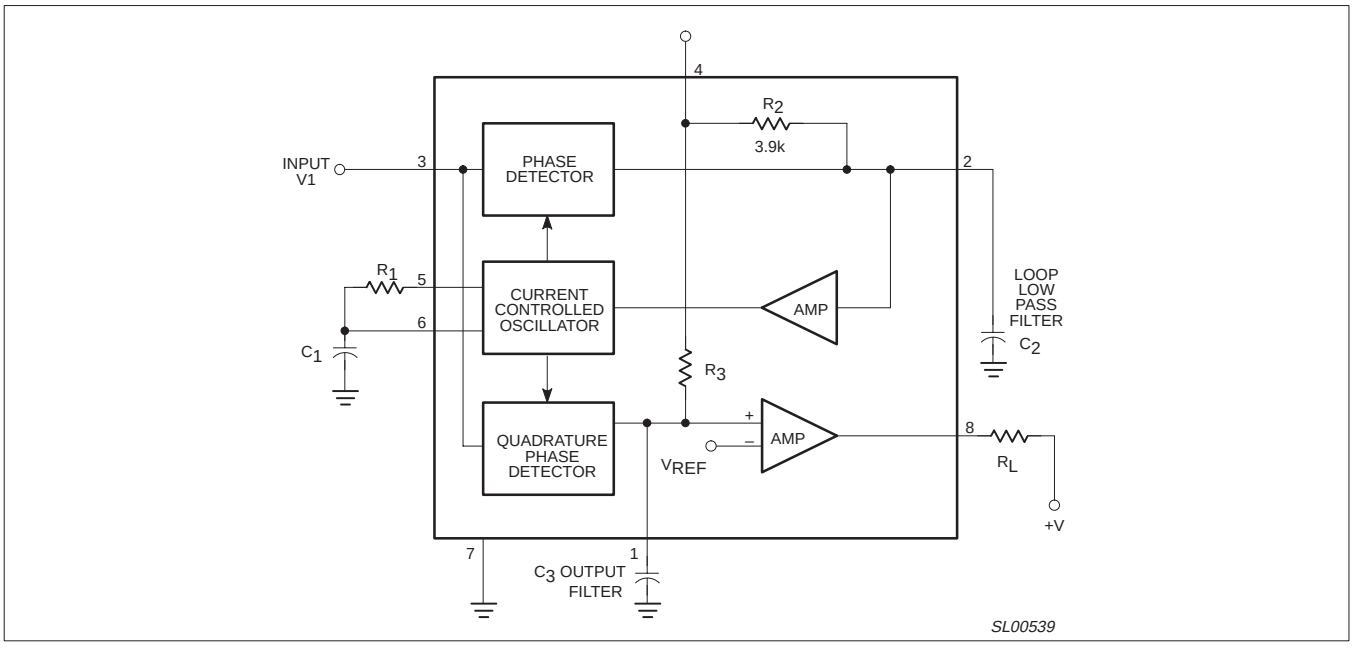

Figure 2. Block Diagram

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EQUIVALENT SCHEMATIC

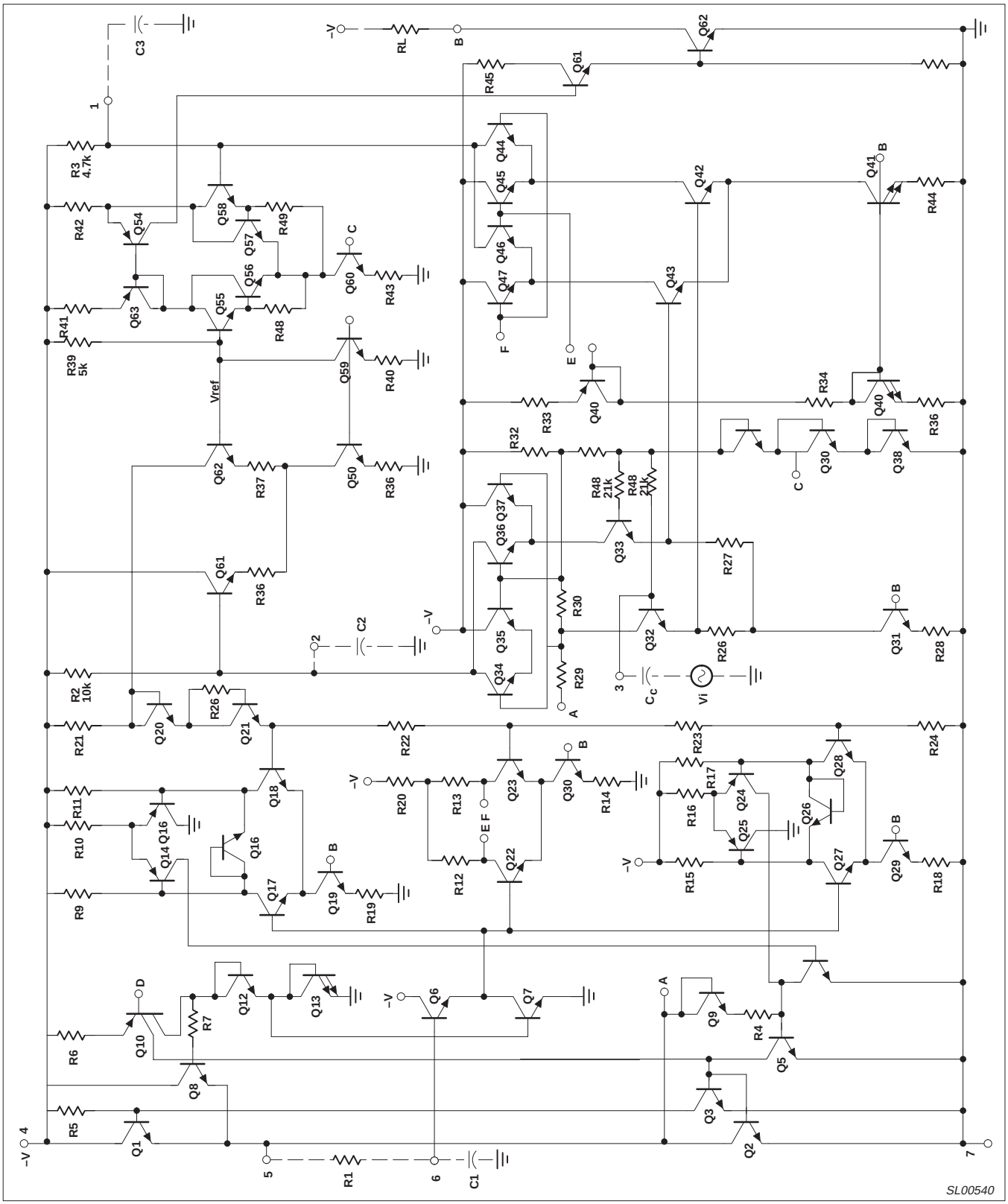


Figure 3. Equivalent schematic

ORDERING INFORMATION

ORDER CODE	DESCRIPTION	TEMPERATURE RANGE	DWG #
NE567D	SO8: plastic small outline package; 8 leads; body width 3.9 mm	0 °C to +70 °C	SOT96-1
NE567N	DIP8: plastic dual in-line package; 8 leads (300 mil)	0 °C to +70 °C	SOT97-1
SE567D	SO8: plastic small outline package; 8 leads; body width 3.9 mm	–55 °C to +125 °C	SOT96-1
SE567N	DIP8: plastic dual in-line package; 8 leads (300 mil)	–55 °C to +125 °C	SOT97-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{amb}	Operating temperature NE567 SE567	 0 to +70 –55 to +125	 °C °C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 +V_S	V
V–	Negative voltage at input	–10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{stg}	Storage temperature range	–65 to +150	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

V+ = 5.0 V; T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	–55 °C to +125 °C		35 ±140			35 ±140		ppm/°C
		0 °C to +70 °C		35 ±60			35 ±60		ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	–10	0	+10	–10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth—variation with temperature	V_I = 300 mV_{RMS}		±0.1			±0.1		%/°C
BW	Largest detection bandwidth—variation with supply voltage	V_I = 300 mV_{RMS}		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	I_L = 100 mA; $f_I = f_O$		20	25		20	25	mV_{RMS}
	Largest no-output input voltage[4]	I_L = 100 mA; $f_I = f_O$	10	15		10	15		mV_{RMS}
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	B_n = 140 kHz		–6			–6		dB
Output									
	Fastest on-off cycling rate			$f_O/20$			$f_O/20$		
	"1" output leakage current	V_8 = 15 V		0.01	25		0.01	25	µA
	"0" output voltage	I_L = 30 mA		0.2	0.4		0.2	0.4	V
		I_L = 100 mA		0.6	1.0		0.6	1.0	V
t_F	Output fall time[3]	R_L = 50 Ω		30			30		ns
t_R	Output rise time[3]	R_L = 50 Ω		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current—activated	R_L = 20 kΩ		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:
1. Frequency determining resistor R_1 should be between 2 and 20 kΩ
2. Applicable over 4.75 V to 5.75 V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With R_2 = 130 kΩ from Pin 1 to V+. See Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS

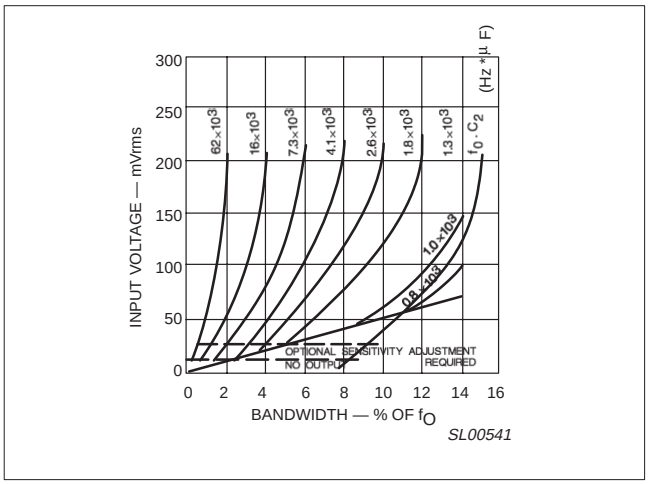


Figure 4. Bandwidth vs. input signal amplitude

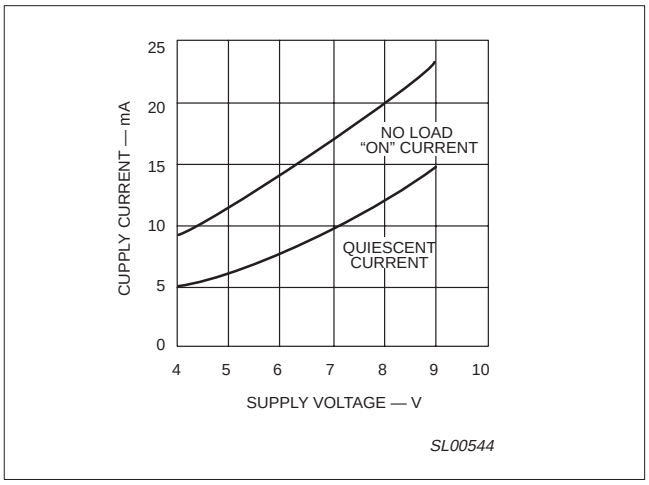


Figure 7. Typical supply current vs. supply voltage

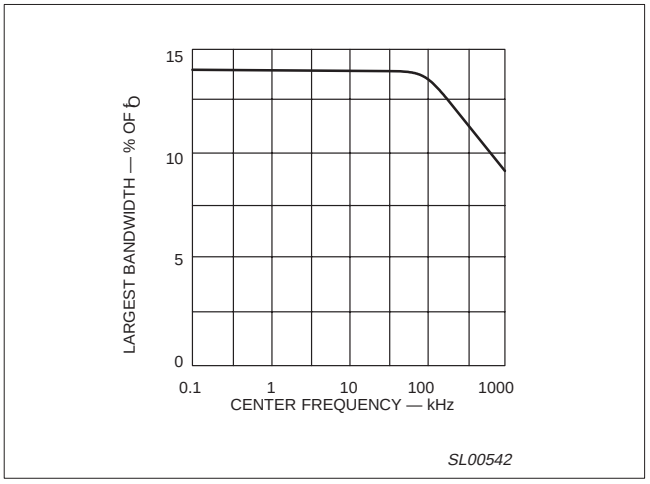


Figure 5. Largest detection bandwidth vs. operating frequency

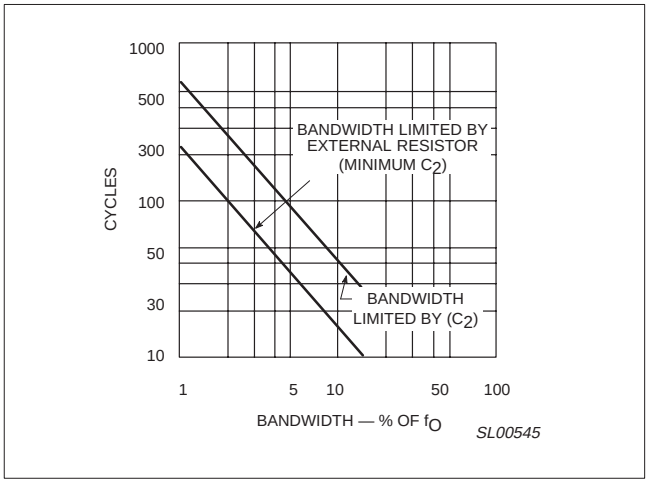


Figure 8. Greatest number of cycles before output

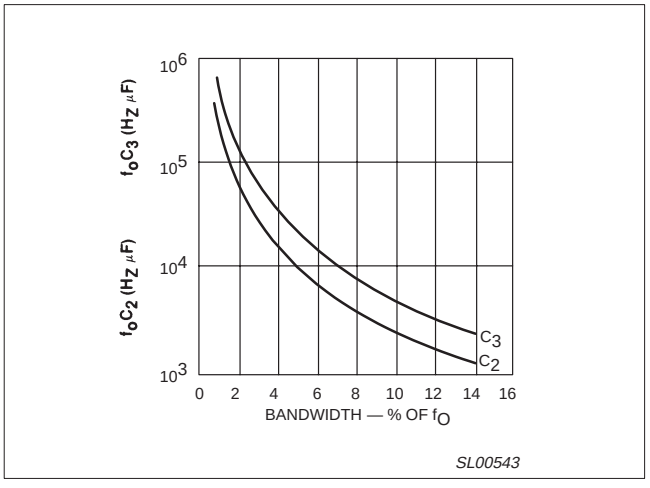


Figure 6. Detection bandwidth as a function of C_2 and C_3

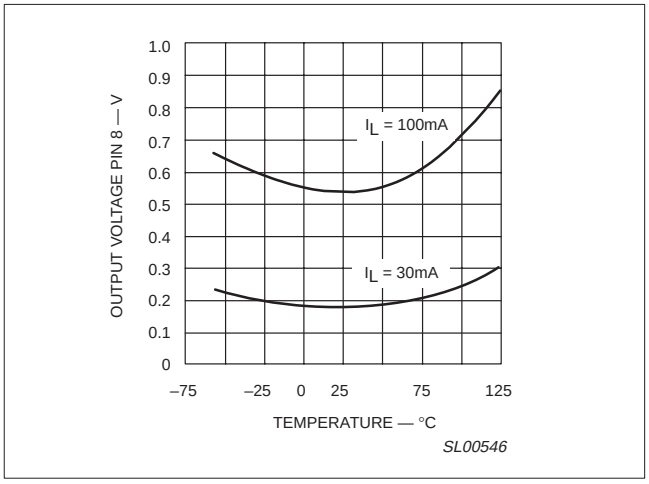


Figure 9. Typical output voltage vs. temperature

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

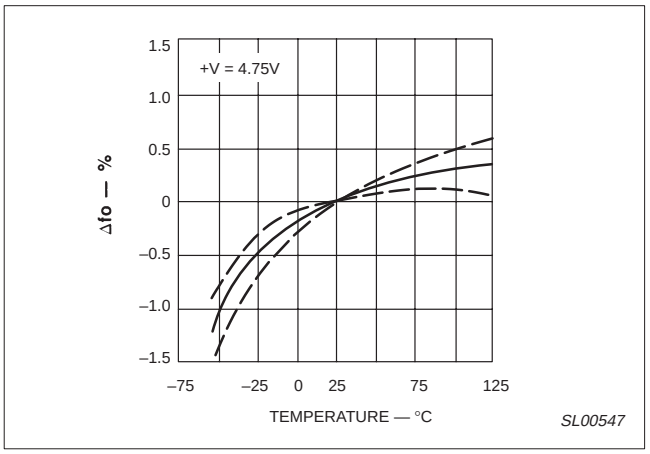


Figure 10. Typical frequency drift with temperature (Mean and SD)

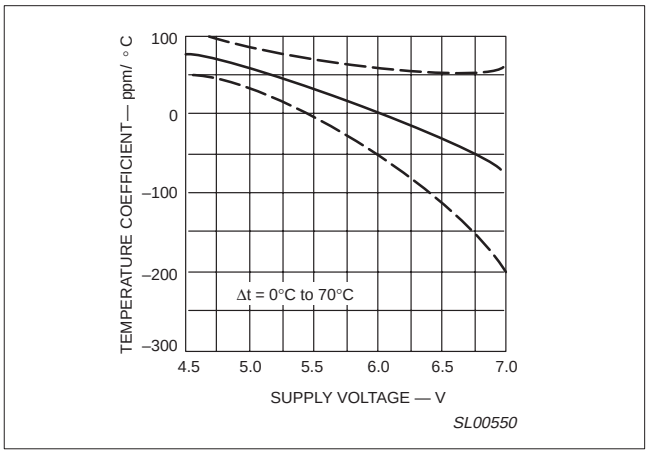


Figure 13. Center frequency temperature coefficient (Mean and SD)

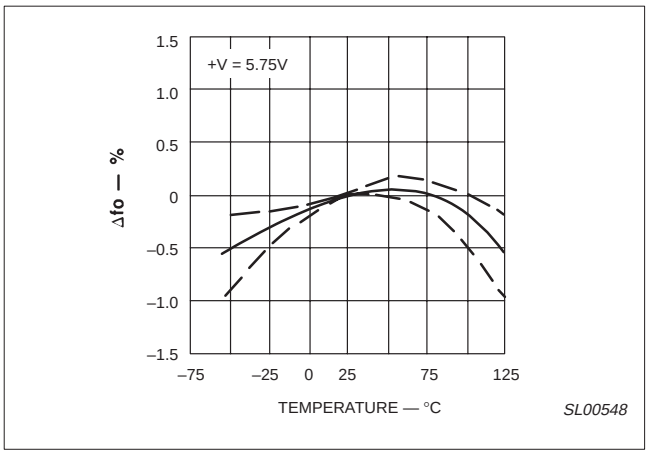


Figure 11. Typical frequency drift with temperature (Mean and SD)

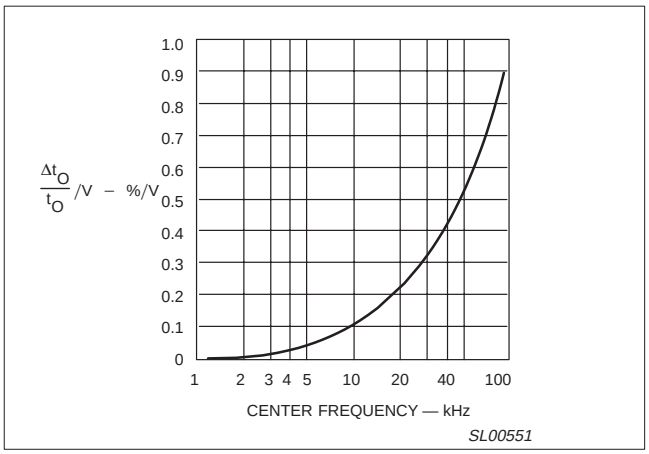


Figure 14. Center frequency shift with supply voltage change vs. operating frequency

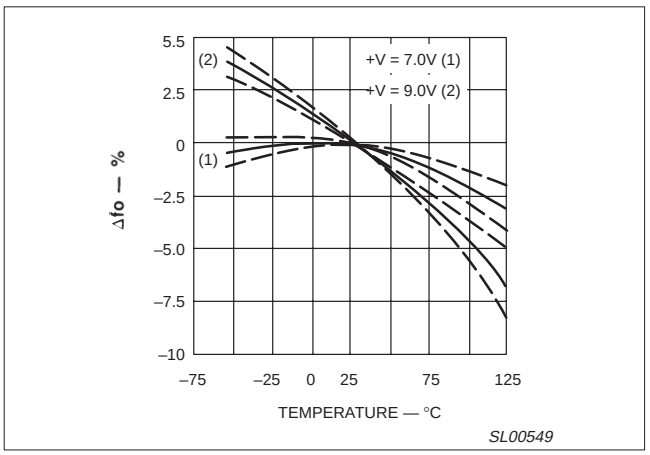


Figure 12. Typical frequency drift with temperature (Mean and SD)

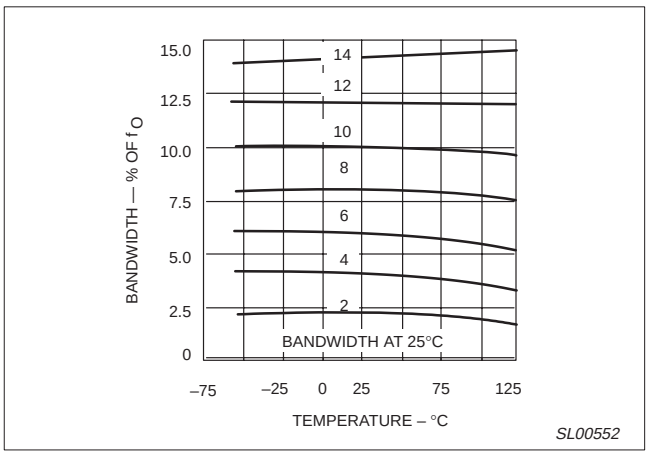


Figure 15. Typical bandwidth variation temperature

DESIGN FORMULAS

$$f_O \approx \frac{1}{1.1R_1\ C_1}$$

$$BW \approx 1070\sqrt{\frac{V_I}{f_O\ C_2}}\ \text{in \% of } f_O$$

$$V_I \leq 200mV_{RMS}$$

Where

V_I = Input voltage (V_{RMS})

C_2 = Low-pass filter capacitor (µF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically 20 mV_{RMS}) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection band skew

A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as:

$$\frac{\left(f_{MAX} + f_{MIN} - 2f_O\right)}{2f_O}$$

where f_{MAX} and f_{MIN} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 16 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R1 and C1 for the desired center frequency. For best temperature stability, R1 should be between 2 kΩ and 20 kΩ, and the combined temperature coefficient of the R1C1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low-pass capacitor, C2, by referring to Figure 4, 'Bandwidth vs. input signal amplitude'. If the input amplitude variation is known, the appropriate value of $f_O \cdot C_2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mV_{RMS}. The bandwidth, as noted on the graph, is then controlled solely by the $f_O \cdot C_2$ product (f_O (Hz), C2(µF)).
3. The value of C3 is generally non-critical. C3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

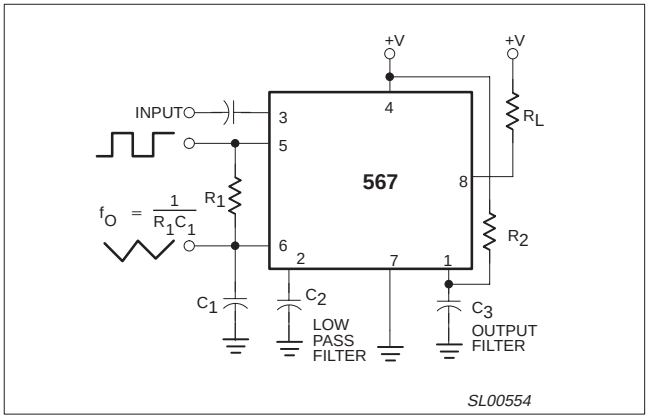


Figure 16. Typical connection

4. Optional resistor R2 sets the threshold for the largest "no output" input voltage. A value of 130 kΩ is used to assure the tested limit of 10 mV_{RMS} min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

TYPICAL RESPONSE

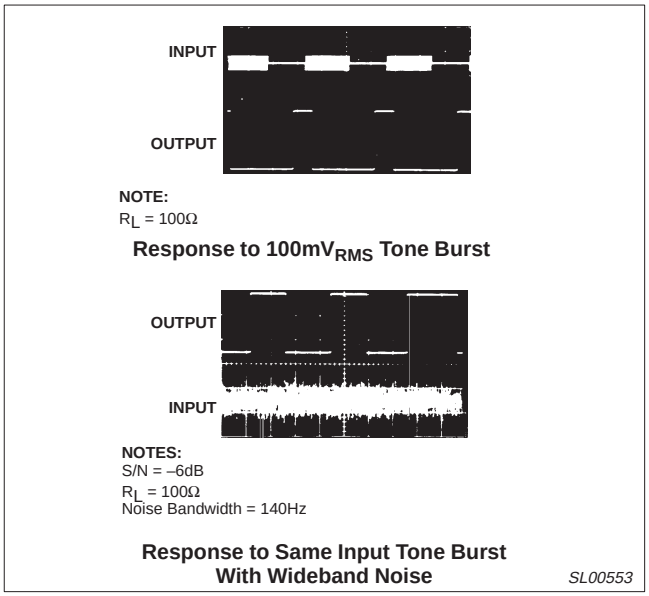


Figure 17. Typical response

AVAILABLE OUTPUTS (Figure 18)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \cong (+V - 1.4V)$ having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

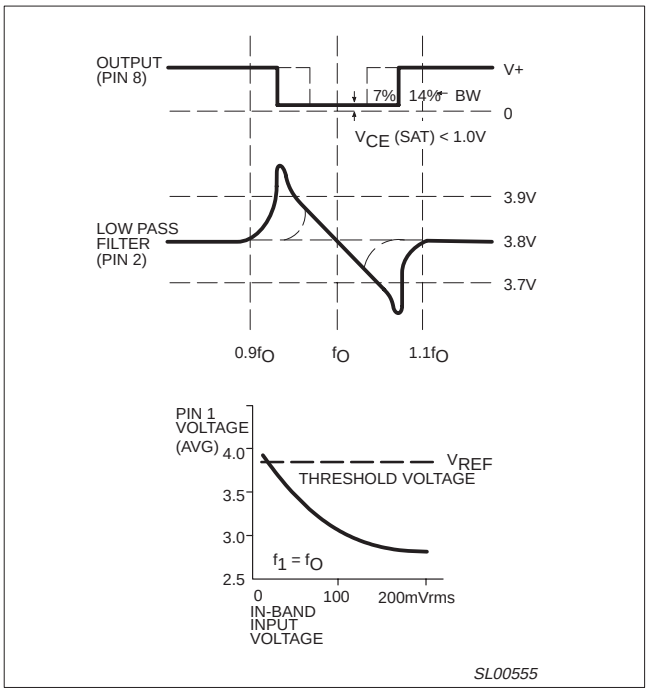


Figure 18. Available outputs

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200 mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n+1)\ f_O$, and will give an output for signals near $(4n+1)\ f_O$ where n = 0, 1, 2, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200 mV_{RMS}) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20 ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

$$C_2 = \frac{130}{f_O}\ \mu F$$

$$C_3 = \frac{260}{f_O}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 19)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

SENSITIVITY ADJUSTMENT (Figure 19)

When operated as a very narrow-band detector (less than 8%), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10 mV or lower).

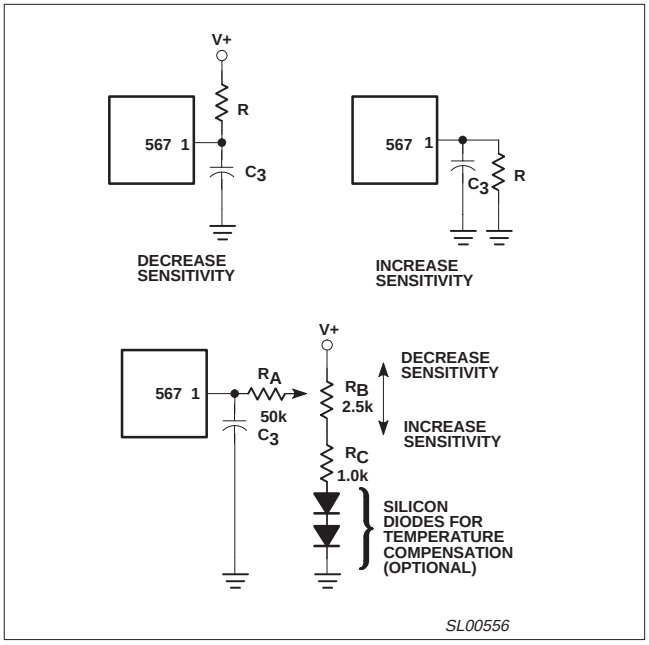


Figure 19. Sensitivity adjustment

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 20)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 20. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

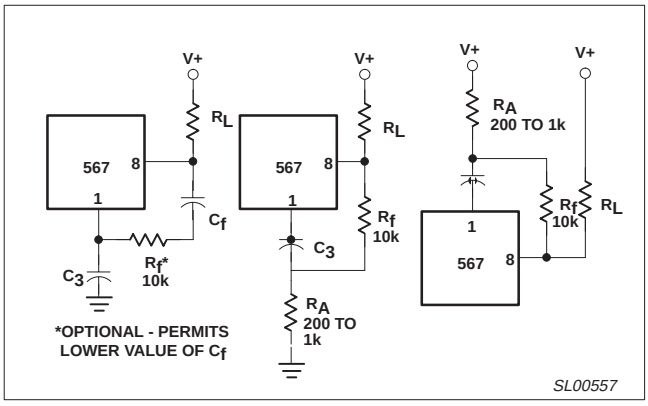


Figure 20. Chatter prevention

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT (Figure 21)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

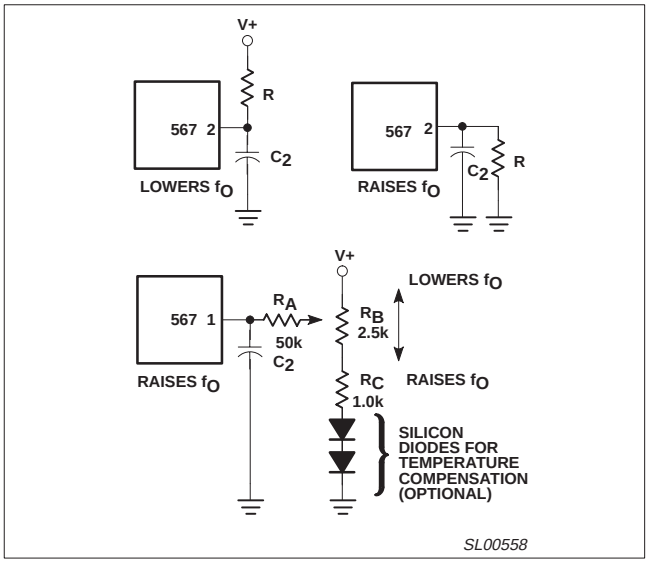
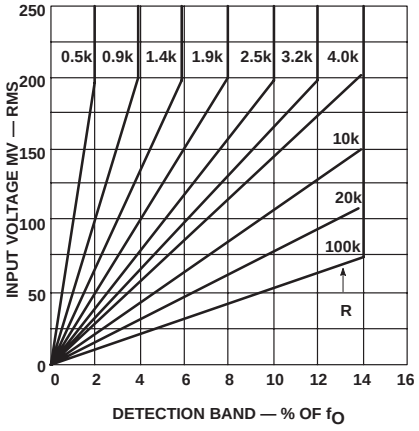
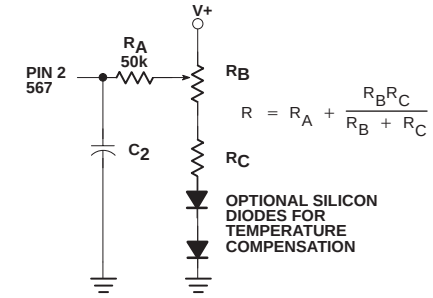


Figure 21. Skew adjust

ALTERNATE METHOD OF BANDWIDTH REDUCTION (Figure 22)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.





NOTE:

$$\frac{130}{f_O}\left(\frac{10k + R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k + R}{R}\right)$$

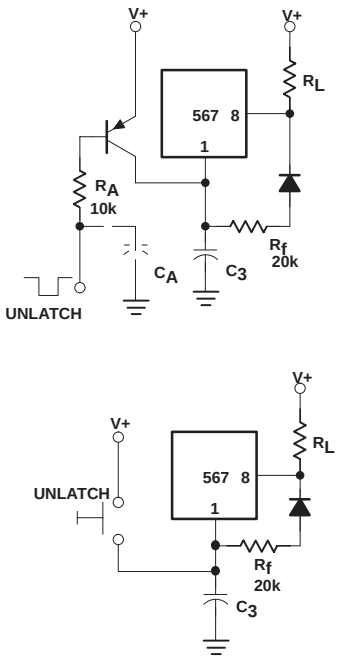
Adjust control for symmetry of detection band edges about f_O.

SL00559

Figure 22. BW reduction

OUTPUT LATCHING (Figure 23)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled-up to unlatch the output stage.



NOTE:

C_A prevents latch-up when power supply is turned on.

SL00560

Figure 23. Output latching

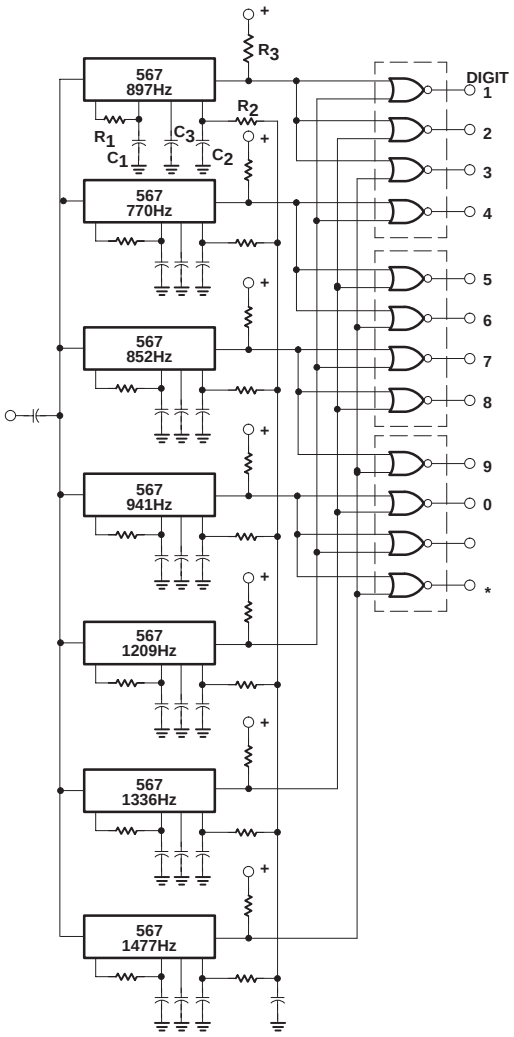
REDUCTION OF C1 VALUE

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.

TYPICAL APPLICATIONS



NOTES:

Component values (Typical)

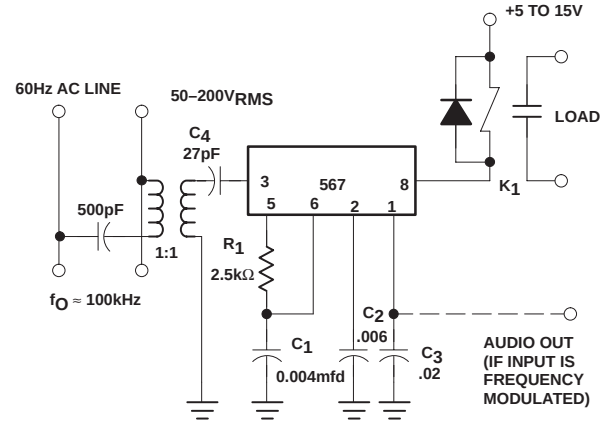
R_1 = 26.8 to 15kΩ
R_2 = 24.7kΩ
R_3 = 20kΩ
C_1 = 0.10mF
C_2 = 1.0mF 5V
C_3 = 2.2mF 6V
C_4 = 250µF 6V

Touch-Tone® Decoder

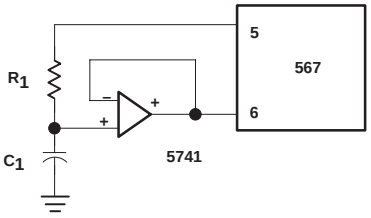
SL00561

Figure 24. Typical applications

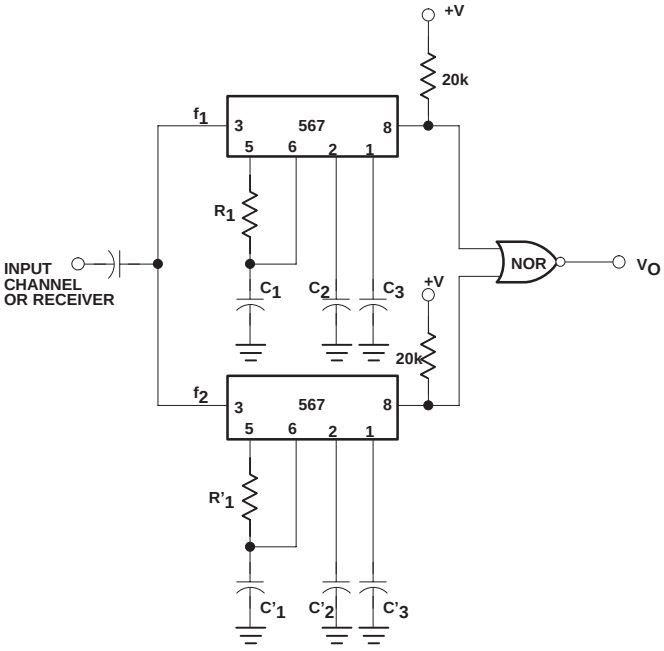
TYPICAL APPLICATIONS *(continued)*



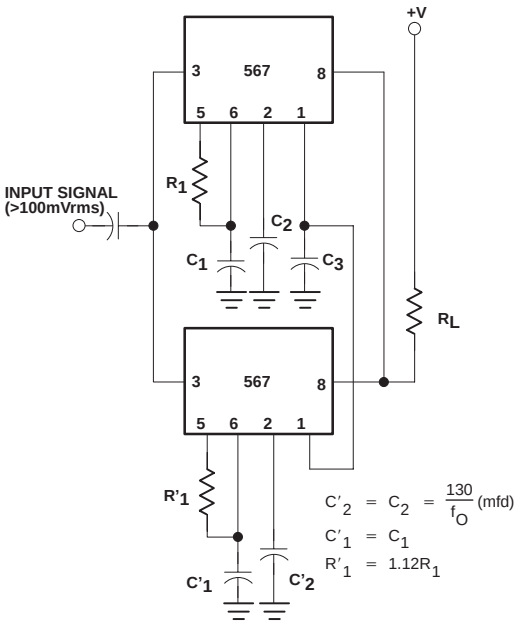
Carrier-Current Remote Control or Intercom



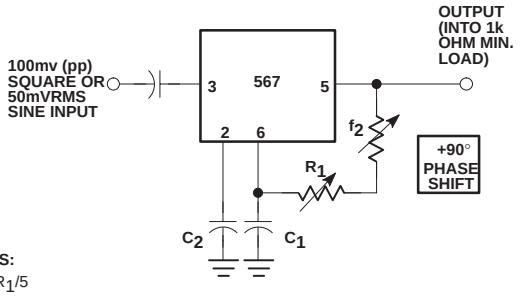
Precision VLF



Dual-Tone Decoder



24% Bandwidth Tone Decoder



NOTES:
$R_2 = R_1/5$
Adjust R_1 so that $\phi = 90°$ with control midway.

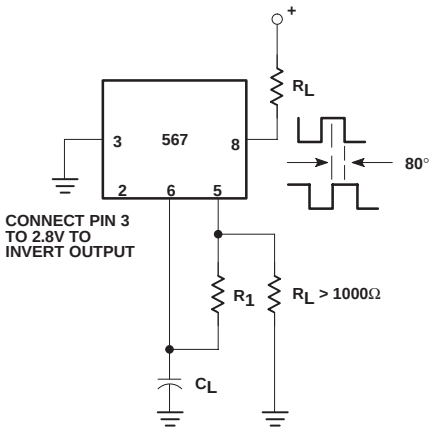
0° to 180° Phase Shifter

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

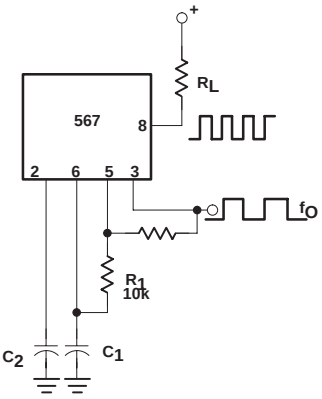
SL00562

Figure 25. Typical applications *(cont.)*

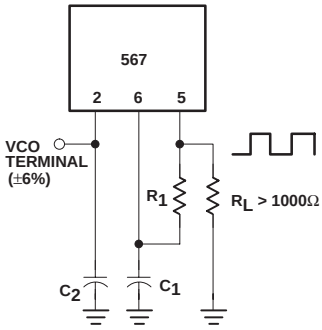
TYPICAL APPLICATIONS *(continued)*



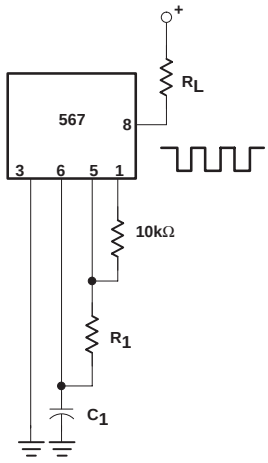
Oscillator With Quadrature Output



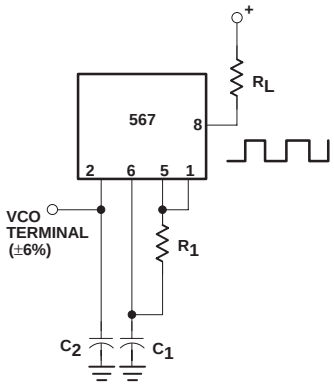
Oscillator With Double Frequency Output



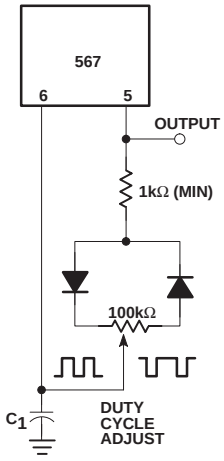
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads

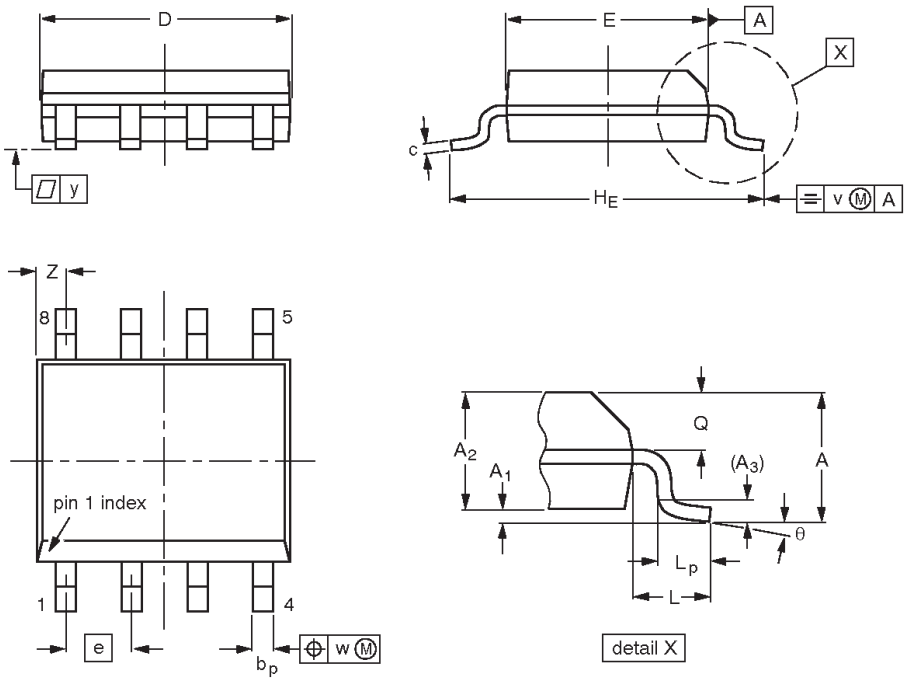


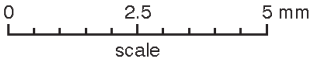
Pulse Generator

SL00563

Figure 26. Typical applications *(cont.)*

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

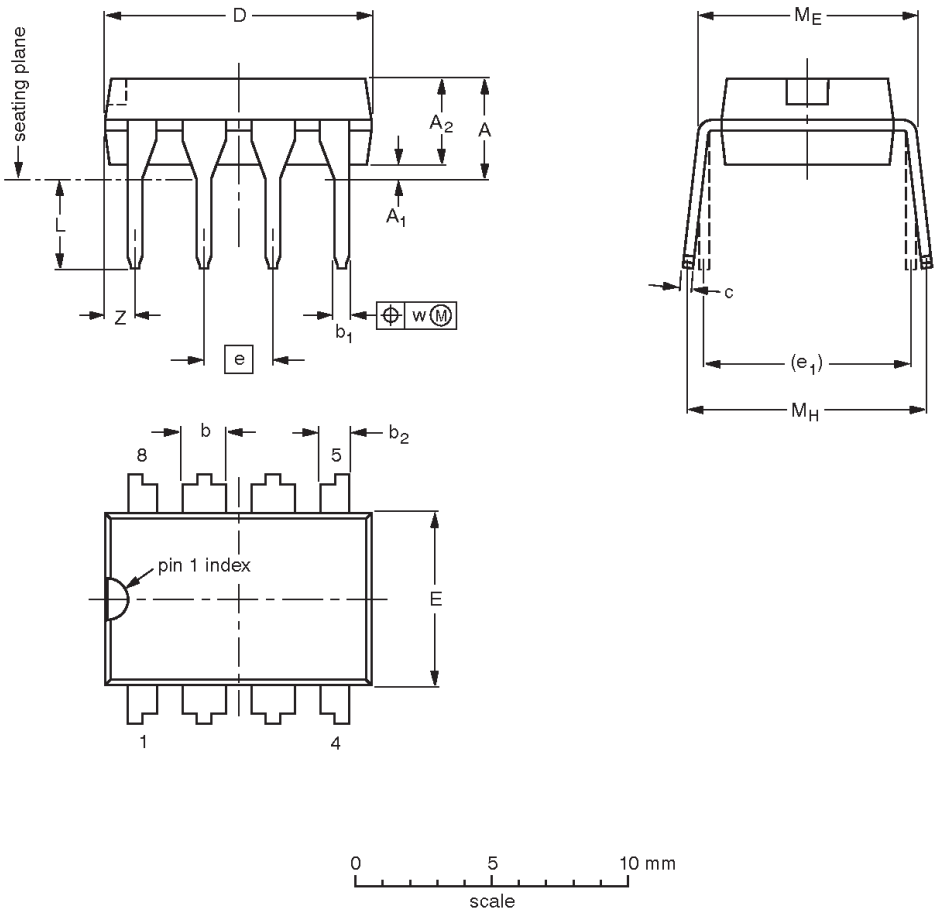
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

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