# INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# **74HC/HCT157**Quad 2-input multiplexer

Product specification
File under Integrated Circuits, IC06

December 1990





# **Quad 2-input multiplexer**

# 74HC/HCT157

#### **FEATURES**

· Non-inverting data path

· Output capability: standard

• I<sub>CC</sub> category: MSI

#### **GENERAL DESCRIPTION**

The 74HC/HCT157 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ( $\overline{E}$ ) is active LOW. When  $\overline{E}$  is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$$1Y = \overline{E}.(1I_1.S + 1I_0.\overline{S})$$

$$2Y = \overline{E}.(2I_1.S + 2I_0.\overline{S})$$

$$3Y = \overline{E}.(3I_1.S + 3I_0.\overline{S})$$

$$4Y = \overline{E}.(4I_1.S + 4I_0.\overline{S})$$

The "157" is identical to the "158" but has non-inverting (true) outputs.

#### **QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25 \, ^{\circ}C$ ;  $t_r = t_f = 6 \, \text{ns}$ 

CVMDOL	DADAMETED	CONDITIONS	TYF	PICAL	LINUT	
SYMBOL	PARAMETER	CONDITIONS	нс	нст	UNIT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$				
	nl <sub>0</sub> , nl <sub>1</sub> to nY		11	13	ns	
	E to nY		11	12	ns	
	S to nY		12	19	ns	
Cı	input capacitance		3.5	3.5	pF	
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	70	70	pF	

#### **Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$ 

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$ For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5$  V

#### ORDERING INFORMATION

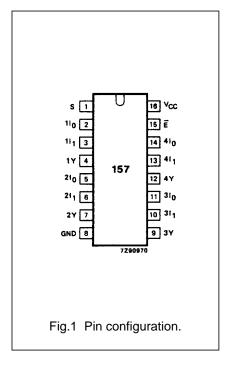
See "74HC/HCT/HCU/HCMOS Logic Package Information".

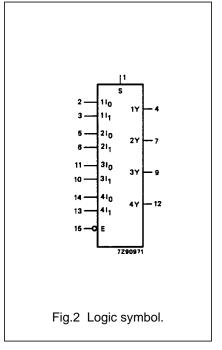
# Quad 2-input multiplexer

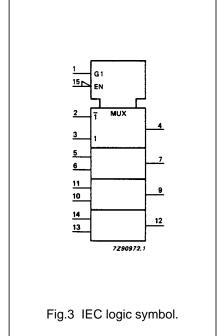
# 74HC/HCT157

## **PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	1I <sub>0</sub> to 4I <sub>0</sub>	data inputs from source 0
3, 6, 10, 13	1I <sub>1</sub> to 4I <sub>1</sub>	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	multiplexer outputs
8	GND	ground (0 V)
15	Ē	enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage

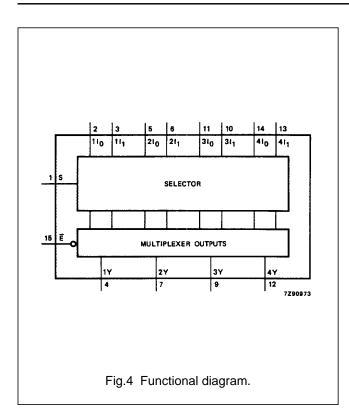






# Quad 2-input multiplexer

# 74HC/HCT157

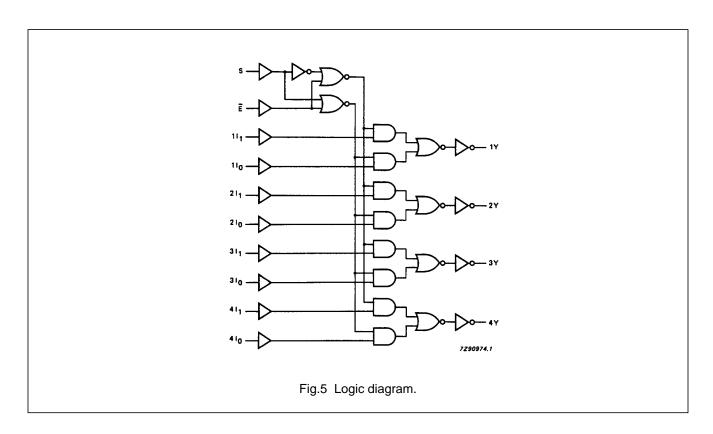


## **FUNCTION TABLE**

	OUTPUT			
Ē	S	nY		
Н	Х	Х	Х	L
L	L	L	Χ	L
L	L	Н	Χ	Н
L	Н	Х	L	L
L	Н	Х	Н	Н

## **Notes**

H = HIGH voltage level
 L = LOW voltage level
 X = don't care



# Quad 2-input multiplexer

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

# **AC CHARACTERISTICS FOR 74HC**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
		74HC									
		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(-)	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay		36	125		155		190	ns	2.0	Fig.7
	nl <sub>0</sub> to nY;		13	25		31		38		4.5	
	nl <sub>1</sub> to nY		10	21		26		32		6.0	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay		39	115		145		175	ns	2.0	Fig.6
	E to nY		14	23		29		35		4.5	
			11	20		25		30		6.0	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay		41	125		155		190	ns	2.0	Fig.7
	S to nY		15	25		31		38		4.5	
			12	21		26		32		6.0	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition		19	75		95		110	ns	2.0	Fig.6 and Fig.7
	time		7	15		19		22		4.5	
			6	13		16		19		6.0	

# Quad 2-input multiplexer

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

# Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nl <sub>0</sub>	1.00
<u>nl₁</u> Ē	1.00
Ē	0.60
S	1.00

#### **AC CHARACTERISTICS FOR 74HCT**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL			74HCT								WAVEFORMS
		+25			−40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORING
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nl <sub>0</sub> to nY; nl <sub>1</sub> to nY		16	27		34		41	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E to nY		15	26		33		39	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S to nY		22	37		46		56	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6 and Fig.7

# Quad 2-input multiplexer

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## **AC WAVEFORMS**

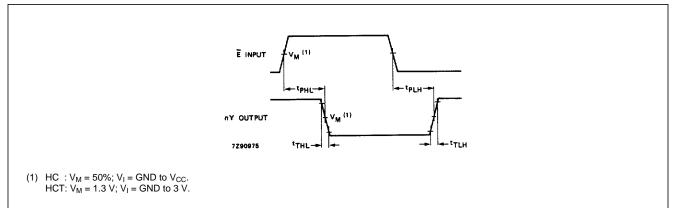
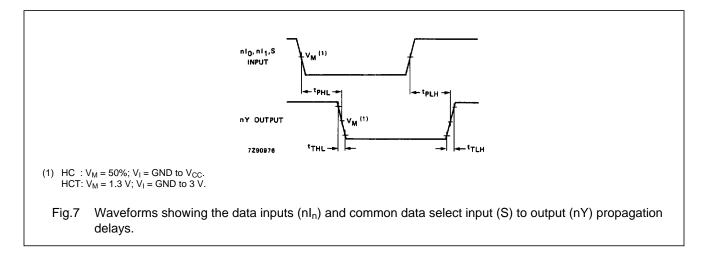


Fig.6 Waveforms showing the enable input  $(\overline{E})$  to output (nY) propagation delays and the output transition times.



# **PACKAGE OUTLINES**

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".